



HARRIS

IRFP140R, IRFP141R IRFP142R, IRFP143R

**N-Channel Power MOSFETs
Avalanche Energy Rated**

August 1991

Features

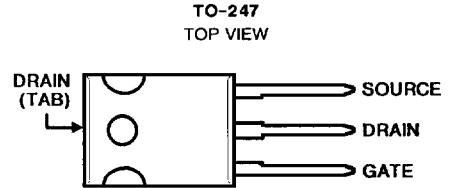
- 27A and 31A, 80V - 100V
- $r_{DS(on)} = 0.077\Omega$ and 0.099Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFP140R, IRFP141R, IRFP142R, and IRFP143R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

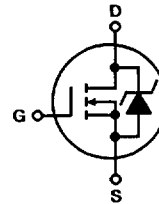
The IRFP types are supplied in the JEDEC TO-247 plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

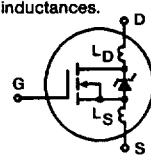
	IRFP140R	IRFP141R	IRFP142R	IRFP143R	UNITS
Drain-Source Voltage (1)	V_{DS} 100	80	100	80	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 100	80	100	80	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 31	31	27	27	A
$T_C = +100^\circ\text{C}$	I_D 22	22	19	19	A
Pulsed Drain Current (3)	I_{DM} 120	120	110	110	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 180	180	180	180	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (4)	E_{as} 100	100	100	100	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +175	-55 to +175	-55 to +175	-55 to +175	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
- $V_{DD} = 25\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 160\mu\text{H}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 31\text{A}$. See Figures 14 and 15.

Specifications IRFP140R, IRFP141R, IRFP142R, IRFP143R

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage IRFP140R, IRFP142R IRFP141R, IRFP143R	BV _{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V	
			80	-	-	V	
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V	
Gate-Source Leakage Forward	I _{GSS}	$V_{GS} = 20V$	-	-	100	nA	
Gate-Source Leakage Reverse	I _{GSS}	$V_{GS} = -20V$	-	-	-100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	250	μA	
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_J = +125^\circ\text{C}$	-	-	1000	μA	
On-State Drain Current (Note 2) IRFP140R, IRFP141R IRFP142R, IRFP143R	I _{D(ON)}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = 10V$	31	-	-	A	
			27	-	-	A	
Static Drain-Source On-State Resistance (Note 2) IRFP140R, IRFP141R IRFP142R, IRFP143R	r _{DS(ON)}	$V_{GS} = 10V, I_D = 19A$	-	0.055	0.077	Ω	
			-	0.077	0.099	Ω	
Forward Transconductance (Note 2)	g _{fs}	$V_{DS} \geq 50V, I_D = 19A$	9.3	14	-	S(tf)	
Input Capacitance	C _{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$ See Figure 10	-	1275	-	pF	
Output Capacitance	C _{OSS}		-	550	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	160	-	pF	
Turn-On Delay Time	t _{d(ON)}	$V_{DD} = 50V, I_D \approx 28A, R_G = 9.1\Omega, R_D = 1.8\Omega$ See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	23	ns	
Rise Time	t _r		-	72	110	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	40	60	ns	
Fall Time	t _f		-	50	75	ns	
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g		$V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 \text{ Max Rating}$. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	59	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC	
Gate-Drain ("Miller") Charge	Q _{gd}		-	21	-	nC	
Internal Drain Inductance	L _D	Measured between the contact screw on header that is closer to source and gate pins and center of die.		-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.		-	12.5	-	nH
Junction-to-Case	R _{θJC}		-	-	0.83	$^\circ\text{C/W}$	
Case-to-Sink	R _{θCS}	Mounting surface flat, smooth and greased	-	0.1	-	$^\circ\text{C/W}$	
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	30	$^\circ\text{C/W}$	

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Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	31	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	120	A
Diode Forward Voltage (Note 2)	V _{SD}	$T_J = +25^\circ\text{C}, I_S = 31A, V_{GS} = 0V$	-	-	2.5	V
Reverse Recovery Time	t _{rr}	$T_J = +25^\circ\text{C}, I_F = 28A, dI_F/dt = 100A/\mu s$	70	150	300	ns
Reverse Recovered Charge	Q _{RR}	$T_J = +25^\circ\text{C}, I_F = 28A, dI_F/dt = 100A/\mu s$	0.44	0.91	1.9	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
 2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
 4. $V_{DD} = 25V$, Start $T_J = +25^\circ\text{C}$, $L = 160\mu H$, $R_G = 50\Omega$, $I_{PEAK} = 31A$. (See Figures 14 & 15)

IRFP140R, IRFP141R, IRFP142R, IRFP143R

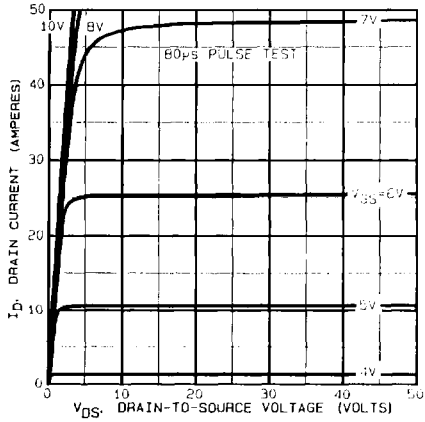


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

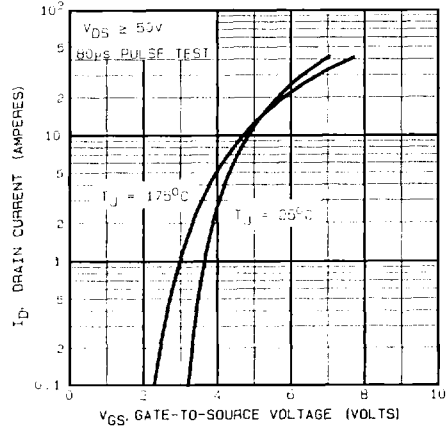


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

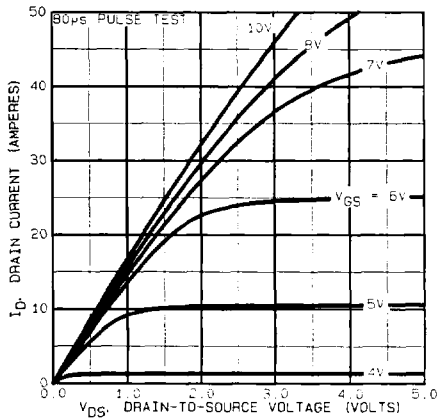


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

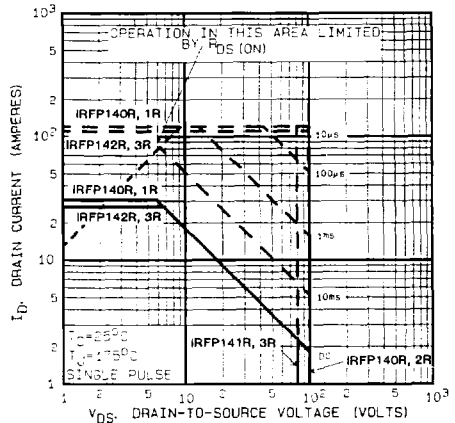


FIGURE 4. MAXIMUM SAFE OPERATING AREA

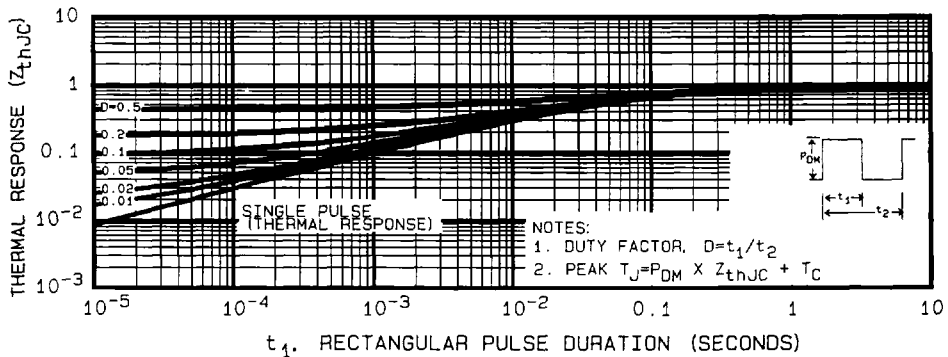


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

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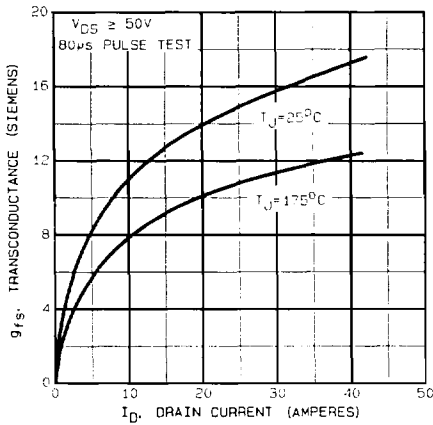


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

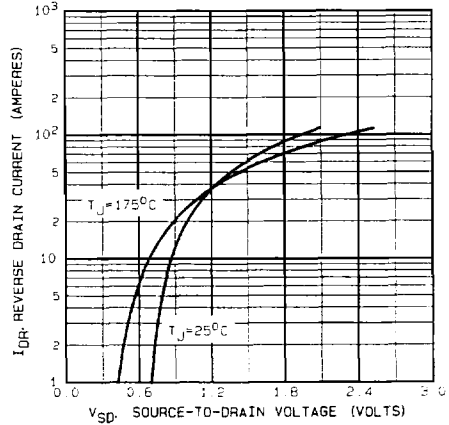


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

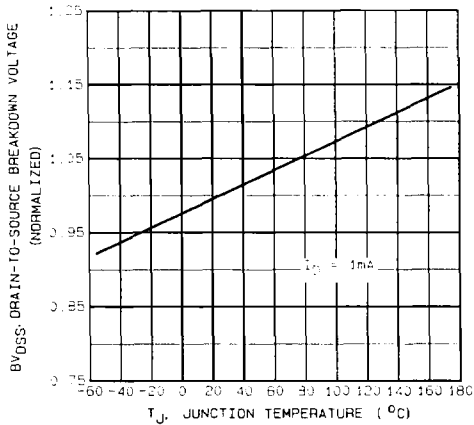


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

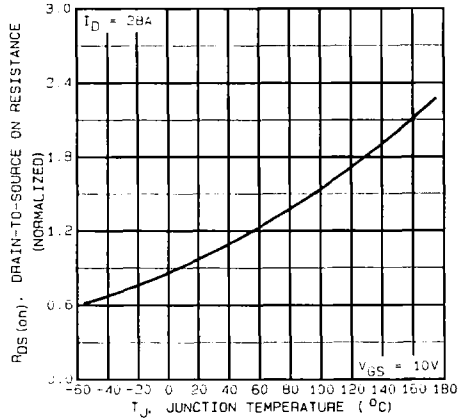


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

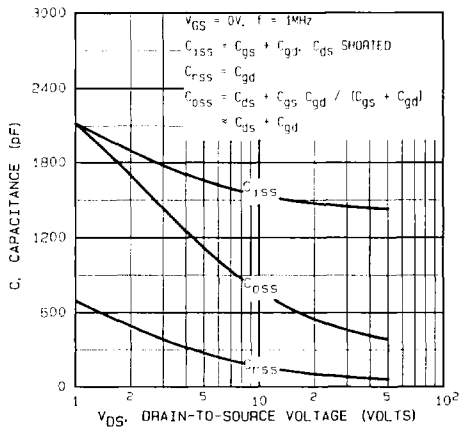


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

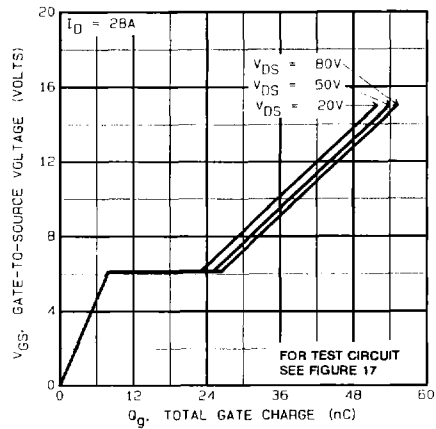


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

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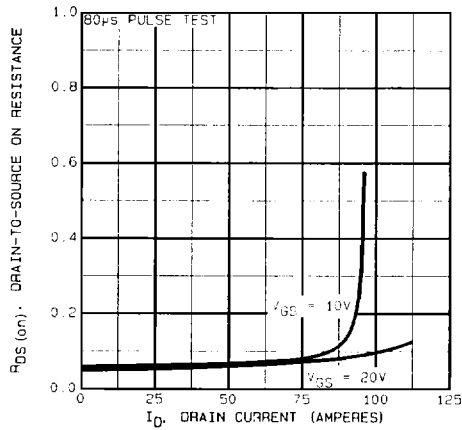


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

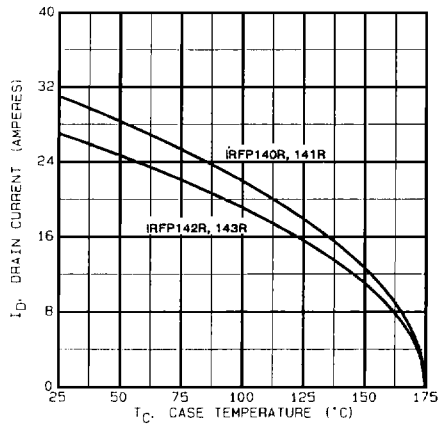


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

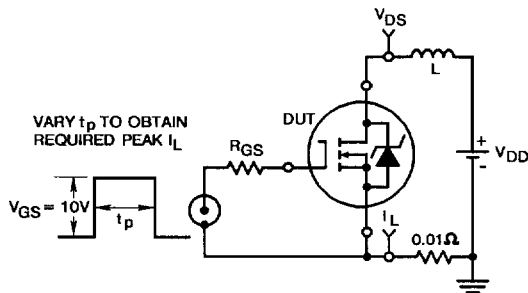


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

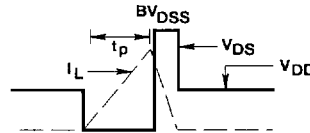


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

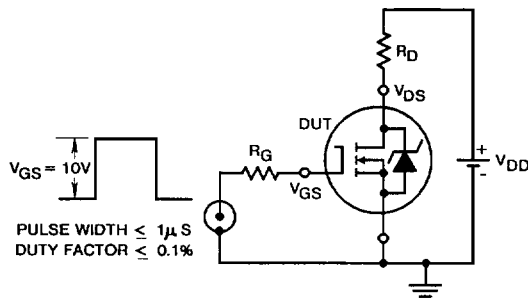


FIGURE 16. SWITCHING TIME TEST CIRCUIT

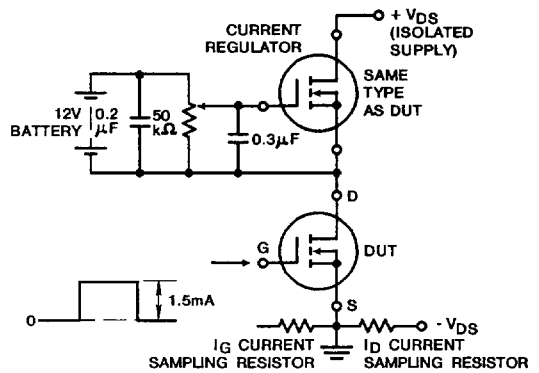


FIGURE 17. GATE CHARGE TEST CIRCUIT