NCP1529ASNT1GEVB, NCP1529MUTBGEVB

NCP1529 Series 1.7 MHz, 1 A, High Efficiency, Low Ripple, Adjustable Output Voltage Step-down Converter Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Overview

The NCP1529 step−down DC−DC converter is a monolithic integrated circuit for portable applications powered from one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries.

The device – available in an adjustable output voltage from 0.9 V to 3.9 V – is able to deliver up to 1 A. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 1.7 MHz (nominal) oscillator which reduces component size by allowing a small inductor and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Additional features include integrated soft−start, cycle−by−cycle current limiting and thermal shutdown protection. The NCP1529 is available in a space saving, low profile 2x2 x 0.5 mm UDFN6 package and TSOP−5 package.

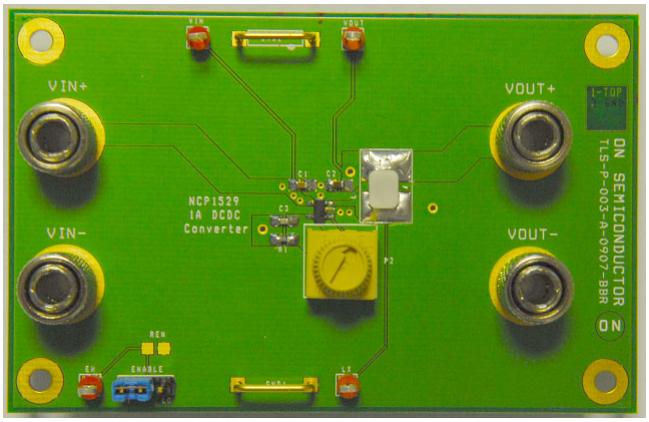

Figure 1. NCP1529ASNT1GEVB Board Picture in TSOP−5

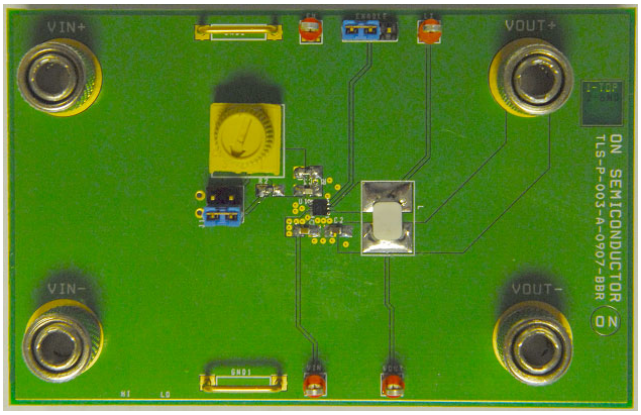

Figure 2. NCP1529MUTBGEVB Board Picture in UDFN−6

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins (Note 1)	V_{max}	7.0	V
Maximum Voltage EN, ENI2C, SDA, SCL	V_{max}	V_{IN} + 0.3	V
Thermal Resistance, Junction−to−Air (TSOP−5 Package) Thermal Resistance using TSOP−5 Recommended Board Layout (Note 8)	$R_{\theta JA}$	300 110	°C/W
Thermal Resistance, Junction−to−Air (UDFN6 Package) Thermal Resistance using UDFN6 Recommended Board Layout (Note 8)	$R_{\theta JA}$	220 40	°C/W
Operating Ambient Temperature Range (Notes 6 and 7)	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature (Notes 6 and 7)	T_J	−40 to 125	°C
Latchup Current Maximum Rating (T_A = 85°C) (Note 4) Other Pins	Lu	±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level (Note 5)	MSL	1	per IPC

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
4. Latchup current maximum rating per JEDEC standard: JESD78.
5. JEDEC Standard: J−STD−020A.
6. In applications with high power dissipation (low V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. Board design considerations − thermal dissipation vias, traces or planes and PCB material − can significantly improve junction to air thermal resistance $R_{\theta JA}$ (for more information, see design and layout consideration section). Environmental conditions such as ambient temperature T_A brings thermal limitation on maximum power dissipation allowed.
   The following formula gives calculation of maximum ambient temperature allowed by the application:
   $T_{A\ MAX} = T_{J\ MAX} - (R_{\theta JA} \times P_d)$
   Where: T_J is the junction temperature,
   P_d is the maximum power dissipated by the device (worst case of the application),
   and $R_{\theta JA}$ is the junction−to−ambient thermal resistance.
7. To prevent permanent thermal damages, this device include a thermal shutdown which engages at 180°C (typ).
8. Board recommended TSOP−5 and UDFN−6 layouts are described on Layout Considerations section.

ELECTRICAL CHARACTERISTICS

For Electrical Characteristic, please report to our NCP1529 datasheet available on our website: http://onsemi.com.

Table 2. NCP1529 – BOARD CONNECTIONS

Symbol	Switch Descriptions
INPUT POWER	
VIN+	This is the positive connection for power supply.
VIN–	This is the return connection for the power supply
GND1, GND2	Ground clip
SETUP	
ENABLE	To enable the buck converter, connect a shorting jumper between ENABLE–1 and ENABLE–2. To disable the buck converter, connect a shorting jumper between ENABLE–3 and ENABLE–2.
SELECT (UDFN package)	A shorting jumper must be used to select an output voltage of 1.2V or an adjustable output voltage.
OUTPUT POWER	
VOUT+	This is the positive connection of the output voltage.
VOUT–	This is the return connection of the output voltage.
TEST POINT	
TPVIN	This is the test point of the input voltage.
TPEN	This is the test point of the enable pin.
TPSW	This is the test point of the inductor voltage.
TPVOUT	This is the test point of the output voltage.

NCP1529 − BOARD SCHEMATIC

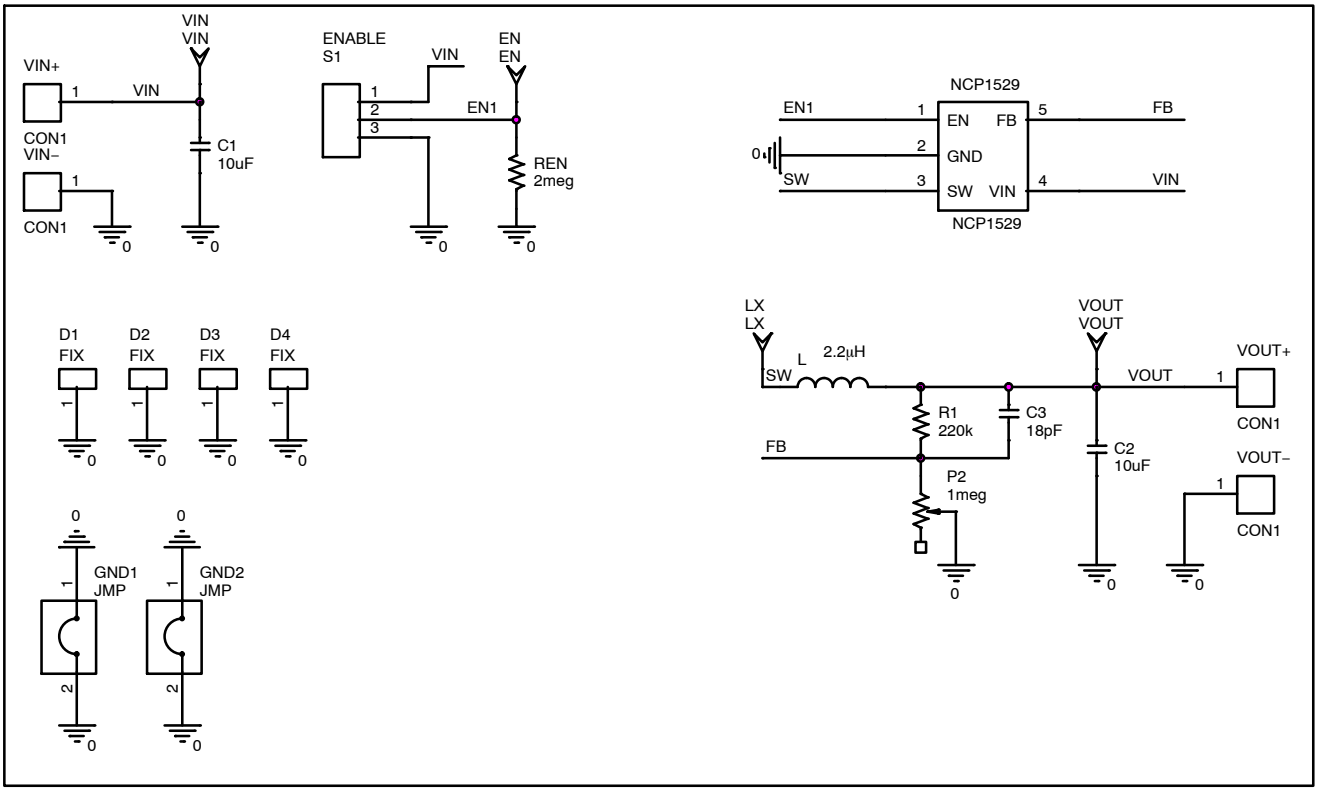

Figure 3. Board Schematic in TSOP−5

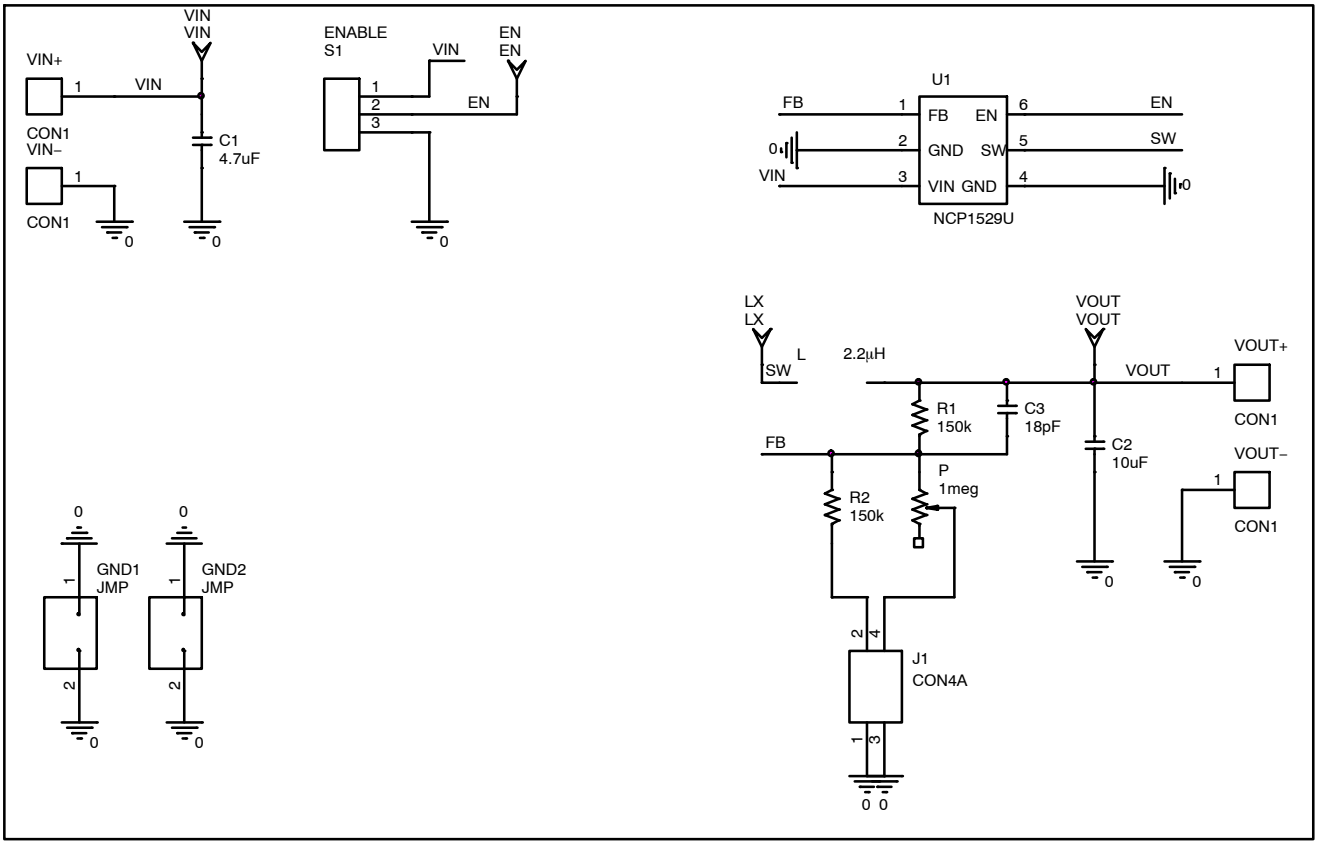

Figure 4. Board Schematic in UDFN6

NCP1529 – TEST PROCEDURE

Equipment Needed

Power supply
Digital Volt Meter
Digital Amp Meter

Test

1. Jumper ENABLE (and SELECT for the UDFN6 package) should be open.
2. Set the power supply to 3.6 V and the current limit of at least 1.5 A.
3. Connect Vin+ to power supply and Vin− to ground. The DC current measurement on Vin+ line should be around 0.3 μA.
4. For the UDFN6 package, close the SELECT connector to the potentiometer.
5. Close EN connector.
6. Modify P2 potentiometer to get Vout to 1.2 V. Output voltage value is defined by : Vout = 0.6 x (1 + R1/R2)
7. The DC current measurement on Vin+ line should be around 36 μA. The part operates in PFM mode:

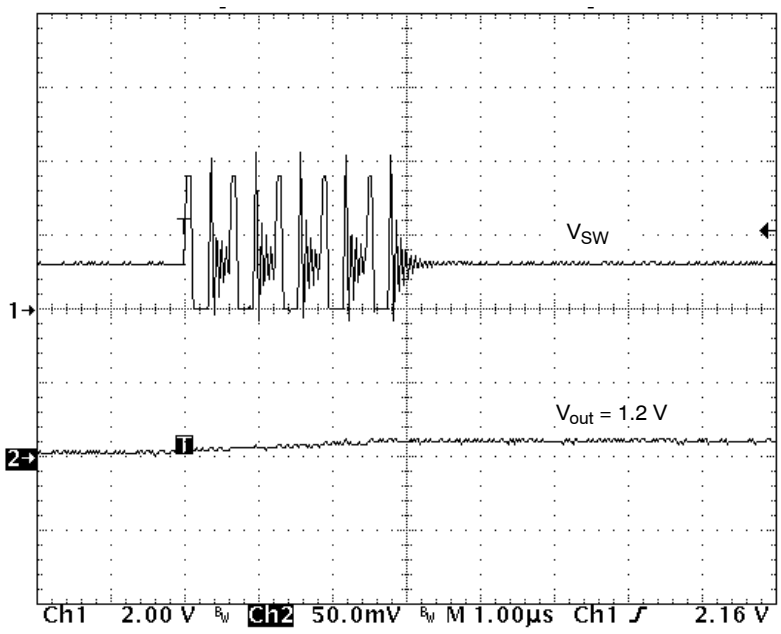

Figure 5. V_{SW} and V_{out} in PFM Mode

8. Increase Output current to 1 A. The part works in PWM mode with a low ripple:

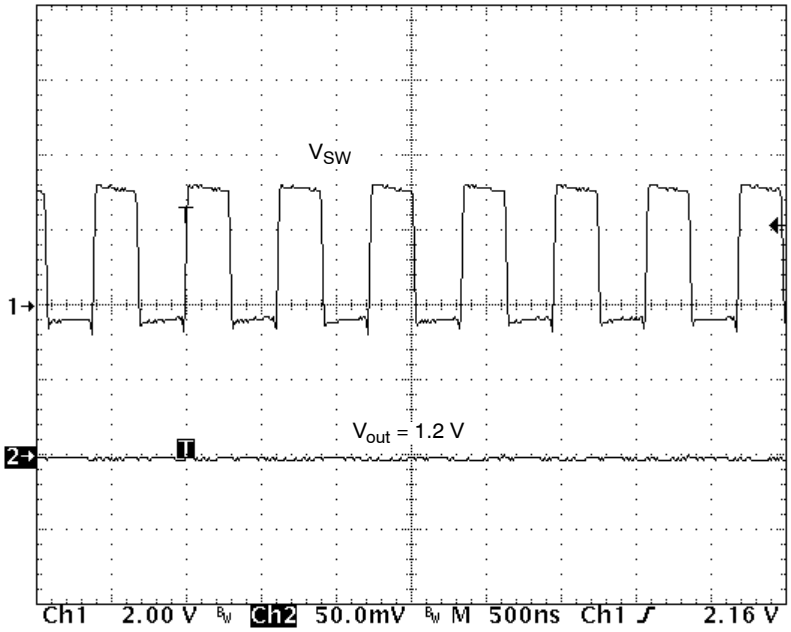

Figure 6. V_{SW} and V_{out} in PWM Mode

9. Remove J5 connector. The DC current measurement on Vp line should be back around 0.3 μA.

NCP1529 – COMPONENTS SELECTION

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1529, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin

Table 3. LIST OF INPUT CAPACITOR

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
Taiyo Yuden	JMK212BY475MG	4.7 μF
TDK	C2012X5R0J475KT	4.7 μF
	C1608X5R0J475KT	

Output L–C Filter Design Considerations

The NCP1529 operates at 1.7 MHz frequency and uses current mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L–C filter must be selected to work with internal compensation. For NCP1529, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 10 μF.

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 10\ \mu F}} = 34\ kHz \quad \text{(eq. 1)}$$

The device operates with inductance value of 2.2 μH. If the corner frequency is moved, it is recommended to check the loop stability depending of the accepted output ripple voltage and the required output current. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 4. L–C FILTER EXAMPLE

Inductance (L)	Output Capacitor (C_{OUT})
2.2 μH	10 μF
4.7 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 2)}$$

- ΔI_L: Peak to peak inductor ripple current
- L: Inductor value
- f_{SW}: Switching frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \quad \text{(eq. 3)}$$

- $I_{L(max)}$: Maximum inductor current
- $I_{O(max)}$: Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 5. LIST OF INDUCTOR

FDK	MIPW3226 Series
TDK	VLF3010AT Series
	TFC252005 Series
Taiyo Yuden	LQ CBL2012
Coil Craft	DO1605−T Series
	LPS3008

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR\right) \quad \text{(eq. 4)}$$

Table 6. LIST OF OUTPUT CAPACITOR

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5R0J475	4.7 μuF
	C1608X5R0J475	
	C2012X5R0J106	10 μF

Feed−Forward Capacitor Selection

The feed−forward capacitor sets the feedback loop response and is critical to obtain good loop stability. Given that the compensation is internally fixed, an 18 pF ceramic capacitor is needed. Choose a small ceramic capacitor X7R or X5R or COG dielectric.

NCP1529 − BILL OF MATERIAL

Table 7. BOM IN TSOP−5 PACKAGE

Designator	Qty	Description	Value	Toler-ance	Foot-print	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	TSOP−5	ON Semiconductor	NCP1529
C1	1	Ceramic Capacitor	4.7 μF, 6.3 V, X5R	10%	0603	TDK	C1608X5R0J475
C2	1	Ceramic Capacitor	10 μF, 6,3 V, X5R	10%	0603	TDK	C1608X5R0J106
C3	1	Ceramic Capacitor	18 pF, 50 V, COG	5%	0603	TDK	C1608C0G1H180
R1	1	SMD Resistor	110k	1%	0603	std	std
P2	1	Potentiometer	1meg	10%		Vishay Spectrol	63M−T607−105
L1	1	Inductor	2,2 μH	20%	1605	Coilcraft	DO1605T−222MLB
VIN, VOUT	4	Connector	NA	NA	NA	Emerson Network Power Connectivity Solutions	111−2223−001

Table 7. BOM IN TSOP−5 PACKAGE

Designator	Qty	Description	Value	Toler-ance	Foot-print	Manufacturer	Manufacturer Part Number
ENABLE	1	3 Pin Jumper Header	NA	NA	2,54mm	TYCO/AMP Molex/Waldom	5−826629−0 90120−0160
GND1, GND2	2	Jumper for GND	NA	NA	10.16mm	Harwin Molex / Waldom	D3082−01 90120−0160
EN, SW, VIN, VOUT	4	Test Point Type 3	NA	NA	f 1.60mm	Keystone	5010
PCB	1	87 mm x 57 mm x 1.0 mm 4 Layers	NA	NA	NA	Any	TLS−P−003−A−0907 −BBR

Table 8. BOM IN UDFN−6 PACKAGE

Designator	Qty	Description	Value	Toler-ance	Foot-print	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	UDFN6	ON Semiconductor	NCP1529
C1	1	Ceramic capacitor	4.7 μF, 6.3 V, X5R	10%	0603	TDK	C1608X5R0J475
C2	1	Ceramic capacitor	10 μF, 6.3 V, X5R	10%	0603	TDK	C1608X5R0J106
C3	1	Ceramic capacitor	18 pF, 50 V, COG	5%	0603	TDK	C1608C0G1H180
R1, R2	2	SMD resistor	150k	1%	0603	std	std
P2	1	Potentiometer	1meg	10%		Vishay Spectrol	63M−T607−105
L1	1	Inductor	2.2 μH	20%	1605	Coilcraft	DO1605T−222MLB
VIN, VOUT	4	Connector	NA	NA	NA	Emerson Network Power Connectivity Solutions	111−2223−001
ENABLE	1	3 Pin Jumper Header	NA	NA	2,54mm	TYCO/AMP Molex/Waldom	5−826629−0 90120−0160
SELECT	J1	2x2 Pin Jumper Header	NA	NA	2,54mm	TYCO/AMP Molex/Waldom	6−166591−5 90131−0140
GND1, GND2	2	Jumper for GND	NA	NA	10,16mm	Harwin Molex/Waldom	D3082−01 90120−0160
EN, SW, VIN, VOUT	4	Test point type 3	NA	NA	ϕ 1,60mm	Keystone	5010
PCB	1	87mm x 57mm x 1.0 mm 4 Layers	NA	NA	NA	Any	TLS−P−003−A−0907 −BBR

NCP1529 – PCB LAYOUT GUIDELINES

LAYOUT CONSIDERATIONS

Electrical Layout Considerations

Implementing a high frequency DC−DC converter requires respect of some rules to get a powerful portable application. Good layout is key to prevent switching regulators to generate noise to application and to themselves.

Electrical layout guide lines are:

- Use short and large traces when large amount of current is flowing.
- Keep the same ground reference for input and output capacitors to minimize the loop formed by high current path from the battery to the ground plane.
- Isolate feedback pin from the switching pin and the current loop to protect against any external parasitic signal coupling. Add a feed−forward capacitor between V_{OUT} and FB which adds a zero to the loop and participates to the good loop stability. A 18pF capacitor is recommended to meet compensation requirements.

A four layer PCB with a ground plane and a power plane will help NCP1529 noise immunity and loop stability.

Thermal Layout Considerations

High power dissipation in small package leads to thermal consideration such as:

- Enlarge V_{IN} trace and added several vias connected to power plane.
- Connect GND pin to top plane.
- Join top, bottom and each ground plane together using several free vias in order to increase radiator size.

For high ambient temperature and high power dissipation requirements, UDFN6 package using exposed pad connected to main radiator is recommended. Refer to Notes 6, 7, and 8.

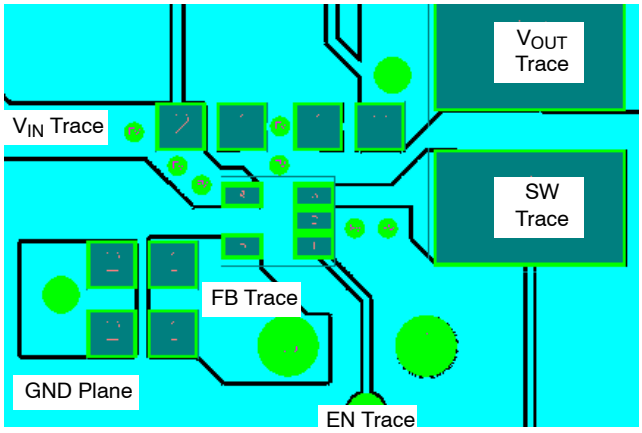

Figure 7. TSOP−5 Recommended Board Layout

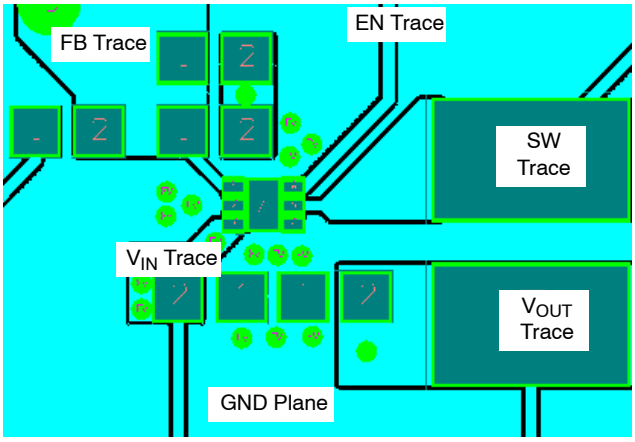

Figure 8. UDFN6 Recommended Board Layout

NCP1529 − PCB LAYOUT OF TSOP−5 DEMO BOARD

Board reference: TLS−P−003−A−0907−BBR

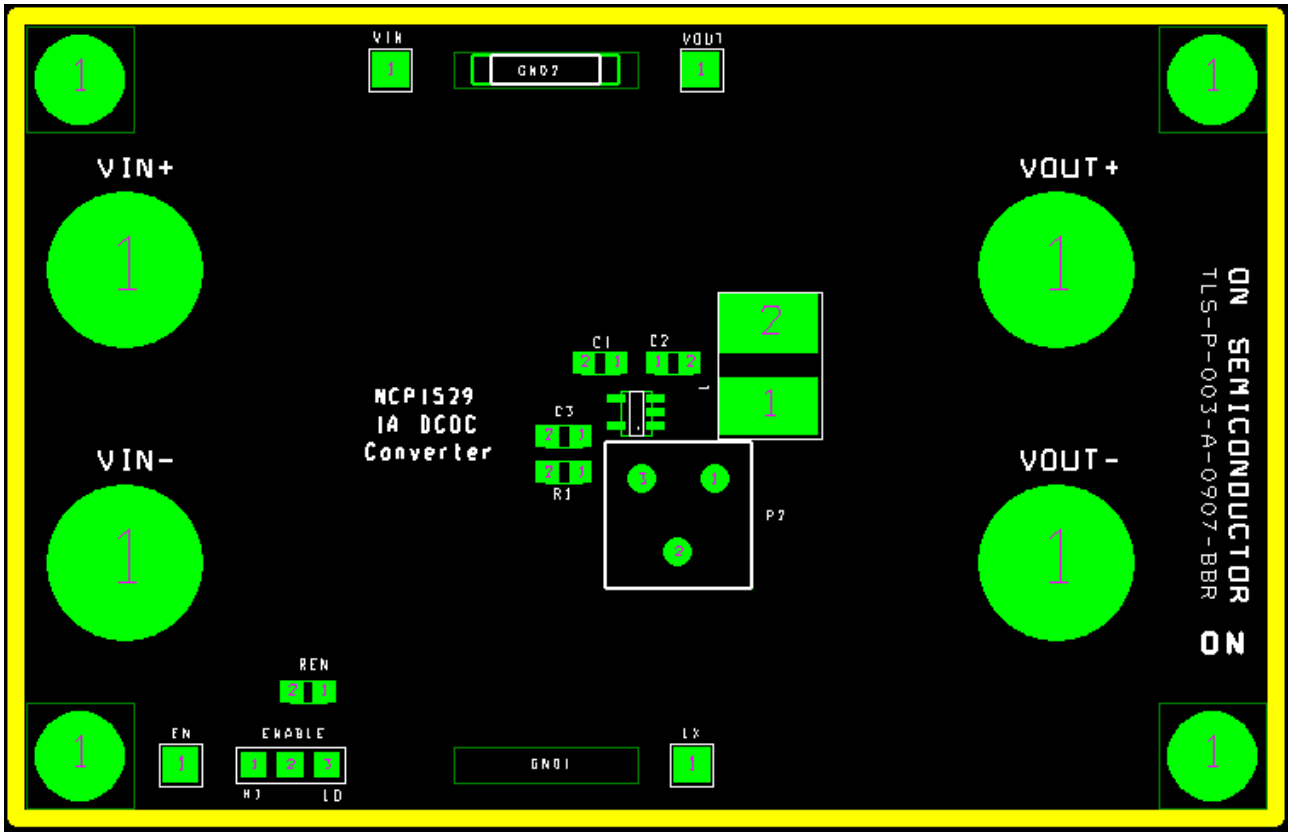

Figure 9. Assembly Layer in TSOP−5

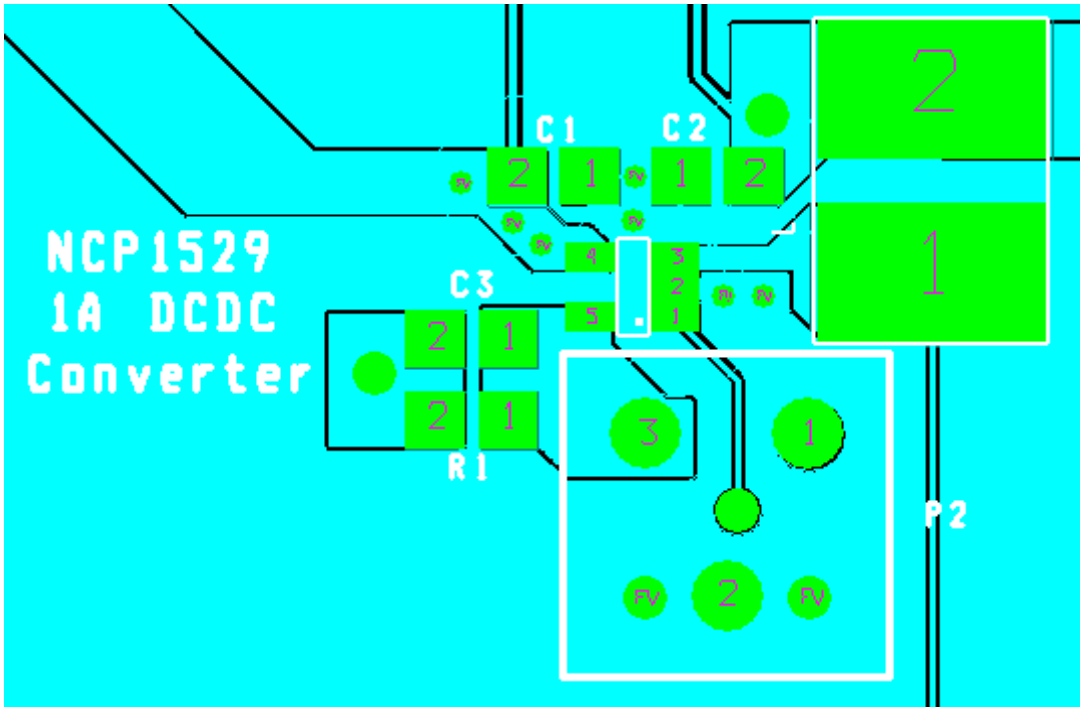

Figure 10. Part Layout in TSOP−5

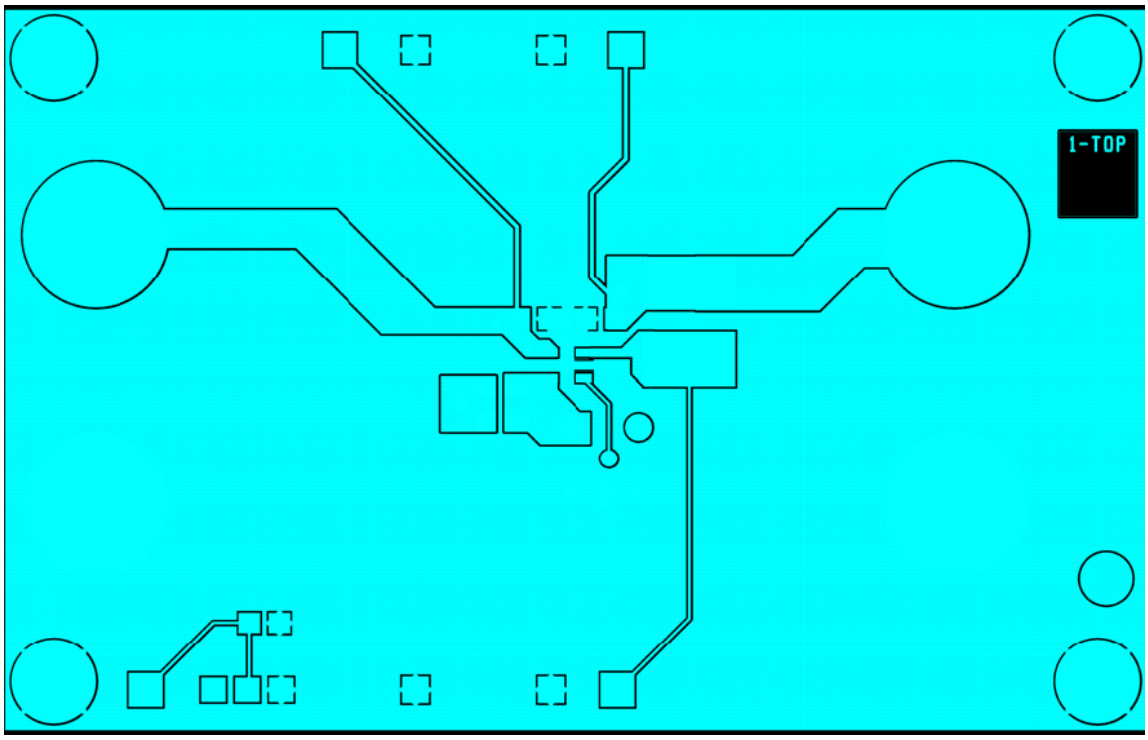

Figure 11. Top Layer Routing in TSOP−5

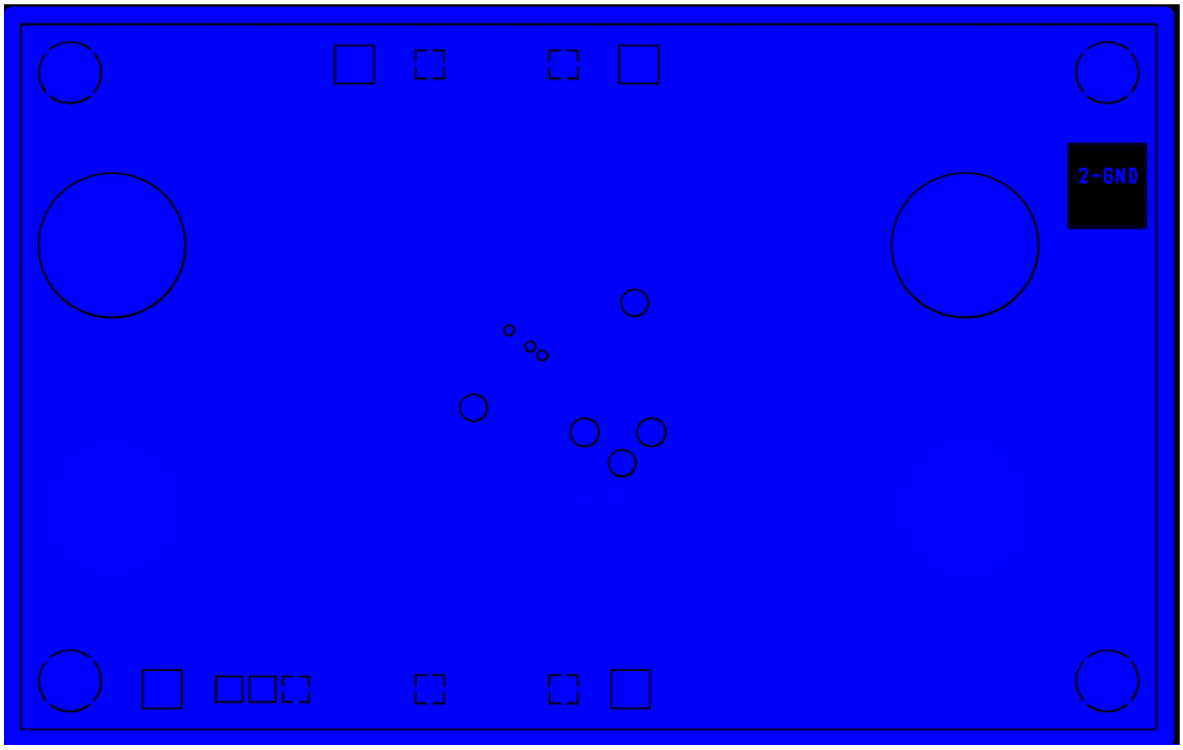

Figure 12. Ground Layer Routing in TSOP−5

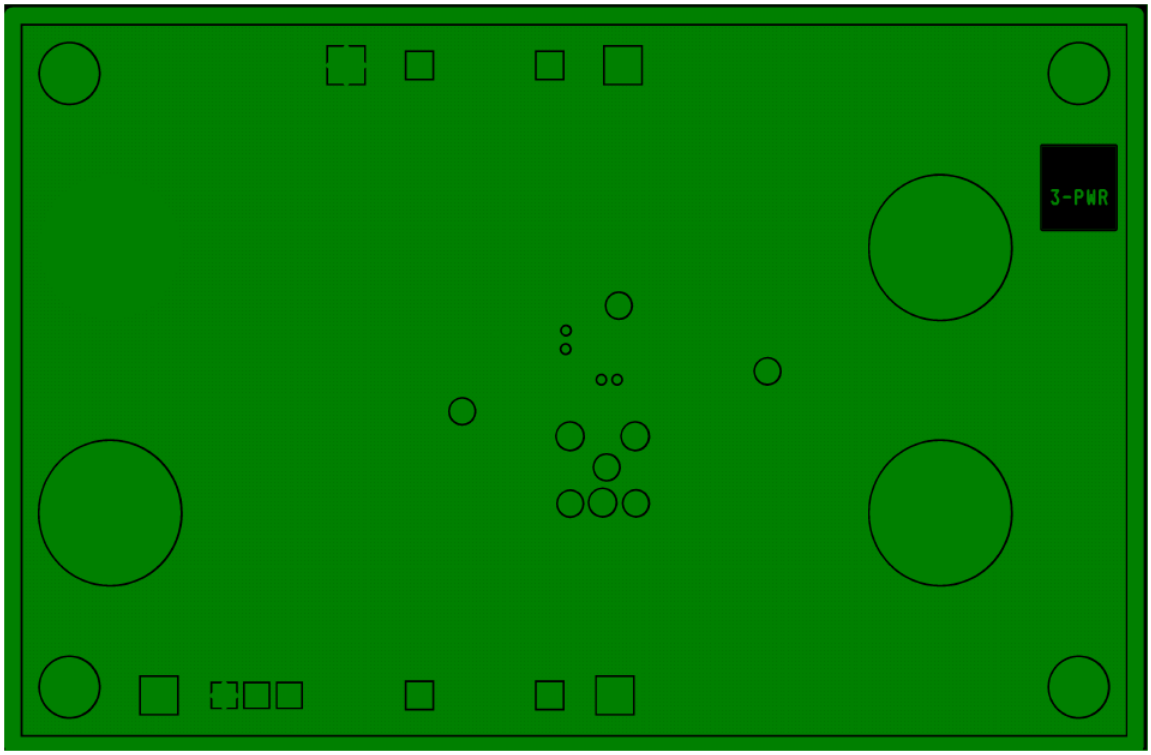

Figure 13. Power Layer Routing in TSOP−5

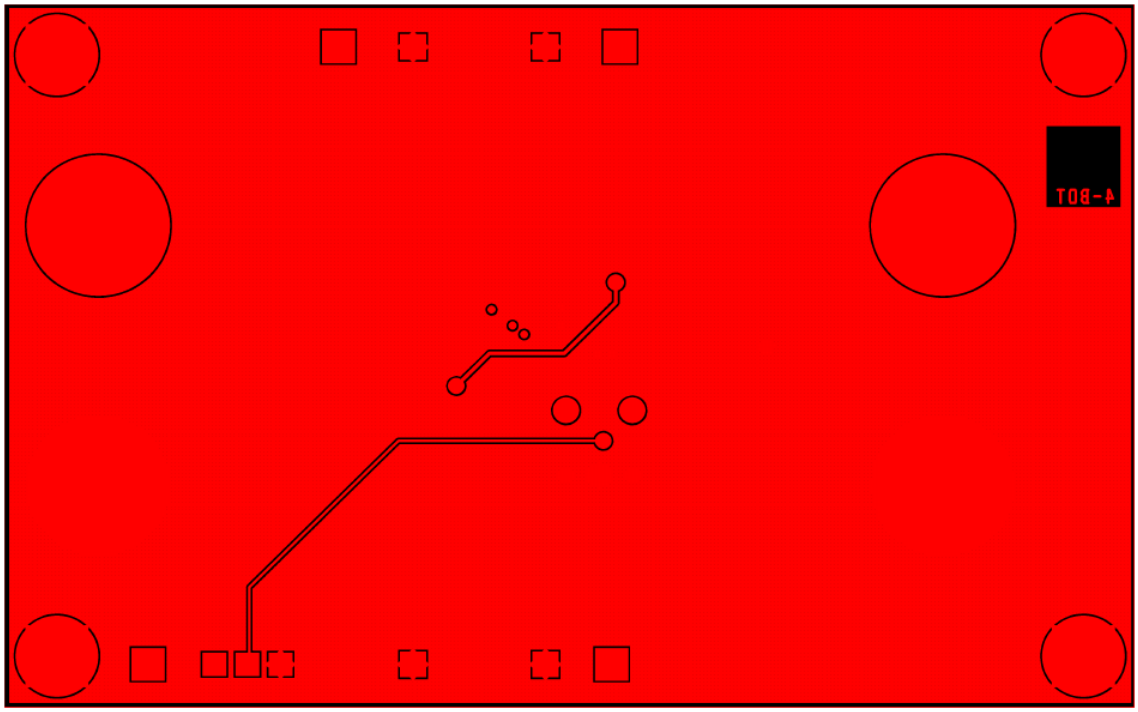

Figure 14. Bottom Layer Routing in TSOP−5

NCP1529 − PCB LAYOUT OF UDFN−6 DEMO BOARD

Board reference: TLS−P−003−A−0907−BBR

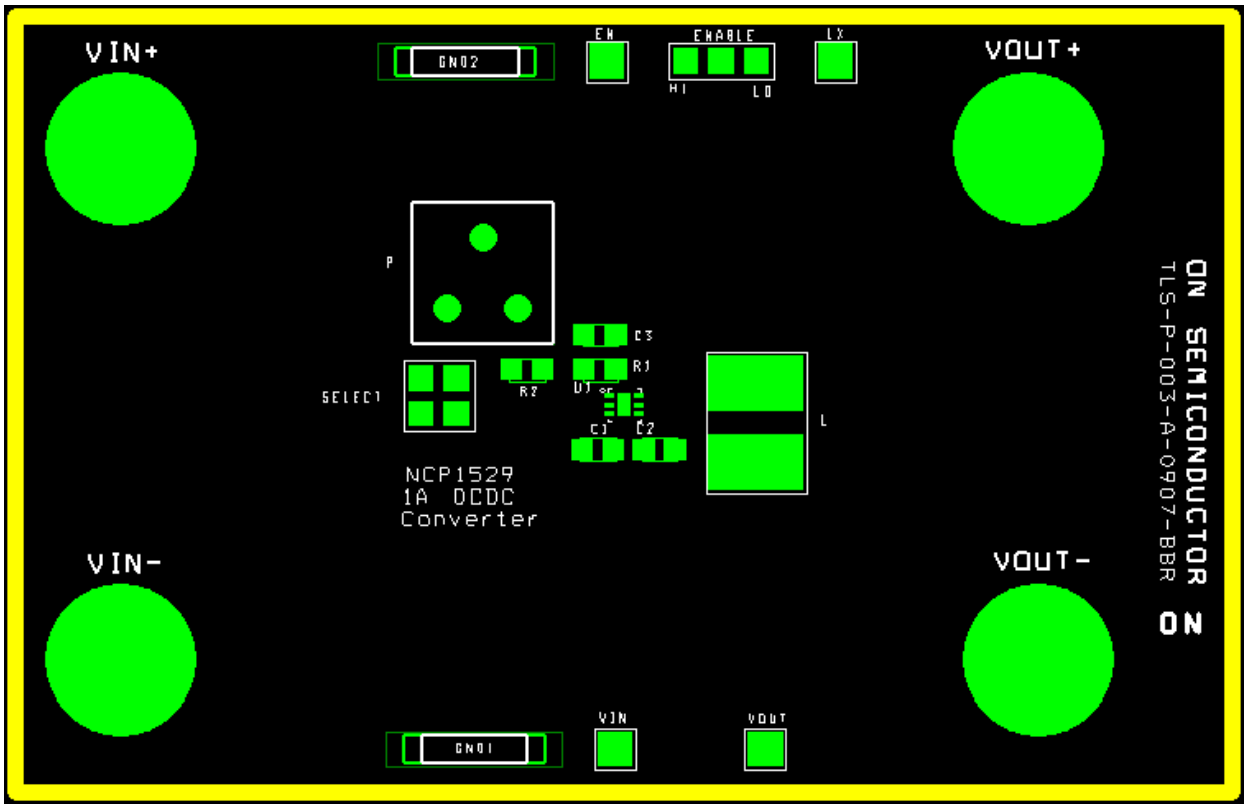

Figure 15. : Assembly Layer in UDFN6

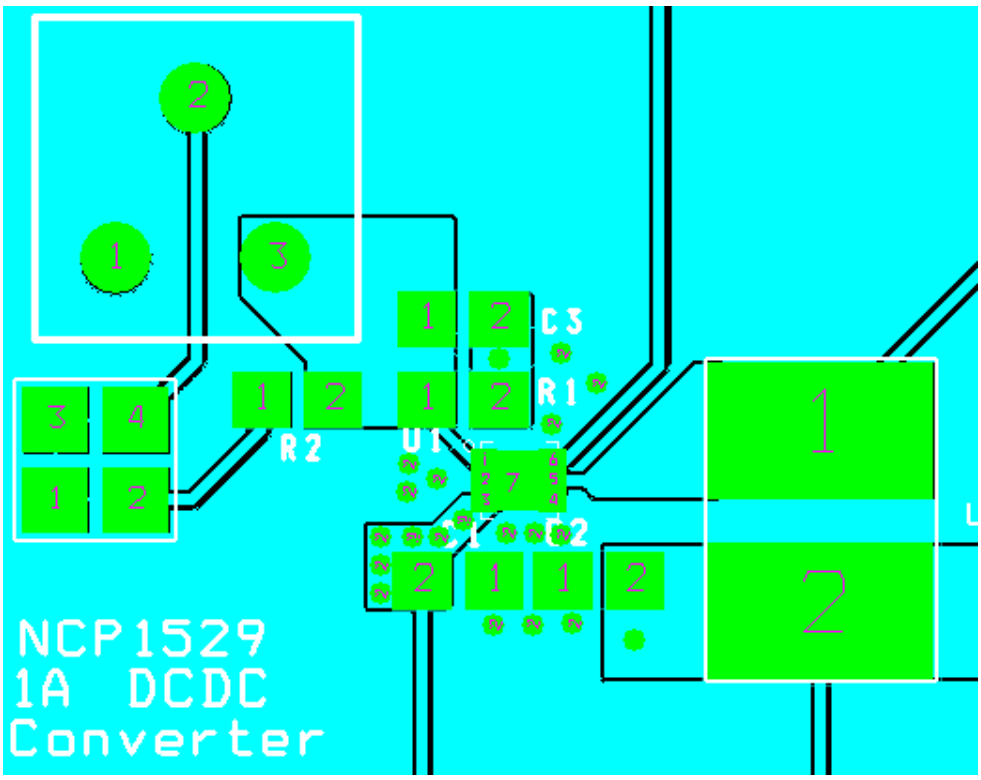

Figure 16. Part Layout in UDFN−6

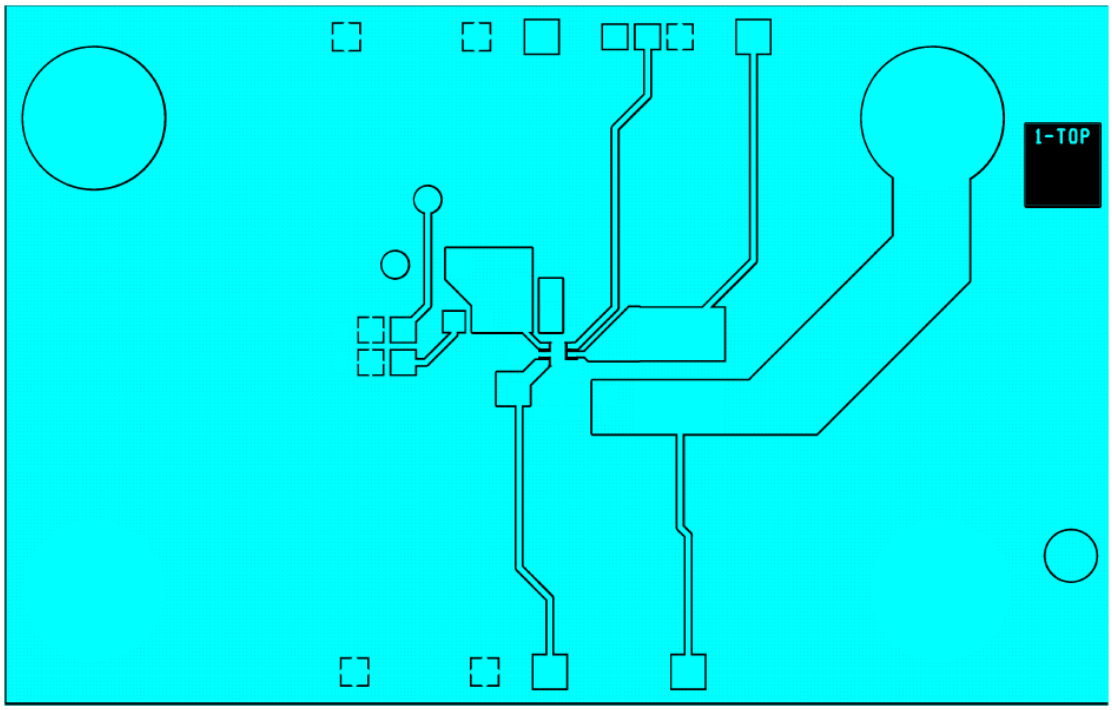

Figure 17. Top Layer Routing in UDFN−6

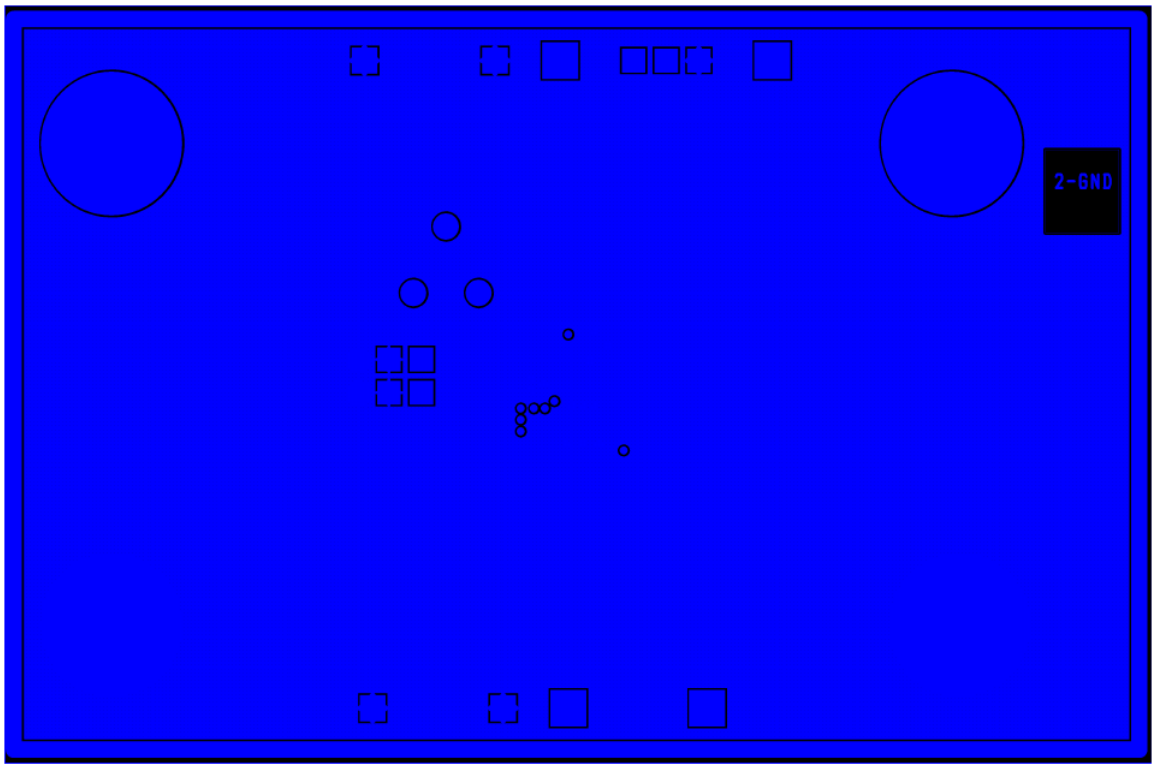

Figure 18. Ground Layer Routing in UDFN6

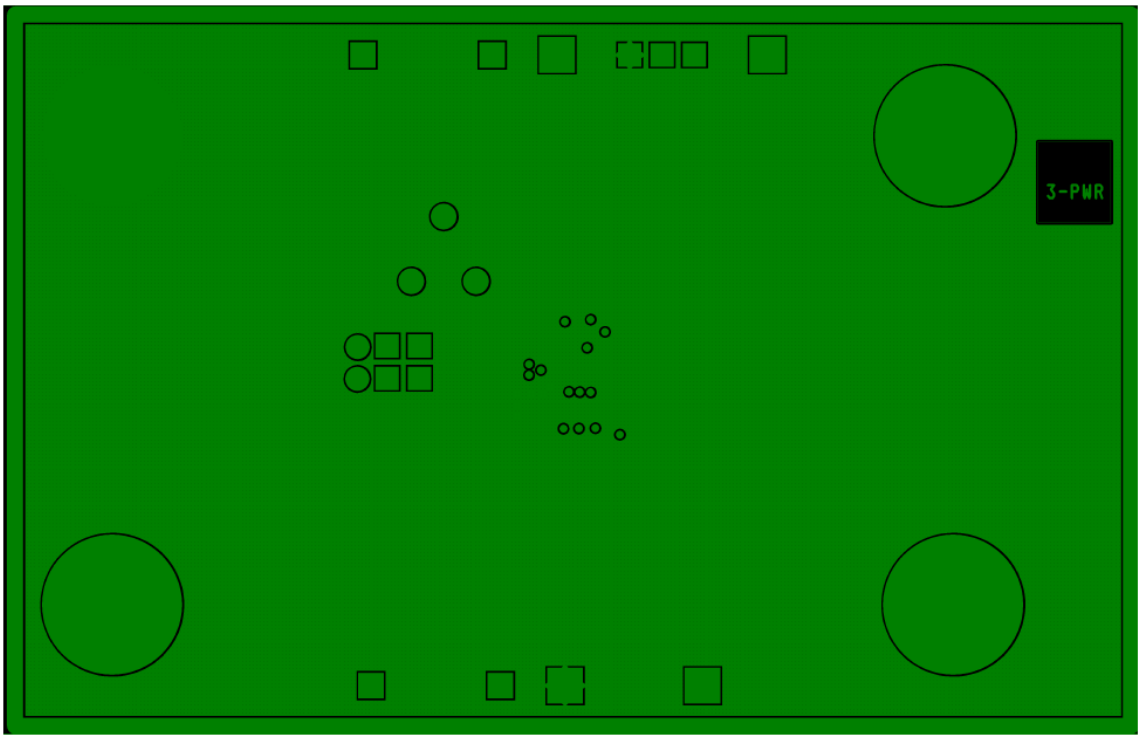

Figure 19. Power Layer Routing in UDFN−6

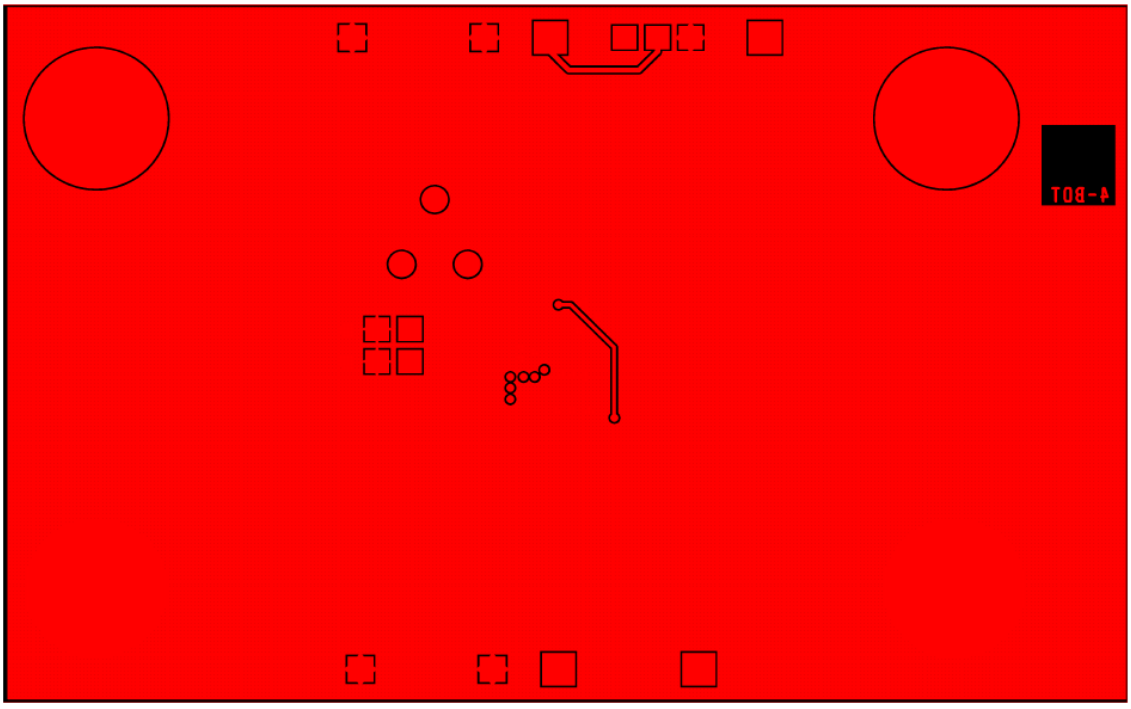

Figure 20. Bottom Layer Routing in UDFN6

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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