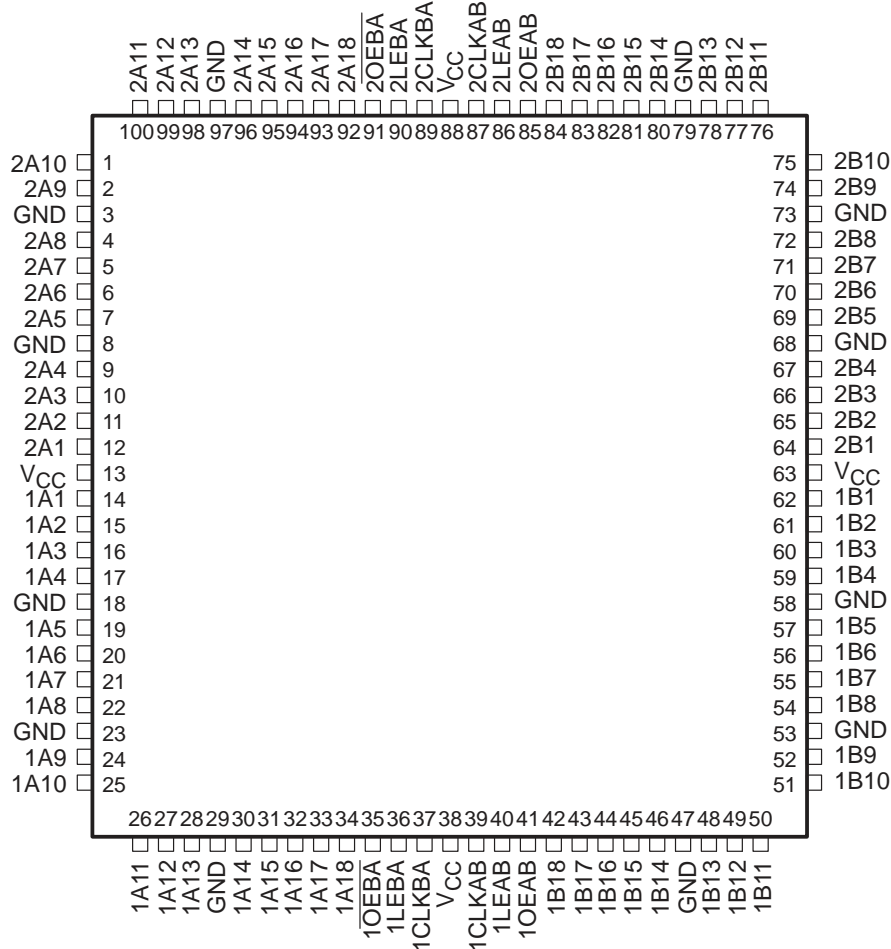


SN54ABTH32501, SN74ABTH32501 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Released as DSCC SMD 5962-9557601NXD
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With 14 × 14-mm Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

†ABTH32501 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



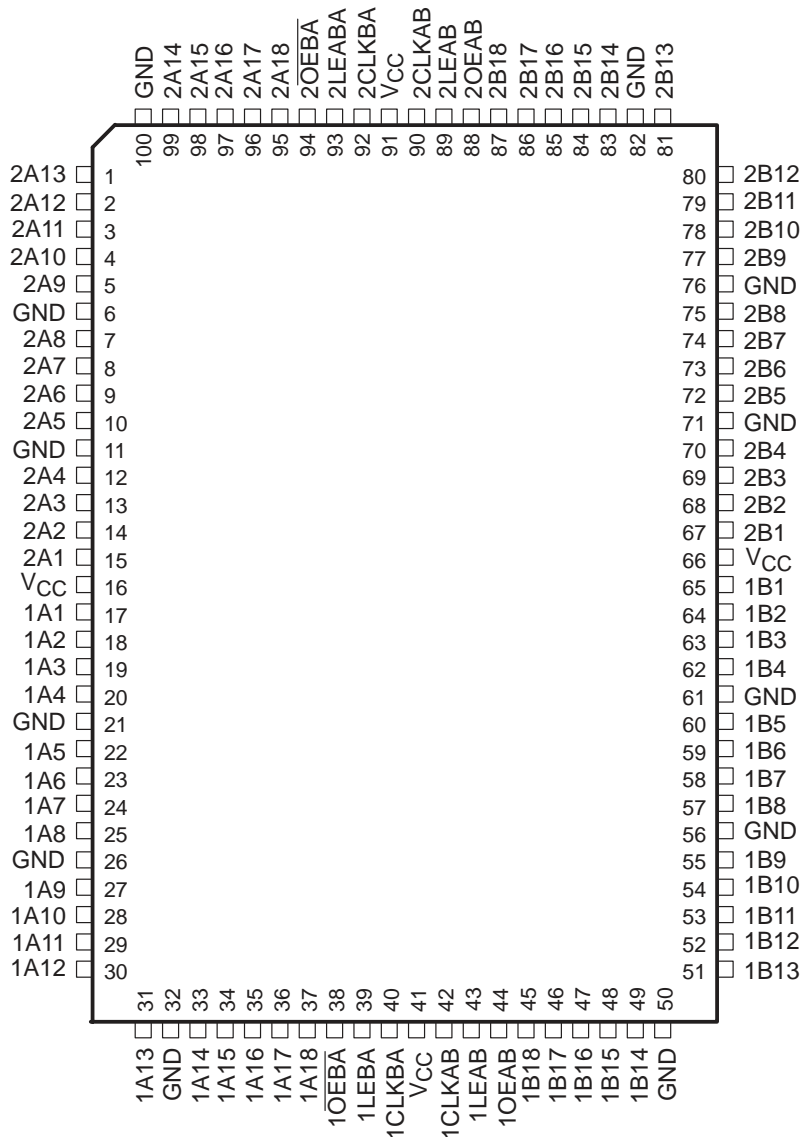
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SN54ABTH32501, SN74ABTH32501 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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SN54ABTH32501 . . . HS PACKAGE† (TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.



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SN54ABTH32501, SN74ABTH32501 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description

These 36-bit UBTs combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, and CLKBA.

Output-enable OEAB is active high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state. The output enables are complementary (OEAB is active high, and \overline{OEBA} is active low).

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32501 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH32501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

| INPUTS | | | | OUTPUT |
|--------|------|-------|---|------------------|
| OEAB | LEAB | CLKAB | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | H | X | B_0^{\ddagger} |
| H | L | L | X | B_0^{\S} |

† A-to-B data flow is shown: B-to-A flow is similar, but uses \overline{OEBA} , LEBA, and CLKBA.

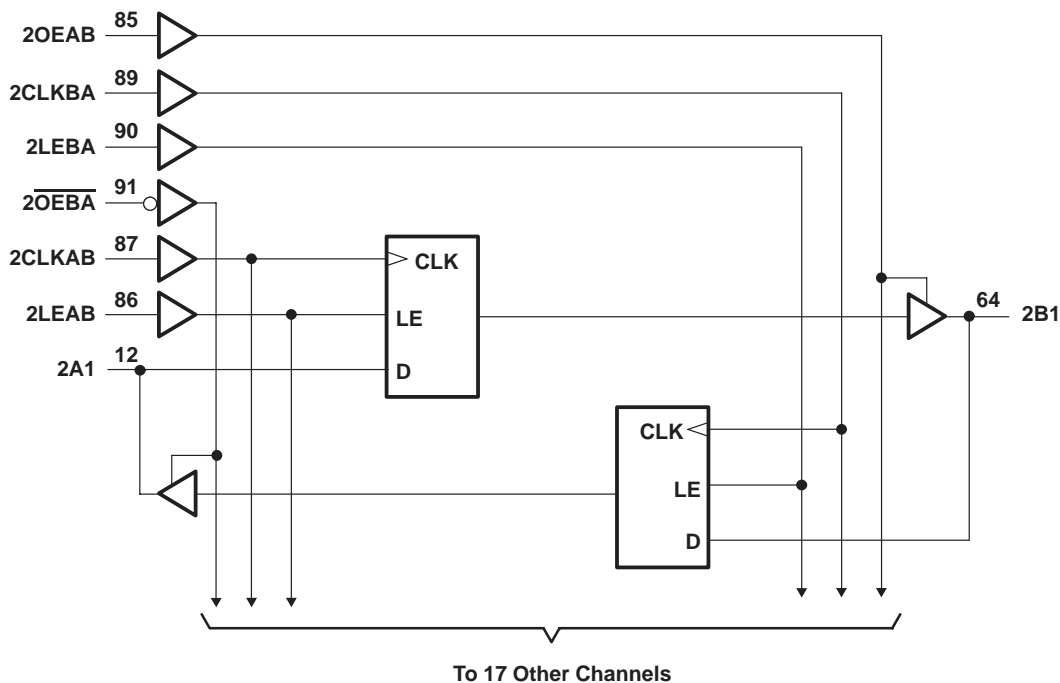
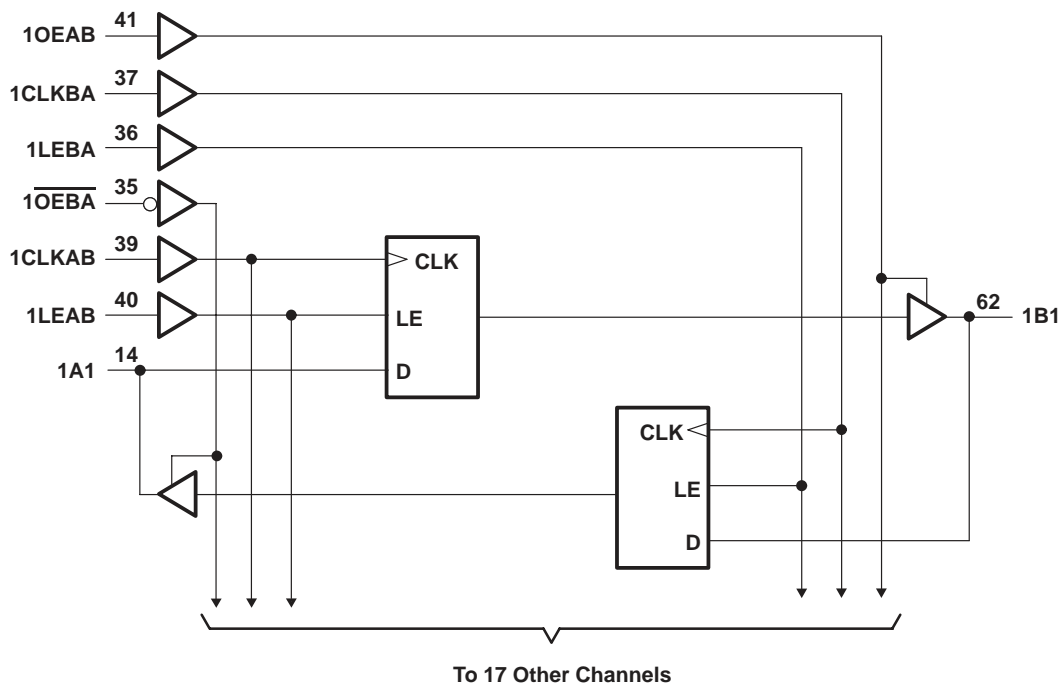
‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

SN54ABTH32501, SN74ABTH32501 36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the PZ package.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | –0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABTH32501 | 96 mA |
| SN74ABTH32501 | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): PZ package | 50°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

| | | SN54ABTH32501 | | SN74ABTH32501 | | UNIT |
|--------------------------|------------------------------------|-----------------|----------|---------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | –24 | | –32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μs/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



SN54ABTH32501, SN74ABTH32501
36-BIT UNIVERSAL BUS TRANSCEIVERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54ABTH32501 | | | SN74ABTH32501 | | | UNIT |
|----------------------|----------------|--|-------------------------|------|------|---------------|------|------|------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | | V _{CC} = 4.5 V, I _I = -18 mA | -1.2 | | | -1.2 | | | V |
| V _{OH} | | V _{CC} = 4.5 V, I _{OH} = -3 mA | 2.5 | | | 2.5 | | | V |
| | | V _{CC} = 5 V, I _{OH} = -3 mA | 3 | | | 3 | | | |
| | | V _{CC} = 4.5 V, I _{OH} = -24 mA | 2 | | | 2 | | | |
| V _{OL} | | V _{CC} = 4.5 V, I _{OL} = 48 mA | 0.55 | | | 0.55 | | | V |
| | | | I _{OL} = 64 mA | | | | 0.55 | | |
| V _{hys} | | | 100 | | | 100 | | | mV |
| I _I | Control inputs | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | | | | ±1 | | | μA |
| | A or B ports | V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND | | | | ±20 | | | |
| | Control inputs | V _{CC} = 5.5 V, V _I = V _{CC} or GND | ±5 | | | | | | |
| | A or B ports | | ±50 | | | | | | |
| I _{I(hold)} | A or B ports | V _{CC} = 4.5 V, V _I = 0.8 V | 100 | | | 100 | | | μA |
| | | | V _I = 2 V | -100 | | | -100 | | |
| I _{OZPU} ‡ | | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE or \overline{OE} = X | ±50 | | | ±50 | | | μA |
| I _{OZPD} ‡ | | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE or \overline{OE} = X | ±50 | | | ±50 | | | μA |
| I _{off} | | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | | ±100 | | | μA |
| I _{CEX} | | V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high | 50 | | | 50 | | | μA |
| I _O § | | V _{CC} = 5.5 V, V _O = 2.5 V | -50 | -100 | -180 | -50 | -100 | -180 | mA |
| I _{CC} | | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | | 6 | | | mA |
| | | | Outputs low | | | 90 | | | |
| | | | Outputs disabled | | | 6 | | | |
| ΔI _{CC} ¶ | | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | 1 | | | 1 | | | mA |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | 3.5 | | | 3.5 | | | pF |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | 11.5 | | | 11.5 | | | pF |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | | SN54ABTH32501 | | SN74ABTH32501 | | UNIT |
|--------------------|-----------------|--------------------|---------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | 0 | 150 | 0 | 150 | MHz |
| t _w | Pulse duration | LE high | 3.5 | | 3.3 | | ns |
| | | CLK high or low | 3.5 | | 3.3 | | |
| t _{su} | Setup time | A or B before CLK↑ | 4.3 | | 3.5 | | ns |
| | | A or B before LE↓ | 2.5 | | 1.6 | | |
| t _h | Hold time | A or B after CLK↑ | 0.2 | | 0 | | ns |
| | | A or B after LE↓ | 1.8 | | 1.6 | | |



SN54ABTH32501, SN74ABTH32501
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

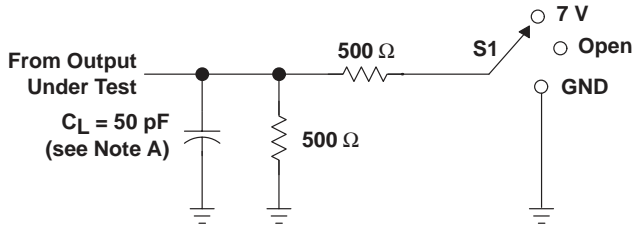
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABTH32501 | | | SN74ABTH32501 | | | UNIT |
|-----------|---------------------------|-------------|---------------|------|-----|---------------|------|-----|------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| f_{max} | | | 150 | | | 150 | | | MHz |
| t_{PLH} | A or B | B or A | 0.5 | 2.9 | 5.2 | 1.3 | 2.9 | 4.8 | ns |
| t_{PHL} | | | 0.5 | 2.7 | 5.8 | 1.4 | 2.7 | 5.4 | |
| t_{PLH} | LEAB or LEBA | A or B | 0.7 | 3.4 | 5.7 | 1.6 | 3.4 | 5.3 | ns |
| t_{PHL} | | | 0.7 | 3.6 | 5.9 | 1.9 | 3.6 | 5.5 | |
| t_{PLH} | CLKAB or CLKBA | A or B | 0.5 | 3.2 | 5.7 | 1.5 | 3.2 | 5.3 | ns |
| t_{PHL} | | | 0.7 | 3.3 | 5.8 | 1.7 | 3.3 | 5.4 | |
| t_{PZH} | OEAB or \overline{OEBA} | A or B | 0.5 | 3.2 | 6.2 | 1.2 | 3.2 | 5.6 | ns |
| t_{PZL} | | | 0.5 | 3.6 | 6.6 | 1.5 | 3.6 | 6 | |
| t_{PHZ} | OEAB or \overline{OEBA} | A or B | 0.7 | 3.6 | 7 | 1.8 | 3.6 | 5.9 | ns |
| t_{PLZ} | | | 0.7 | 3.5 | 6.1 | 1.7 | 3.5 | 5.6 | |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

SN54ABTH32501, SN74ABTH32501
36-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

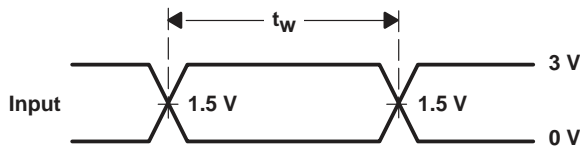
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PARAMETER MEASUREMENT INFORMATION

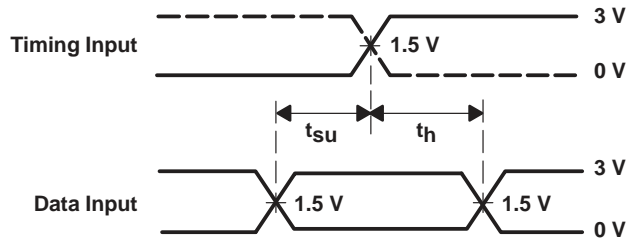


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

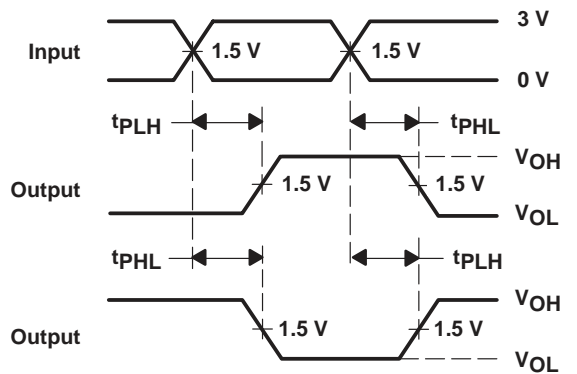
LOAD CIRCUIT



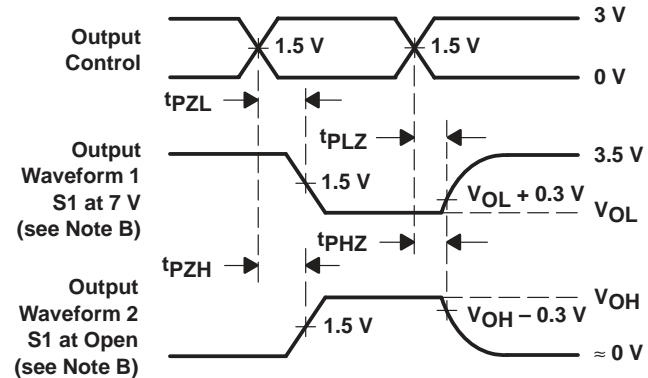
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9557601NXD | OBSOLETE | LQFP | PZ | 100 | | TBD | Call TI | Call TI |
| SN74ABTH32501PZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| SN74ABTH32501PZG4 | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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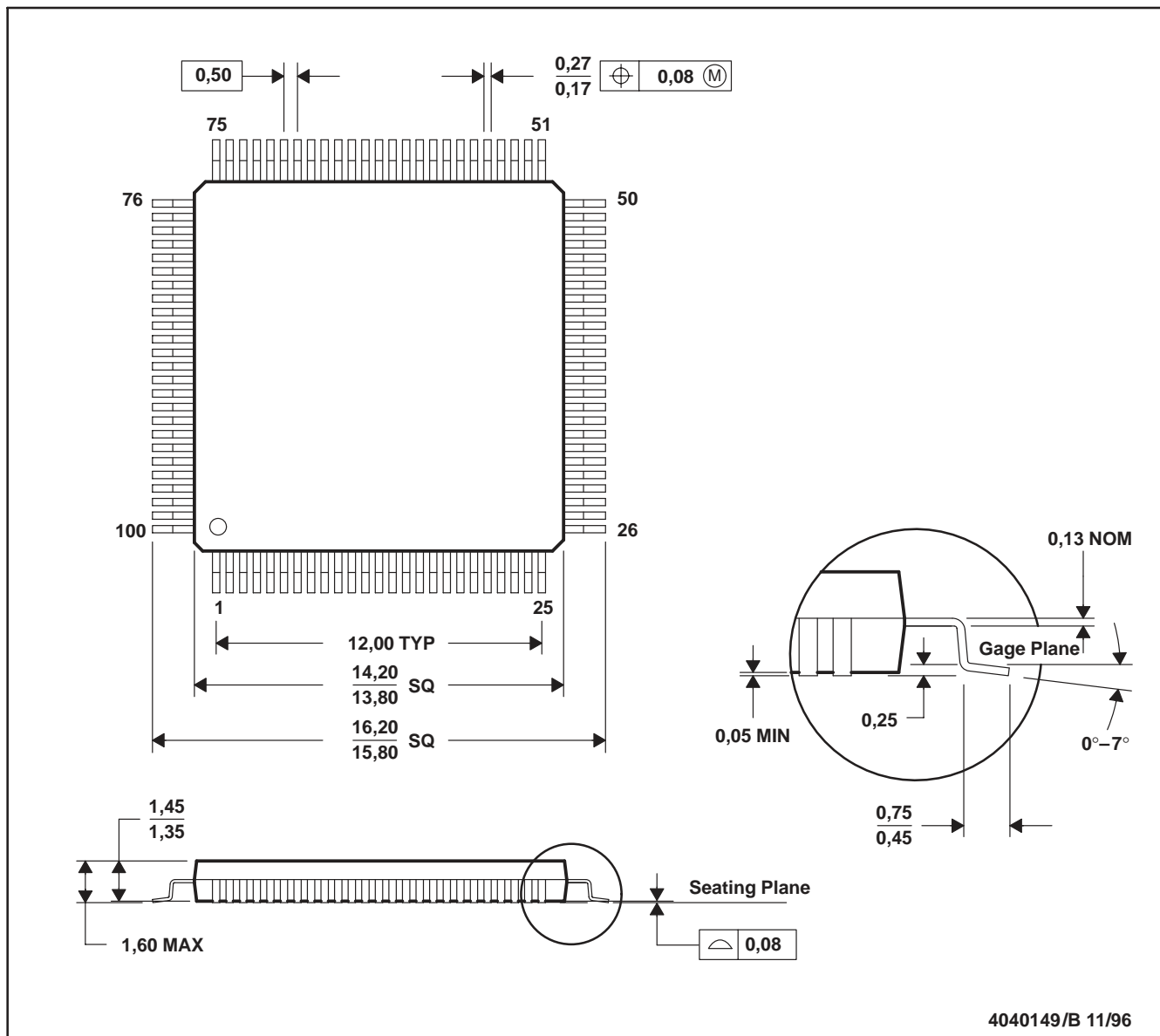
- Enhanced Product: [SN74ABTH32501-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



4040149/B 11/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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