User's Guide
SLUU323–JUNE 2008

# Using theTPS51200 EVM Sink/Source DDR Termination Regulator

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# 1 Introduction

The TPS51200EVM evaluation board, HPA322A is designed to evaluate the performance and characteristics of TI's cost optimized DDR/DDR2/DDR3/LP DDR3 VTT termination regulator, the TPS51200.

## 1.1 Background

The TPS51200 is designed to provide proper termination voltage and a 10-mA buffered reference voltage for DDR memory which covered DDR (2.5 V/1.25 V), DDR2 (1.8 V/0.9 V), DDR3 (1.5 V/0.75 V), LP DDR3 (1.2 V/0.6 V) specifications with a minimum of external components.

# 2 Description

The TPS51200 is designed to provide proper termination voltage and a 10-mA buffered reference voltage for DDR memory which covered DDR (2.5 V/1.25 V), DDR2 (1.8 V/0.9 V), DDR3 (1.5 V/0.75 V), LP DDR3 (1.2 V/0.6 V) specifications with minimal external components

## 2.1 Typical Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, LP DDR3
- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer Set-Top Box

## 2.2 Features

- Input Voltage: Support 2.5V Rail and 3.3V Rail
- VLDOIN, VDDQ Voltage Range: 1.2V-2.5V
- Build-in transient load switches (with both sinking and sourcing capability) to emulate the sink/source transient behavior which helps to evaluate the dynamic performance. For ease of use, both load step and timing of transient can be modified by on board resistors, and current information can also be monitored on board
  - DDR: ±1.67 A Sink/Source Transient Load
  - DDR2: ±1.2 A Sink/Source Transient Load
  - DDR3: ±1.0 A Sink/Source Transient Load
  - LP DDR3: ±0.8 A Sink/Source Transient Load
- Switcher S1 for enable function
- Convenient test points for probing PGOOD, CLK_IN and loop response testing
- 2-layer PCB with all the components on the bottom side

# 3 Electrical Performance Specifications

## 3.1 Performance Specification Summary

**Table 1. TPS51120 Performance Specification Summary**

| SPECIFICATION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range, ($V_{VIN}$) | | 2.4 | 3.3 | 3.5 | V |
| VDDQ voltage range ($V_{VDDQ}$) | | 1.2 | | 2.5 | |
| VLDOIN Voltage range ($V_{VLDOIN}$) | | 1.2 | | 2.5 | |
| **VTT TERMINATION VOLTAGE** | | | | | |
| DDR | VTT | | 1.25 | | V |
| | VTTREF | | 1.25 | | |
| DDR2 | VTT | | 0.9 | | |
| | VTTREF | | 0.9 | | |
| DDR3 | VTT | | 0.75 | | |
| | VTTREF | | 0.75 | | |
| LP DDR3 | VTT | | 0.6 | | |
| | VTTREF | | 0.6 | | |
| VTT termination voltage tolerance | | –25 | | 25 | mV |
| Termination current ($I_{VTT}$) | | –2 | | 2 | A |
| VTTREF voltage tolerance | | –15 | | 15 | mV |
| Reference current ($I_{VTTREF}$) | | –10 | | 10 | mA |
| Sink current limit ($I_{VTT}$) | | 3.5 | | 5.5 | A |
| Source current limit ($I_{VTT}$) | | 3.0 | | 4.5 | |

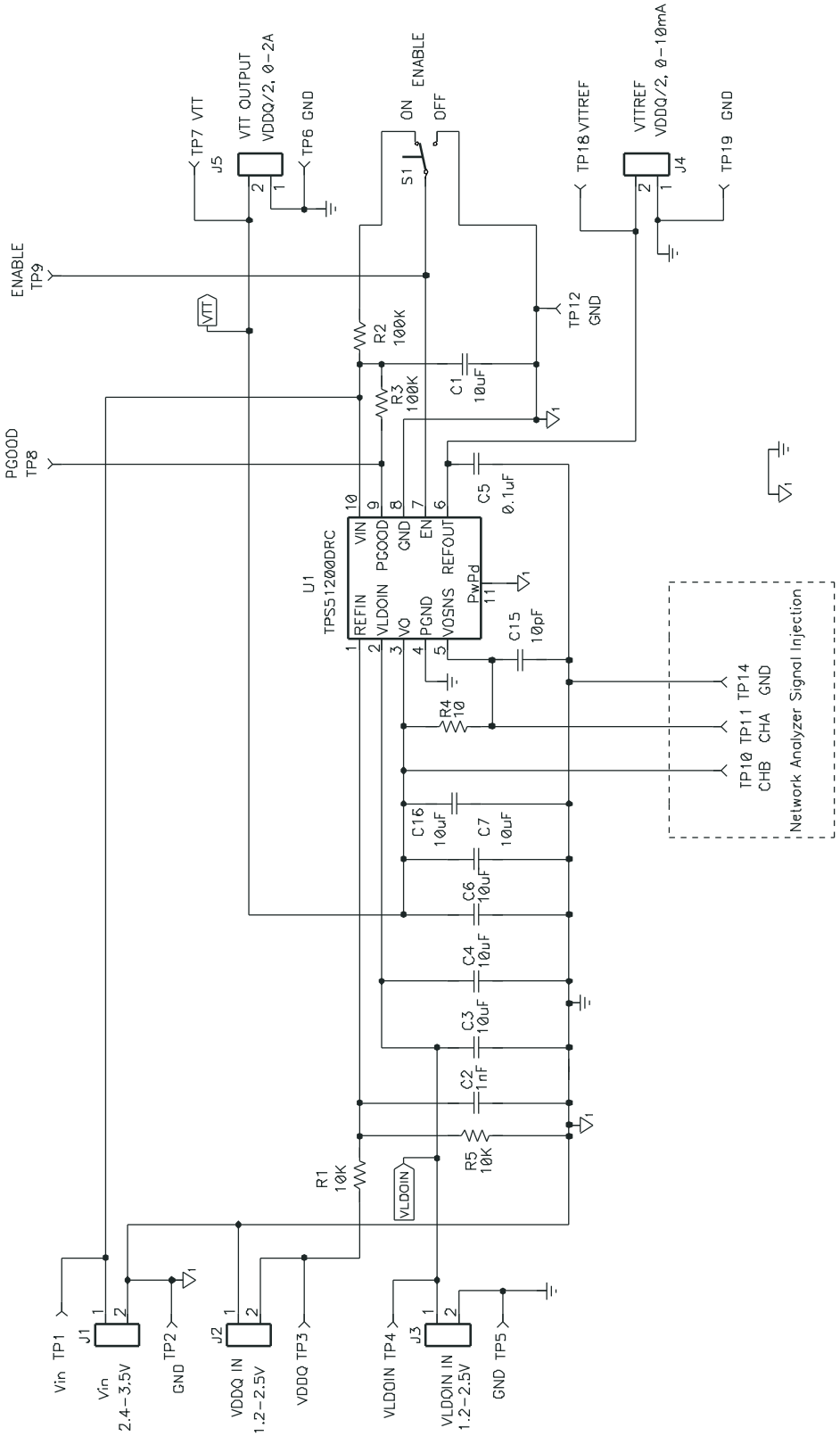



**Figure 1. EVM Schematic**

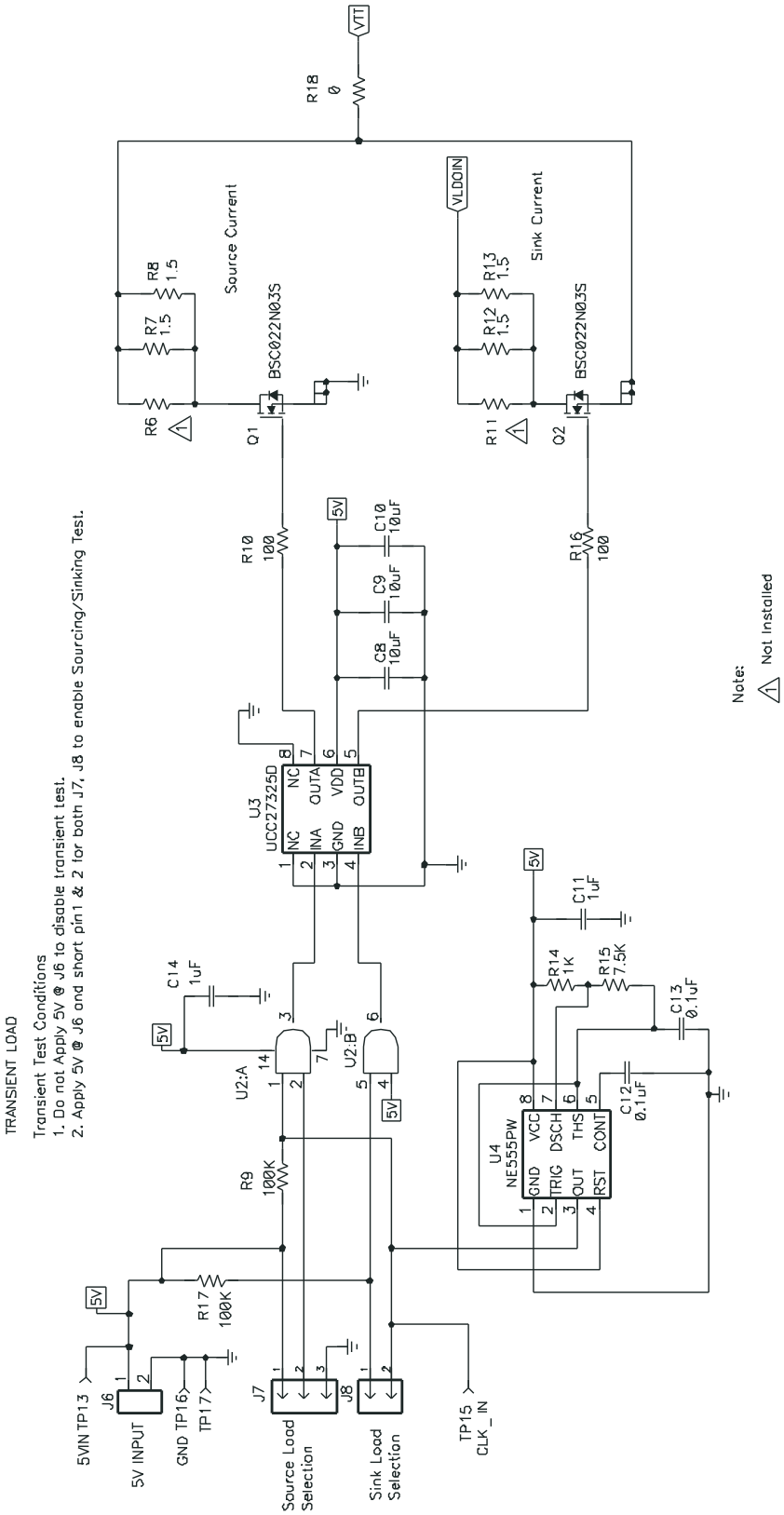



**Figure 2. EVM Schematic**

# 4 Test Setup

This section shows the test setups used and the tests performed in evaluating the EVM. See the TPS51120 data sheet (SLUS670) for complete details regarding the operation and specifications.

## 4.1 Equipment

### 4.1.1 Voltage Source

**Table 2. I/O and Jumper Connections**

| JACK | CONNECTION |
|---|---|
| VIN | The input voltage source 1 should be a 0 V to 10 V variable DC source capable of supplying 1Adc. Connect Vin to J1 as shown in Figure 3. |
| VDDQ | The input voltage source 2 should be a 0 V to 10 V variable DC source capable of supplying 1Adc. Connect VDDQ to J2 as shown in Figure 3. |
| VLDOIN | The input voltage source 3 should be a 0 V to 10 V variable DC source capable of supplying 10Adc. Connect VLDOIN to J3 as shown in Figure 3. |
| 5VINPUT | The input voltage source 4 should be a 0-10V variable DC source capable of supplying 1Adc. Connect 5VINPUT to J6 as shown in Figure 3. |

### 4.1.2 Voltmeters

Voltmeters (0V-10 V) are used to monitor the $V_{IN}$ voltage (V1), VDDQ input voltage (V2), VLDOIN input voltage (V3), VTT output voltage (V4), VTTREF output voltage (V5), 5VIN input (V6) as shown in Figure 3

### 4.1.3 Loads

Load 1 is an electronic load set in constant current mode capable of sinking 0 A to 5 A of current. Load 1 needs to be connected to J5 as shown in Figure 3. Load 2 is recommended to use resistive load around 0.5 W. VTTREF only sink/source maximum 10 mA. Load 2 needs to be connected to J4 as shown in Figure 3.

### 4.1.4 Oscilloscope

An analog or digital oscilloscope can be used to monitor various test points around the EVM. It also can be used to measure VTT transient load regulation.

### 4.1.5 Fan

Some of the components in this EVM can get hot to approach temperatures of 60°C during operating. A small fan capable of between 200 LFM and 400 LFM is recommended to reduce component temperatures while the EVM is operating.

## 4.2 Recommended Test Setup

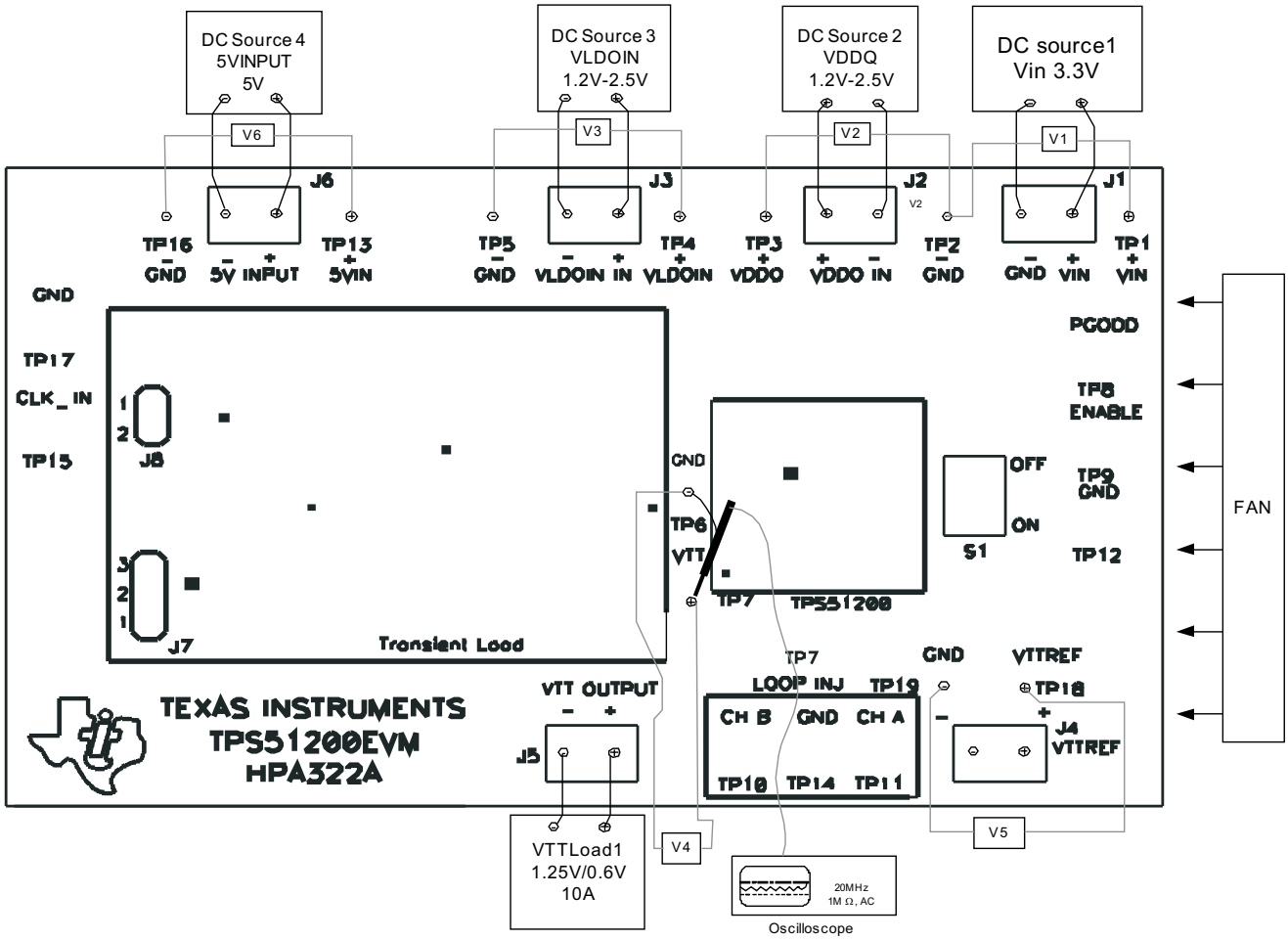



**Figure 3. Recommended Test Setup**

## 4.3 List of Test Points

Table 3 lists the functions of each test point.

**Table 3. Test Points**

| TEST POINTS | NAME | DESCRIPTION |
|---|---|---|
| TP1 | $V_{IN}$+ | 3.3V or 2.5V input |
| TP2 | GND | GND for $V_{IN}$ and VDDQ measurement |
| TP3 | VDDQ | VDDQ input 1.2 V to 2.5 V |
| TP4 | VLDOIN | VLDOIN input 1.2 V to 2.5 V |
| TP5 | GND | GND for VLDOIN measurement |
| TP6 | GND | GND for VTT measurement |
| TP7 | VTT | VTT output |
| TP8 | PGOOD | Monitors power good signal |
| TP9 | ENABLE | Monitors enable signal |
| TP10 | CHB | Input B for loop analysis, See section 6.5 |
| TP11 | CHA | Input A for loop analysis, See section 6.5 |
| TP12 | GND | GND for PGOOD and ENABLE measurement |
| TP13 | 5VIN | 5-V input for transient load |
| TP14 | GND | GND for loop measurement |
| TP15 | CLK_IN | Monitor the load transient timing |
| TP16 | GND | GND for 5VIN measurement |
| TP17 | GND | GND for CLK_IN signal measurement |
| TP18 | VTTREF | VTTREF output |
| TP19 | GND | GND for VTTREF measurement |

## 4.4 Note on Power Up and Power Down

The following steps are guidelines for power up and power down of the EVM. Never walk away from a powered EVM.

### 4.4.1 Workstation

An ESD workstation is recommended. Make sure that an ionizer is on. Any wrist straps, boot straps or mats must connect the user to earth ground before the EVM is removed from the protective packaging and power is applied to it. Electrostatic smock and safety glasses should also be worn.

### 4.4.2 Power Up

1. Prior to connecting the DC input source, limit the source current and then connect the DC source to EVM as shown in Figure 3
   - Set DC source 1 source current limit to 1 A.
   - Set DC source 2 source current limit to 1 A.
   - Set DC source 3 source current limit to 10 A.
   - Set DC source 4 source current limit to 1 A.
2. Connect voltage meter (V1, V2, V3, V4, V5, V6) as shown in Figure 3.
3. For operation with load, connect Load 1 and Load 2 to EVM as shown in Figure 3.
   a. Connect Load 1 to J5 and Load 2 to J4
   b. Set electronic load to constant current mode with initial value of 0 A.
4. Power on the DC source 1.
5. Power on the DC source 2.
6. Power on the DC source 3.

### 4.4.3 Power Down

Power off the DC sources and loads in the following order.

1. Power off DC Source 4.
2. Power off DC Source 3.
3. Power off DC Source2.
4. Power off DC Source 1.
5. Power off Load 1.
6. Power off Load 2.

# 5 Test Procedure

## *5.1 DDR Operation*

### 5.1.1 DDR Source Load Regulation

1. Set Switch S1 to the OFF position.
2. Ensure DC Source 4 is OFF.
3. Increase $V_{IN}$ (DC Source 1) from 0 V to 3.3 V at J1. This is the bias supply required for TPS51200 operation. Using V1, verify $V_{IN}$ voltage is between 3.25 V and 3.35 V.
4. Increase VDDQ (DC Source 2) from 0 V to 2.5 V at J2. This is the reference input. Using V2, verify that the VDDQ voltage is between 2.45 V and 2.55 V.
5. Increase VLDOIN (DC Source 3) from 0 V to 2.5 V at J3. This is the LDO input. Using V3, verify that the VLDOIN voltage is between 2.45 V and 2.55 V. Ensure that this input wires are short and heavy (gauge 14 and lower).
6. Set Switch S1 to the ON position.
7. Set Load 1 to between 0 A to 2 A, Load 2 to between 0 mA to 10 mA.
8. Verify V3 between 2.45 V and 2.55 V. Adjust VLDOIN if necessary.
9. Using V4 and V5 to measure VTT, VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF both should be around 1.25 V
10. Decrease Load 1 to 0 A.
11. Decrease Load 2 to 0 mA.
12. Set Switch S1 to the OFF position.
13. Continue on the test procedure Section 5.1.2.

### 5.1.2 DDR Sink/Source Transient

Perform the following operations in the order shown.

1. Remove Load 1 from J5.
2. Ensure that the two jumpers provided in the EVM to short pin1and pin2 are connected at location J7 and J8.
3. Increase DC Source 4 from 0 V to 5 V at J6. This is the bias supply required for transient load operation. Using V6, verify that the 5VINPUT voltage is between 4.95 V and 5.05 V.
4. Set Switch S1 to the ON position.
5. TPS51200 is now operating at sink (1.67 A) and source (1.67 A) load transient.
6. Verify V3 between 2.45 V and 2.55 V, Adjust VLDOIN if necessary.
7. Using V4 and V5 to measure VTT, VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF each should measure approximately 1.25 V.
8. Use scope probe to monitor VTT load transient regulation. The scope probe should be put at TP7 (+) and TP6 (–) by setting to AC with 20 MHz bandwidth limiting. Use a vertical resolution of 20 mV per division and a horizontal resolution of 200 µs per division. The measurement should ignore high frequency switch transition "spike". Refer to Figure 3 and Figure 9.

9. Set Switch S1 to the OFF position.
10. Decrease DC Source 4 to 0 V.
11. Decrease DC Source 3 to 0 V.
12. Decrease DC Source 2 to 0 V.
13. Decrease DC Source 1 to 0 V.

## 5.2 DDR2 Operation

### 5.2.1 DDR2 Source Load Regulation

1. Set Switch S1 to the OFF position.
2. Ensure DC Source 4 is OFF.
3. Increase $V_{IN}$ (DC Source 1) from 0 V to 3.3 V at J1. This is the bias supply required for TPS51200 operation. Using V1, verify that $V_{IN}$ measures between 3.25 V and 3.35 V.
4. Increase VDDQ (DC Source 2) from 0 V to 1.8 V at J2. This is the reference input. Using V2, verify that the VDDQ voltage is between 1.75 V and 1.85 V.
5. Increase VLDOIN (DC Source 3) from 0V to 1.8V at J3. This is the LDO input. Using V3, verify that the VLDOIN voltage is between 1.75V and 1.85V. Ensure that the input wires are short and heavy (gauge 14 and lower).
6. Set Switch S1 to the ON position.
7. Set Load 1 to between 0 A and 2 A. Set Load 2 to between 0 mA and 10 mA.
8. Verify that V3 is between 1.75 V and 1.85 V, Adjust VLDOIN if necessary.
9. Use V4 and V5 to measure VTT, and VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF both should be around 0.9 V.
10. Decrease Load 1 to 0 A,
11. Decrease Load 2 to 0 mA.
12. Set Switch S1 to the OFF position.
13. Continue on the test procedure Section 5.2.2.

### 5.2.2 DDR2 Sink/Source Transient

1. Remove Load 1 from J5.
2. Ensure two jumpers provided in the EVM to short pin1and pin2 are connected at location J7 and J8.
3. Increase DC Source 4 from 0 V to 5 V at J6. This is the bias supply required for transient load operation. Using V6, verify that the 5VINPUT is between 4.95 V and 5.05 V.
4. Set Switch S1 to the ON position.
5. TPS51200 is now operating at sink (1.2 A) and source (1.2 A) load transient.
6. Verify V3 between 1.75 V and 1.85 V, Adjust VLDOIN if necessary.
7. Using V4 and V5 to measure VTT, VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF each should measure approximately 0.9 V.
8. Use scope probe to monitor VTT load transient regulation. The scope probe should be put at TP7 (+) and TP6 (–) by setting to AC with 20 MHz bandwidth limiting. Use a vertical resolution of 20 mV per division and a horizontal resolution of 200 μs per division. Use horizontal cursor to measure transient load regulation. The measurement should ignore high frequency switch transition “spike”. Refer to Figure 3 and Figure 9.
9. Set Switch S1 to the OFF position.
10. Decrease DC Source 4 to 0 V.
11. Decrease DC Source 3 to 0 V.
12. Decrease DC Source 2 to 0 V.
13. Decrease DC Source 1 to 0 V.

## 5.3 DDR3 Operation

### 5.3.1 DDR3 Source Load Regulation

1. Set Switch S1 to the OFF position.
2. Ensure DC Source 4 is OFF.
3. Increase $V_{IN}$ (DC Source 1) from 0 V to 3.3 V at J1. This is the bias supply required for TPS51200 operation. Using V1, verify that $V_{IN}$ is between 3.25 V and 3.35 V.
4. Increase VDDQ (DC Source 2) from 0 V to 1.5 V at J2. This is the reference input. Using V2, verify that the VDDQ voltage is between 1.45 V and 1.55V.
5. Increase VLDOIN (DC Source 3) from 0 V to 1.5 V at J3. This is the LDO input. Using V3, verify that the VLDOIN voltage is between 1.45 V and 1.55 V. Ensure that the input wires are short and heavy (gauge 14 and lower).
6. Set Switch S1 to the ON position.
7. Set Load 1 to between 0 A to 2 A Set Load 2 to between 0 mA and 10 mA.
8. Verify that V3 is between 1.45 V and 1.55 V. Adjust VLDOIN if necessary.
9. Use V4 and V5 to measure the VTT and VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF both should be approximately 0.75 V.
10. Decrease Load 1 to 0 A.
11. Decrease Load 2 to 0 mA.
12. Set Switch S1 to the OFF position.
13. Continue on the test procedure Section 5.3.2.

### 5.3.2 DDR3 Sink/Source Transient

1. Remove Load 1 from J5.
2. Ensure that the two jumpers provided in the EVM to short pin1and pin2 are connected at location J7 and J8.
3. Increase DC Source 4 from 0 V to 5 V at J6. This is the bias supply required for transient load operation. Using V6, verify that the 5VINPUT is between 4.95 V and 5.05 V.
4. Set Switch S1 to the ON position.
5. The TPS51200 is now operating at sink (1.0A) and source (1.0A) load transient.
6. Verify that V3 is between 1.45 V and 1.55 V. Adjust VLDOIN if necessary.
7. Use V4 and V5 to measure the VTT and VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF should each measure approximately 0.75 V.
8. Use a scope probe to monitor the VTT load transient regulation. The scope probe should be put at TP7 (+) and TP6(–) by setting to AC with 20 MHz bandwidth limiting. Use a vertical resolution of 20 mV per division and a horizontal resolution of 200 μs per division. Use the horizontal cursor to measure transient load regulation. The measurement should ignore high-frequency switch transition spikes. Refer to Figure 3 and the Figure 9.
9. Set Switch S1 to the OFF position.
10. Decrease DC source 4 to 0 V.
11. Decrease DC source 3 to 0 V.
12. Decrease DC source 2 to 0 V.
13. Decrease DC source 1 to 0 V.

## 5.4 LP DDR3 Operation

### 5.4.1 LP DDR3 Source Load Regulation

1. Set Switch S1 to the OFF position.
2. Ensure that the DC Source 4 is OFF.
3. Increase $V_{IN}$ (DC Source 1) from 0 V to 3.3 V at J1. This is the bias supply required for TPS51200 operation. Using V1, verify that the $V_{IN}$ voltage is between 3.25 V and 3.35 V.
4. Increase VDDQ (DC Source 2) from 0 V to 1.2 V at J2. This is the reference input. Use V2 to verify that the VDDQ voltage is between 1.15 V and 1.25 V.
5. Increase VLDOIN (DC Source 3) from 0 V to 1.2 V at J3. This is the LDO input. Use V3 to verify that the VLDOIN voltage is between 1.15 V and 1.25 V. Ensure that the input wires are short and heavy (gauge 14 and lower).
6. Set Switch S1 to the ON.
7. Set Load 1 to between 0 A and 2 A. Increase Load 2 to between 0 mA and 10 mA.
8. Verify V3 is between 1.15 V and 1.25 V. Adjust VLDOIN if necessary.
9. Use V4 and V5 to measure the VTT and VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF should each measure approximately 0.6 V
10. Decrease Load 1 to 0 A.
11. Decrease Load 2 to 0 mA.
12. Set Switch S1 to the OFF position.
13. Continue on to test procedure Section 5.4.2

### 5.4.2 LP DDR3 Sink/Source Transient

1. Remove Load 1 from J5.
2. Ensure that the two jumpers provided in the EVM to short pin1and pin2 are connected at location J7 and J8.
3. Increase DC Source 4 from 0 V to 5 V at J6. This is the bias supply required for transient load operation. Use V6 to verify that the 5VINPUT is between 4.95 V and 5.05 V.
4. Set Switch S1 to the ON position.
5. TPS51200 is now operating at sink (0.8 A) and source (0.8 A) load transient.
6. Verify that V3 is between 1.15 V and 1.25 V. Adjust VLDOIN if necessary.
7. Use V4 and V5 to measure the VTT and VTTREF voltage. V4 uses for VTT at TP7 (+) and TP6 (–). V5 uses for VTTREF at TP18 (+) and TP19 (–). VTT and VTTREF should each measure approximately 0.6 V.
8. Use a scope probe to monitor the VTT load transient regulation. The scope probe should be inserted at TP7 (+) and TP6(–) by setting to AC with 20 MHz bandwidth limiting. Use a vertical resolution of 20 mV per division and a horizontal resolution of 200 μs per division . Use horizontal cursor to measure transient load regulation. The measurement should ignore high-frequency switch transition spikes. Refer to Figure 3 and Figure 9.
9. Set Switch S1 to the OFF position.
10. Decrease DC source 4 to 0 V.
11. Decrease DC source 3 to 0 V.
12. Decrease DC source 2 to 0 V.
13. Decrease DC source 1 to 0 V.

## 5.5 Loop Measurement (TP10, TP11 and TP14)

TPS51200EVM contains a 10-Ω series resistor in the feedback loop. The control loop measurement set up as shown in Figure 4.

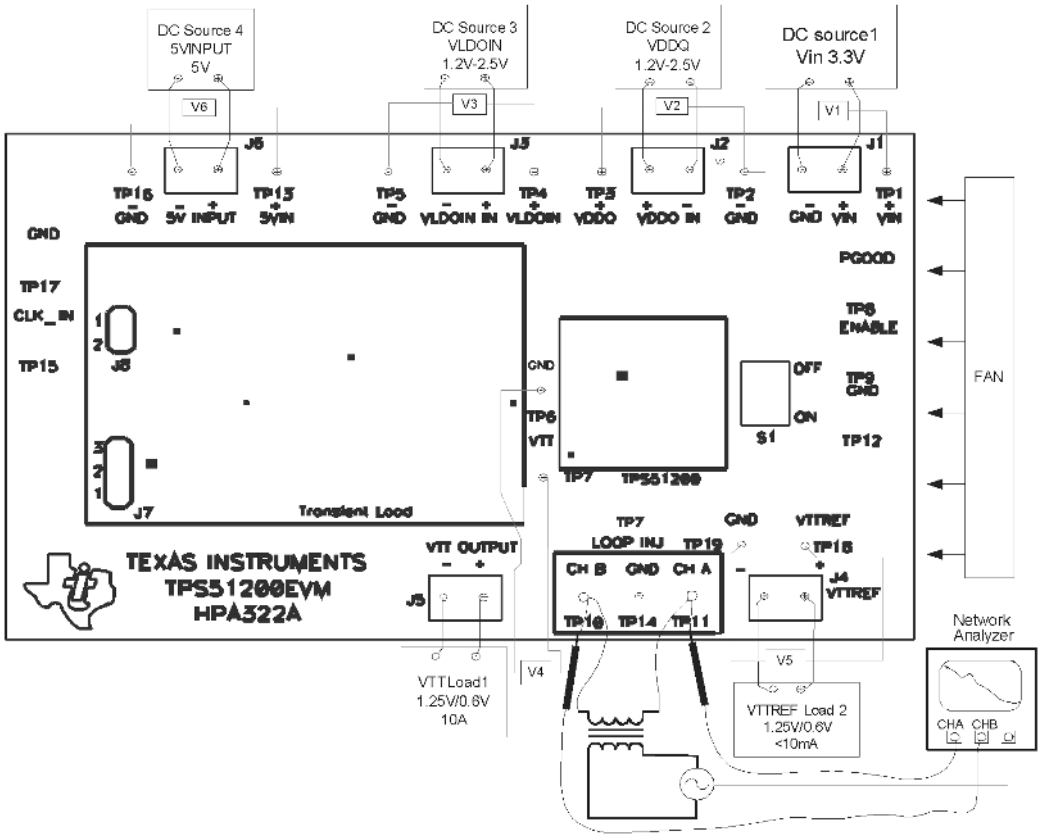



**Figure 4. Control Loop Measurement Setup**

### 5.5.1 Control Loop Measurement Process

1. Set up EVM as shown in Figure 4.
2. Follow test procedure at Step 1 through Step 9 of 5.1.1(DDR), 5.2.1 (DDR2), 5.3.1 (DDR3) or 5.4.1 (LP DDR3) to select the desired application and load condition.
3. Connect Input Signal Amplitude Measurement Probe (Channel A) to TP11.
4. Connect Output Signal Amplitude Measurement Probe (Channel B) to TP10.
5. Connect Ground Lead of Channel A and Channel B to TP14.
6. Inject approximately 100 mV or less signal through an isolation transformer.
7. Sweep frequency from 1 kHz to 10 MHz with a 10-Hz or lower post filter.
8. Measure the control loop gain margin and phase margin. (Refer to Bode plot Figure 10 in Section 6.)
9. Disconnect isolation transformer, probe Channel A and Channel B before making other measurements.
10. Decrease Load 1 to 0 A.
11. Decrease Load 2 to 0 mA.
12. Set switch S1 to the OFF position.
13. Decrease DC Source 3 to 0 V.
14. Decrease DC Source 2 to 0 V.
15. Decrease DC Source 1 to 0 V.

## 6 Performance Data and Typical Characteristic Curves

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

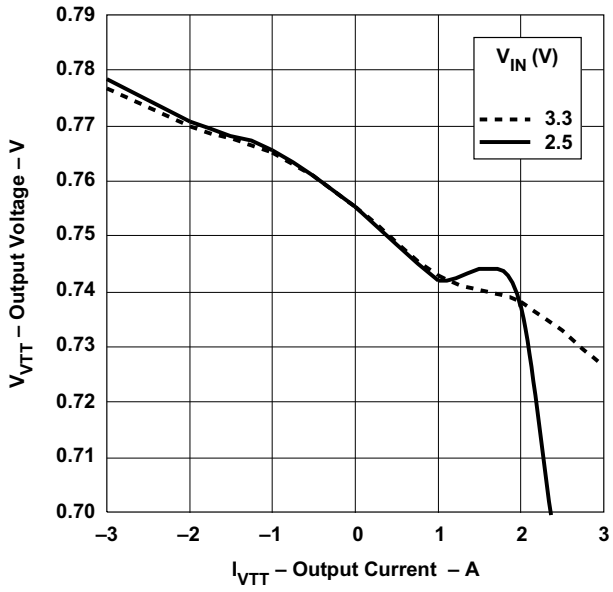



**Figure 5. DDR3 VTT Sink/Source Load Regulation**

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

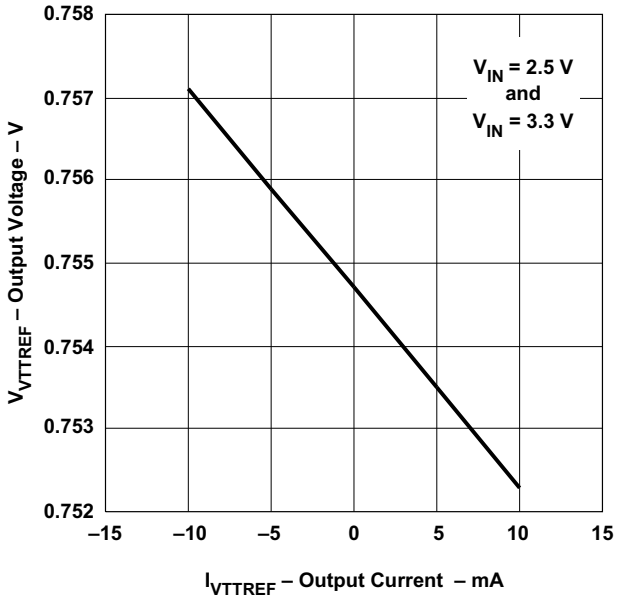
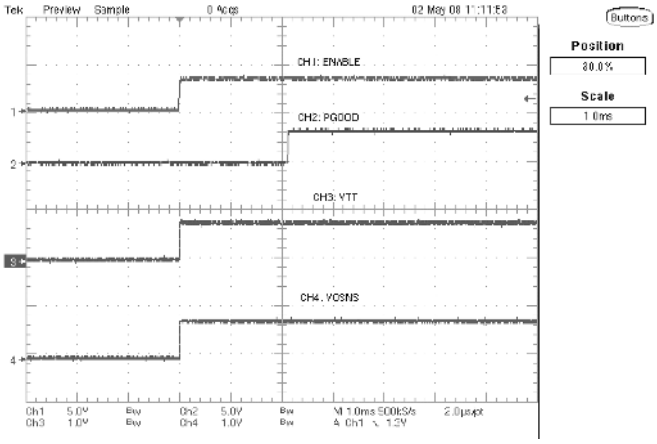
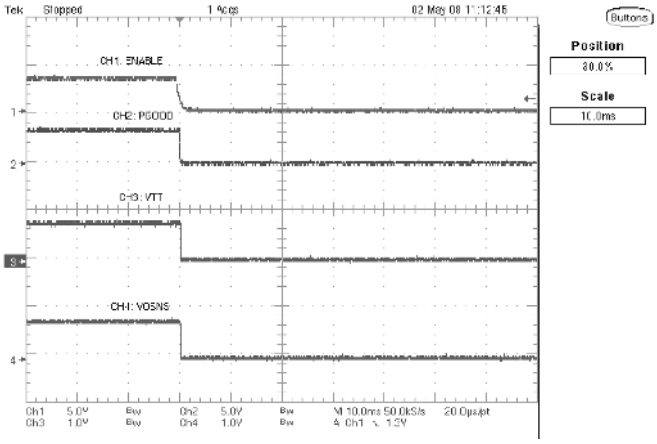



**Figure 6. DDR3 VTTREF Sink/Source Load Regulation**



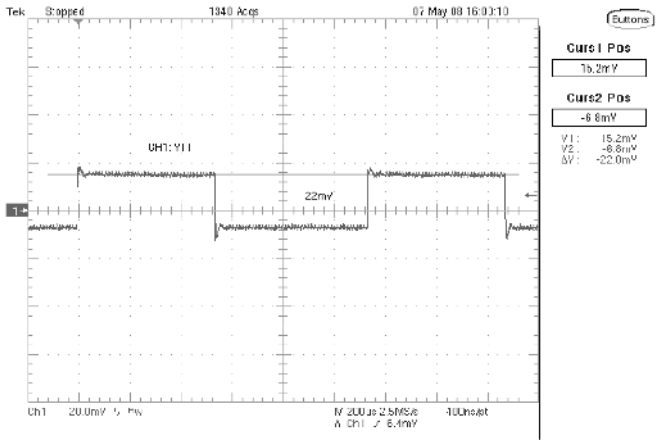

A Test Condition: VTT Source 1 A, Set Enable Switch S1 to the ON position Test Points: CH1: Enable TP9 (+) and TP12 (–), CH2: PGOOD TP8 (+) and TP12 (–), CH3: VTT TP7 (+) and TP6 (–),CH4: VOSNS TPS11 (+) and TP14 (–)

**Figure 7. VTT Source 1 A, Enable Start Up**



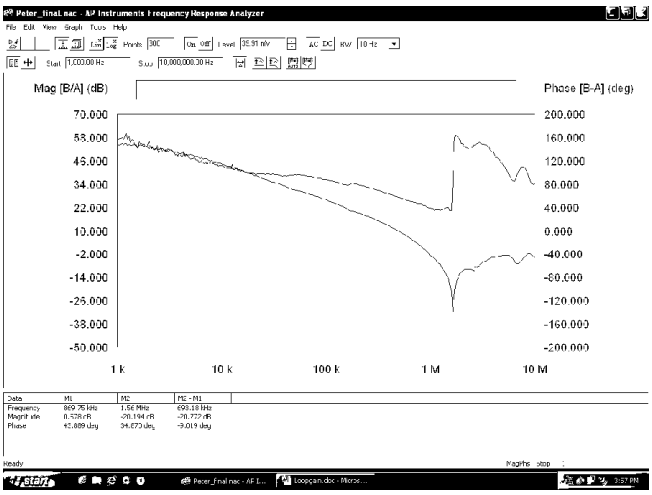

A Test Condition: VTT Source 1 A, Set Enable Switch S1 to the OFF position Test Points: CH1: Enable TP9 (+) and TP12 (–), CH2: PGOOD TP8 (+) and TP12 (–) CH3: VTT TP7 (+) and TP6 (–), CH4: VOSNS TPS11 (+) and TP14 (–)

**Figure 8. VTT Source 1 A, Enable Shutdown**




A Test condition: VTT Sink/Source 1 A, VTT transient load regulation: 22 mV, Test point: VTT TP7 (+) and TP6 (–)

**Figure 9. DDR3 VTT Sink/Source Transient**




A Test Condition: $V_{VIN}$=3.3 V, $V_{VDDQ}$=$V_{VLDOIN}$=1.5 V, $V_{VTT}$=$V_{VTTREF}$=0.75 V, $I_{VTT}$=1 A
Source Test Results: Phase margin: 43.8°, Gain margin: 20.19 dB, Crossover frequency: 869.75 kHz

**Figure 10. Bode Plot for DDR3 Application**

## 7 EVM Assembly

The following figures (Figure 11 through Figure 14) show the design of the TPS51200EVM printed circuit board. The EVM has been designed using 2-Layer, 2-oz. copper-clad circuit board containing all components on the bottom side.

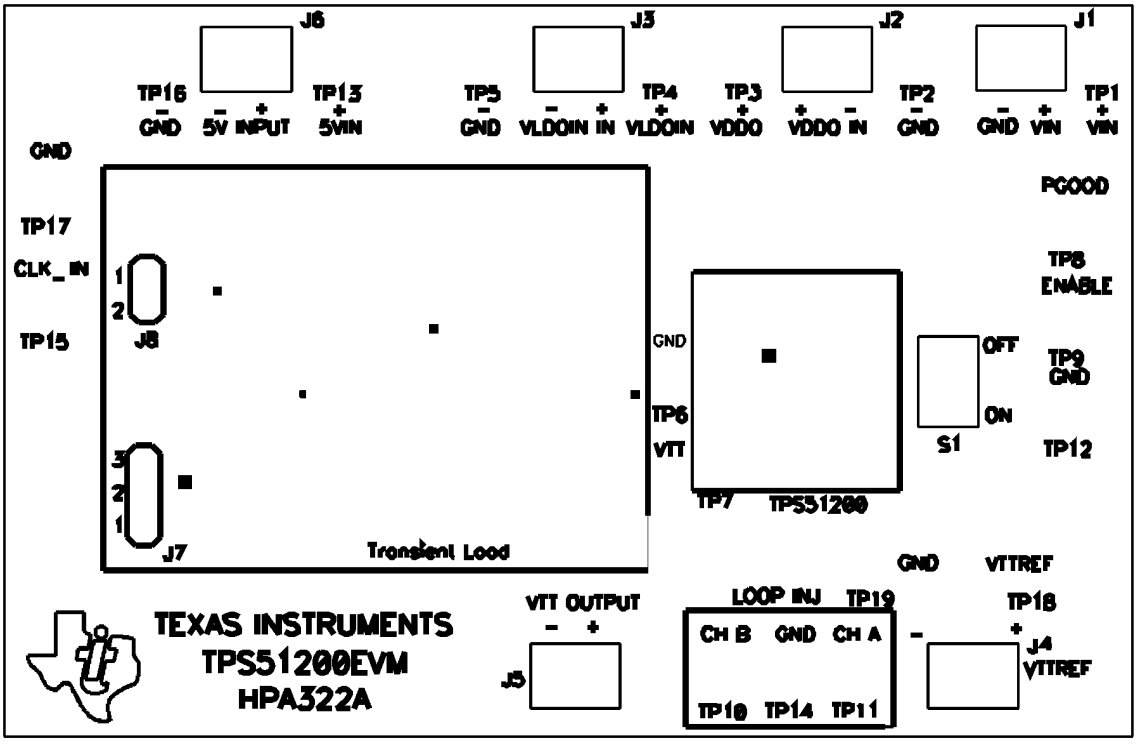



**Figure 11. Bottom Side Silkscreen (Top View)**

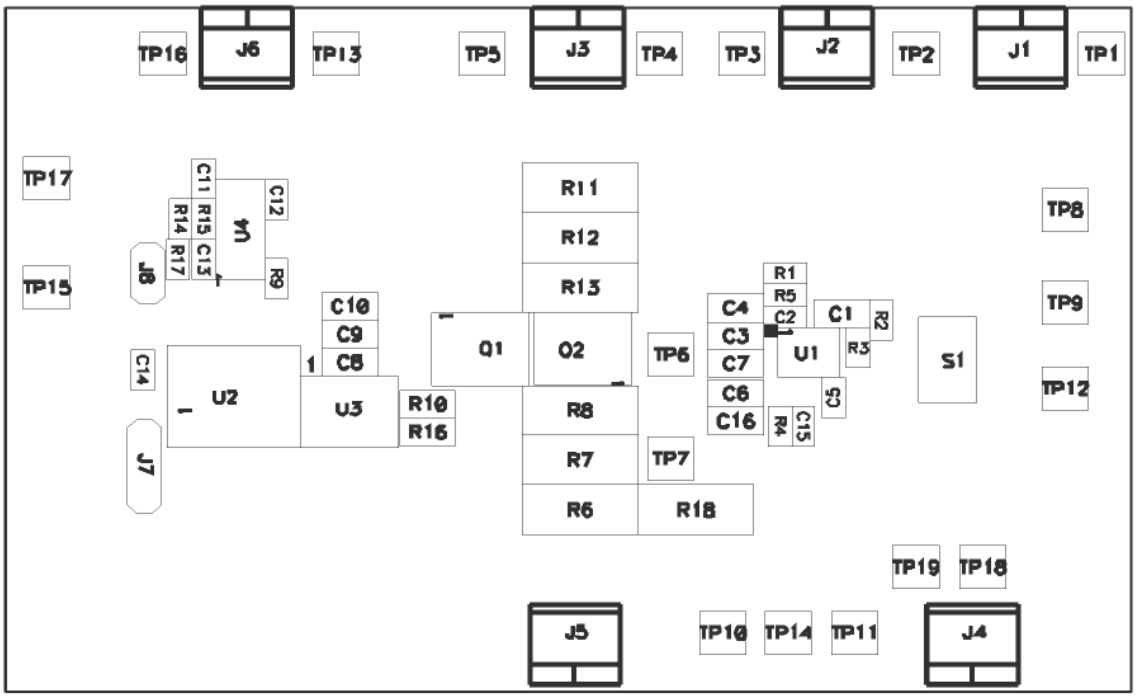



**Figure 12. Bottom Side Assembly**

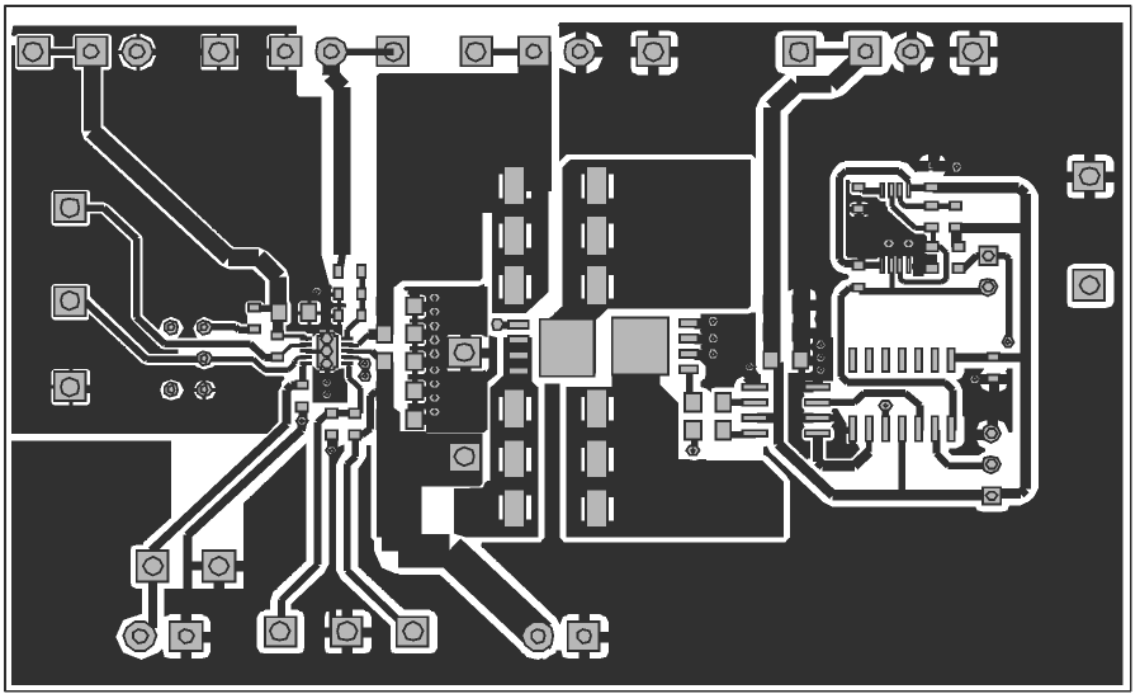


**Figure 13. Bottom Side Copper**

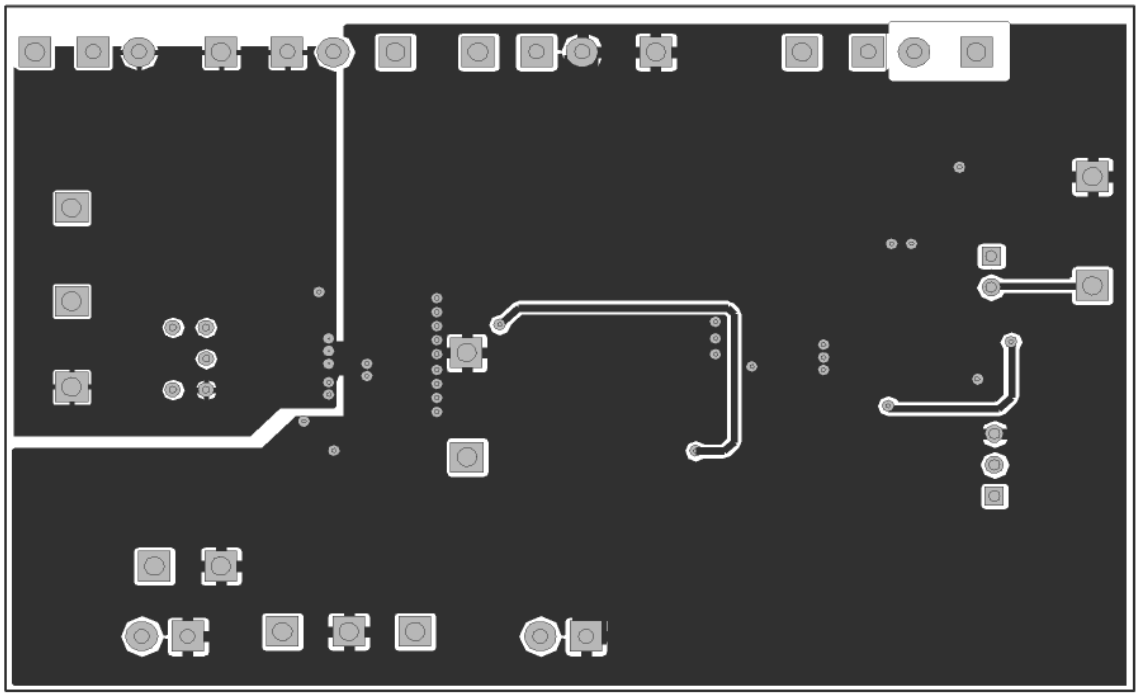


**Figure 14. Top Side Copper**

# 8 List of Materials

Table 4 lists the materials required for the TPS51120EVM.

**Table 4. List of Materials**

| QYT | REFERENCE DESIGNATOR | VALUE | DESCRIPTION | SIZE | PART NUMBER | MFR |
|---|---|---|---|---|---|---|
| 9 | C1, C3, C4, C6, C7, C8, C9, C10, C16 | 10 µF | Capacitor, Ceramic, 10 V, X7R, ±10% | 0805 | Std | Std |
| 2 | C11, C14 | 1 µF | Capacitor, Ceramic, 10 V, X5R,±10% | 0603 | Std | Std |
| 1 | C15 | 10 pF | Capacitor, Ceramic, 50 V, COG, ±5% | 0603 | Std | Std |
| 1 | C2 | 1 nF | Capacitor, Ceramic, 50V, X7R, ±10% | 0603 | Std | Std |
| 3 | C5, C12, C13 | 0.1 µF | Capacitor, Ceramic, 16V, X7R, ±10% | 0603 | Std | Std |
| 6 | J1, J2, J3, J4, J5, J6 | | Terminal Block, 2-pin, 6 A, 3.5 mm | 0.27" × 0.25" | ED555/2DS | OST |
| 1 | J7 | | Header, Male 3-pin, 100 mil spacing, (36-pin strip) | 0.100" x 3" | PTC36SAAN | Sullins |
| 1 | J8 | | Header, Male 2-pin, 100 mil spacing, (36-pin strip) | 0.100" x 2" | PTC36SAAN | Sullins |
| 2 | Q1, Q2 | | MOSFET, N-channel, 30 V, 50 A, 2.2 mΩ | TDSON-8 | BSC022N03S | Infineon |
| 2 | R1, R5 | 10 kΩ | Resistor, Chip, 1/10W, 5% | 0603 | Std | Std |
| 2 | R10, R16 | 100 Ω | Resistor, Chip, 1/8W, 1% | 0805 | Std | Std |
| 1 | R14 | 1 kΩ | Resistor, Chip, 1/10W, 5% | 0603 | Std | Std |
| 1 | R15 | 7.5 kΩ | Resistor, Chip, 1/10W, 5% | 0603 | Std | Std |
| 1 | R18 | 0 | Resistor, Chip, 1W, 5% | 2512 | CRCW25120000Z0EG | Vishay |
| 4 | R2, R3, R9, R17 | 100 kΩ | Resistor, Chip, 1/10W, 5% | 0603 | Std | Std |
| 1 | R4 | 10 Ω | Resistor, Chip, 1/10W, 5% | 0603 | Std | Std |
| 4 | R7, R8, R12, R13 | 1.5 Ω | Resistor, Chip, 1W, 5% | 2512 | CRCW25121R50JNEG | Vishay |
| 1 | S1 | | Switch on-on Mini Toggle | 0.28 x 0.18" | G12AP-RO | NKK |
| 6 | TP1, TP3, TP4, TP7, TP13, TP18 | | Test point, red, thru-hole | 0.125" x 0.125" | 5010 | Keystone |
| 8 | TP2, TP5, TP6, TP12, TP14, TP16, TP17, TP19 | | Test point, black, thru-hole | 0.125" x 0.125" | 5011 | Keystone |
| 5 | TP8, TP9, TP10, TP11, TP15 | | Test point, white, thru-hole | 0.125" x 0.125" | 5012 | Keystone |
| 1 | U1 | | IC, Sink/Source DDR Termination Regulator | DRC | TPS51200DRC | TI |
| 1 | U2 | | IC, QUAD, 2-input positive NAND gates | SO-14 | SN74AHCT00D | TI |
| 1 | U3 | | IC, Dual 4-A High Speed low-side power MOSFET drivers | SO-8 | UCC27325D | TI |
| 1 | U4 | | IC, Precision Timer | TSSOP-8 | NE555PW | TI |
| 0 | R6,R12 | | Not installed | | | |
| 1 | | | Printed circuit board | 3.4" × 2.2" x 0.0625" | HPA322 | Any |
| 4 | Bumpon | | Rubber bumper bumpon, transparent | 0.44" × 0.2" | SJ5303 | 3M |
| 2 | Jumper | | lack | 0.100" | 2-382811-1 | Tyco/AMP |

# 9 References

*Integrated LDO With Switch-Over Circuit for Notebook Computers* data sheet (SLUS808).

*Using the TPS51103EVM, Integrated 3.3V/5V Power LDO with Clock Output* data sheet (SLUU303).

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of VREG + 0.5 V to 5.2 V and the output voltage range of 0 V to 4.2 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70C. The EVM is designed to operate properly with certain components above 70C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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