MIC23158/9

3 MHz PWM Dual 2A Buck Regulator with HyperLight Load and Power Good

Features

- 2.7V to 5.5V Input Voltage
- Adjustable Output Voltage (Down to 1.0V)
- Two Independent 2A Outputs
- Up to 94% Peak Efficiency
- 83% Typical Efficiency at 1 mA
- Two Independent Power Good Indicators
- Independent Programmable Soft-Start
- 45 µA Typical Quiescent Current
- 3 MHz PWM Operation in Continuous Conduction Mode
- Ultra-Fast Transient Response
- Fully Integrated MOSFET Switches
- Output Pre-Bias Safe
- 0.1 µA Shutdown Current
- Thermal-Shutdown and Current-Limit Protection
- 20-Pin 3 mm x 4 mm QFN Package
- Internal 225Ω Pull-Down Circuit on Output (MIC23159)
- –40°C to +125°C Junction Temperature Range

Applications

- Solid State Drives (SSD)
- Smartphones
- Tablet PCs
- Mobile Handsets
- Portable Devices (PMP, PND, UMPC, GPS)
- WiFi/WiMax/WiBro Applications

General Description

The MIC23158/9 is a high efficiency, 3 MHz, dual, 2A synchronous buck regulator with HyperLight Load® mode, power good output indicator, and programmable soft start.

The MIC23159 also provides an auto-discharge feature that switches in a 225Ω pull-down circuit on its output to discharge the output capacitor when disabled. HyperLight Load provides very high efficiency at light loads and ultra-fast transient response which makes the MIC23158/9 perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The 20-pin 3 mm x 4 mm QFN package saves precious board space and requires seven external components for each channel.

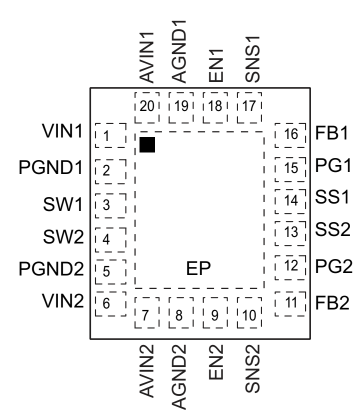
The MIC23158/9 is designed for use with a very small inductor, down to 0.47 µH, and an output capacitor as small as 2.2 µF that enables a total solution size, less than 1 mm in height.

The MIC23158/9 has a very low quiescent current of 45 µA and achieves a peak efficiency of 94% in continuous conduction mode. In discontinuous conduction mode, the MIC23158/9 can achieve 83% efficiency at 1 mA.

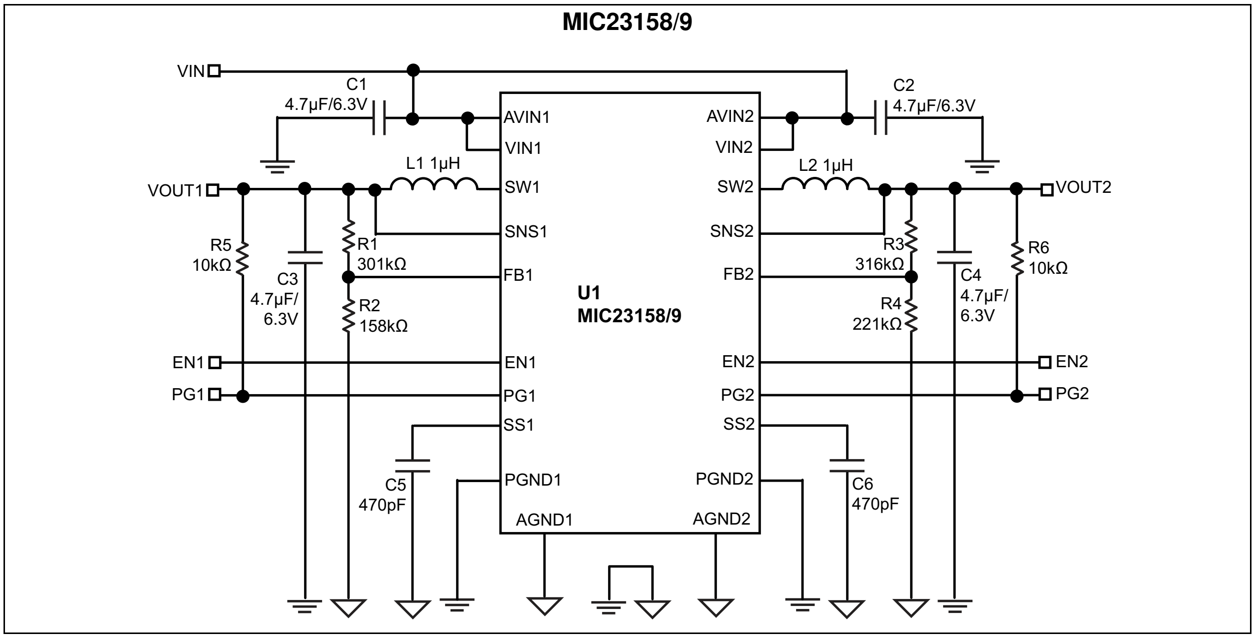
The MIC23158/9 is available in a 20-pin 3 mm x 4 mm QFN package with an operating junction temperature range from –40°C to +125°C.

Package Type

MIC23158/9
20-Lead QFN (ML)
(Top View)

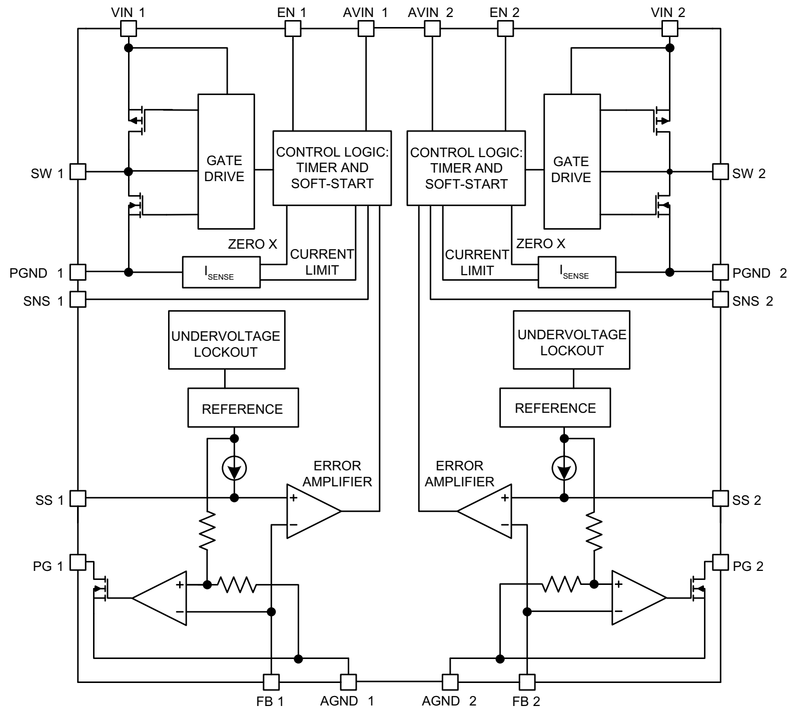


Typical Application Circuit

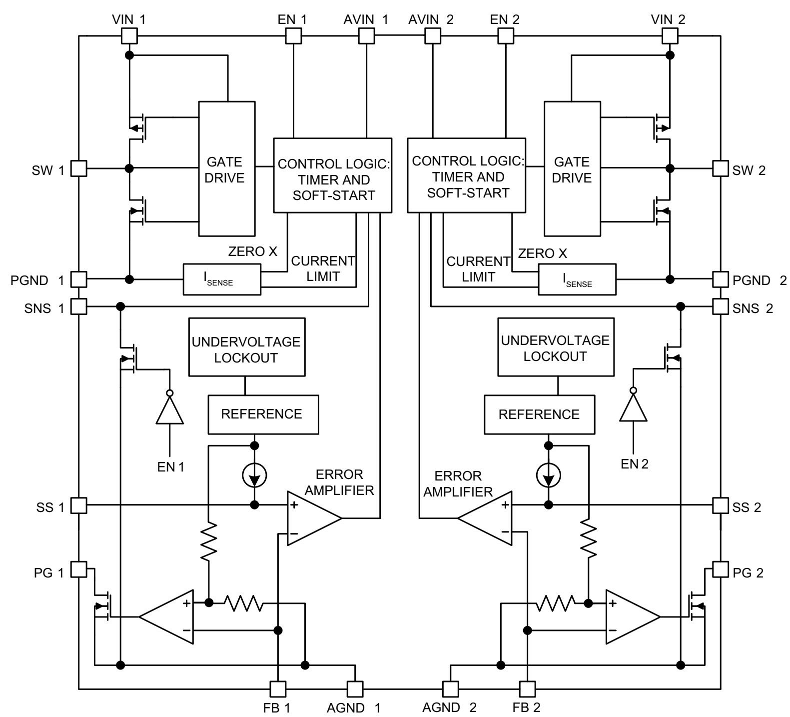


Functional Block Diagrams

Simplified MIC23158 Functional Block Diagram - Adjustable Output Voltage



Simplified MIC23159 Functional Block Diagram - Adjustable Output Voltage



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (AV_{IN1}, AV_{IN2}, V_{IN1}, V_{IN2}) ....–0.3V to +6V
Switch1 (V_{SW1}), Sense1 (V_{SNS1}) ....–0.3V to V_{IN1}
Enable 1 (V_{EN1}), Power Good (V_{PG1}) ....–0.3V to V_{IN1}
Feedback1 (V_{FB1}) ....–0.3V to V_{IN1}
Switch2 (V_{SW2}), Sense2 (V_{SNS2}) ....–0.3V to V_{IN2}
Enable2 (V_{EN2}), Power Good2 (V_{PG2}) ....–0.3V to V_{IN2}
Feedback2 (V_{FB2}) ....–0.3V to V_{IN2}
Power Dissipation (T_A = 70°C)....................Internally Limited
ESD Rating (Note 1)....................ESD Sensitive

Operating Ratings ‡

Supply Voltage (AV_{IN1}, V_{IN1}) ....+2.7V to +5.5V
Supply Voltage (AV_{IN2}, V_{IN2}) ....+2.7V to +5.5V
Enable Input Voltage (V_{EN1}, V_{EN2})....................0V to $V_{IN1,2}$
Output Voltage Range (V_{SNS1}, V_{SNS2})....................+1.0V to +3.3V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C; $AV_{IN1,2}$ = $V_{IN1,2}$ = $V_{EN1,2}$ = 3.6V; L1,2 = 1.0 µH; COUT3,4 = 4.7 µF unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range		**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold		**2.45**	2.55	**2.65**	V	Rising
Undervoltage Lockout Hysteresis		—	75	—	mV	—
Quiescent Current		—	45	**90**	µA	I_{OUT} = 0 mA, SNS > 1.2 * V_{OUTNOM} (both outputs)
Shutdown Current	I_{SHDN}	—	0.1	**5**	µA	V_{EN} = 0V; V_{IN} = 5.5V (per output)
Feedback Regulation Voltage	V_{FB}	**0.6045**	0.62	**0.6355**	V	I_{OUT} = 20 mA
Feedback Bias Current	I_{FB}	—	0.01	—	µA	Per output
Current Limit	I_{LIM}	**2.2**	4.3	—	A	SNS = 0.9 * V_{OUTNOM}
Output Voltage Line Regulation		—	0.45	—	%/V	V_{IN} = 3.6V to 5.5V if V_{OUTNOM} < 2.5V, I_{OUT} = 20 mA
		—	0.45	—		V_{IN} = 4.5V to 5.5V if V_{OUTNOM} ≥ 2.5V, I_{OUT} = 20 mA
Output Voltage Load Regulation		—	0.55	—	%	DCM, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V
		—	1.0	—		DCM, V_{IN} = 5.0V if V_{OUTNOM} ≥ 2.5V
		—	0.8	—		CCM, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V
		—	0.8	—		CCM, V_{IN} = 5.0V if V_{OUTNOM} ≥ 2.5V

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C; $AV_{IN1,2}$ = $V_{IN1,2}$ = $V_{EN1,2}$ = 3.6V; L1,2 = 1.0 µH; COUT3,4 = 4.7 µF unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
PWM Switch $R_{DS(ON)}$		—	0.20	—	Ω	$I_{SW1,2}$ = 100 mA PMOS
		—	0.19	—		$I_{SW1,2}$ = –100 mA NMOS
Switching Frequency	f_{SW}	—	3	—	MHz	I_{OUT} = 180 mA
Soft-Start Time	t_{SS}	—	300	—	µs	V_{OUT} = 90%, C_{SS} = 470 pF
Soft-Start Current	I_{SS}	—	2.7	—	µA	V_{SS} = 0V
Power Good Threshold		86	92	96	%	Rising
Power Good Threshold Hysteresis		—	7	—	%	—
Power Good Delay Time		—	68	—	µs	Rising
Power Good Pull-Down Resistance		—	95	—	Ω	—
Enable Input Voltage		—	—	**0.4**	V	Logic low
		1.2	—	—		Logic high
Enable Input Current		—	0.1	**2**	µA	—
Output Discharge Resistance		—	225	—	Ω	MIC23159 Only; EN = 0V, I_{OUT} = 250 µA
Overtemperature Shutdown		—	160	—	°C	—
Shutdown Hysteresis		—	20	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance 3 mm x 4 mm QFN-20	θ_{JA}	—	53	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

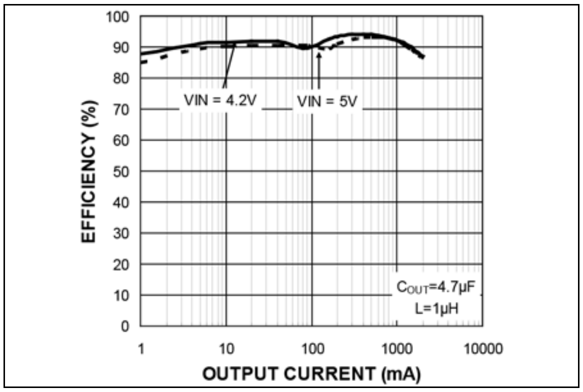


FIGURE 2-1: *Efficiency (V_{OUT} = 3.3V) vs. Output Current.*

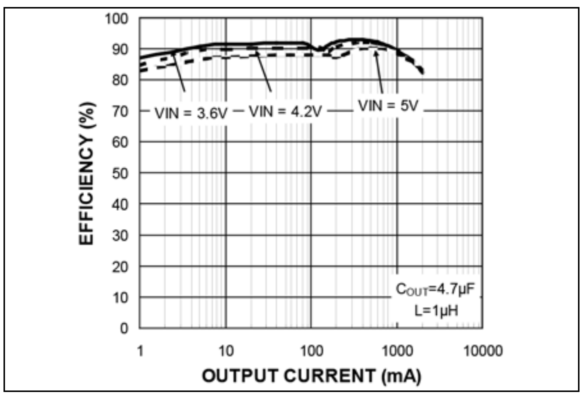


FIGURE 2-2: *Efficiency (V_{OUT} = 2.5V) vs. Output Current.*

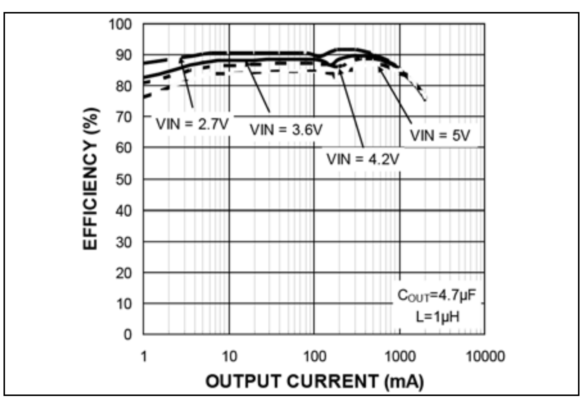


FIGURE 2-3: *Efficiency (V_{OUT} = 1.8V) vs. Output Current.*

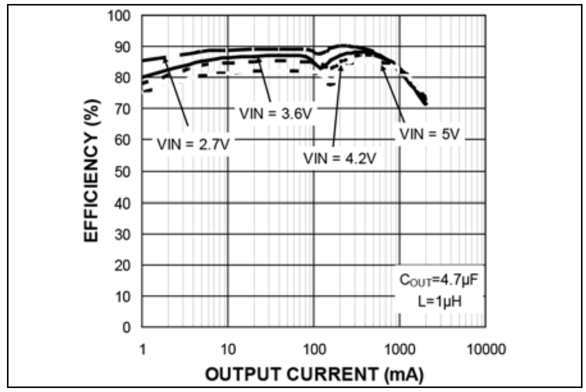


FIGURE 2-4: *Efficiency (V_{OUT} = 1.5V) vs. Output Current.*

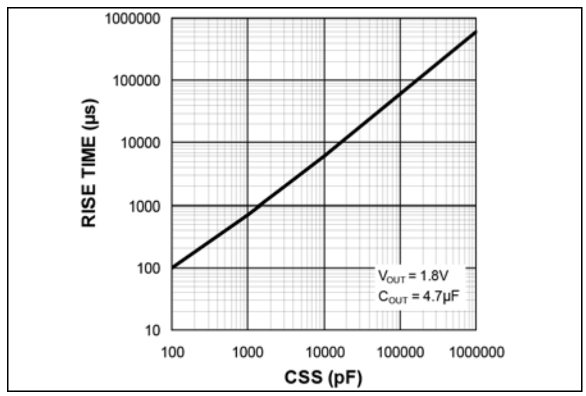


FIGURE 2-5: *V_{OUT} Rise Time vs. C_{SS}.*

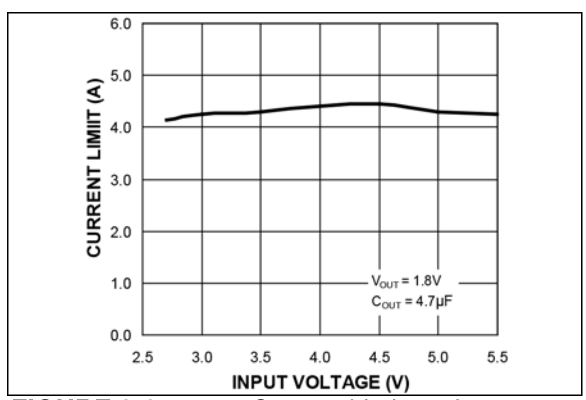


FIGURE 2-6: *Current-Limit vs. Input Voltage.*

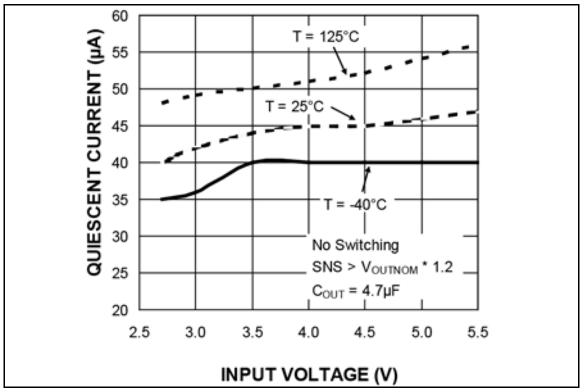


FIGURE 2-7: *Quiescent Current vs. Input Voltage.*

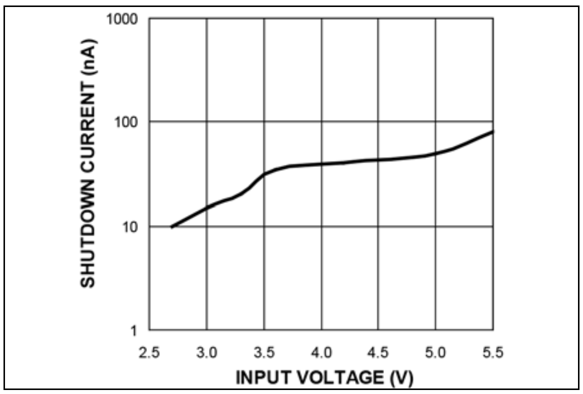


FIGURE 2-8: *Shutdown Current vs. Input Voltage.*

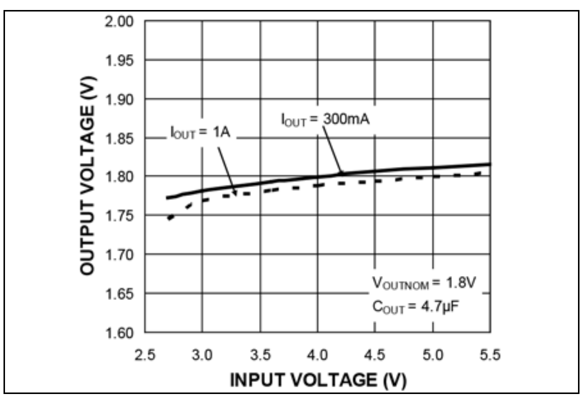


FIGURE 2-9: *Line Regulation (CCM).*

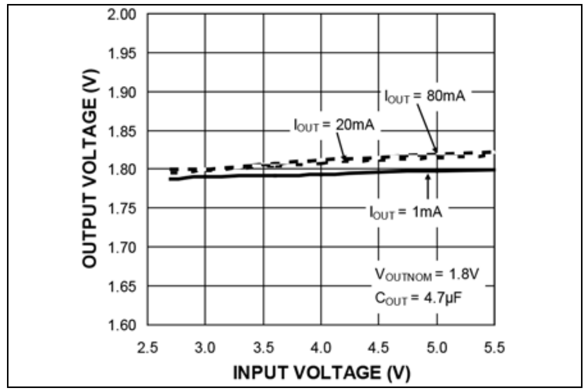


FIGURE 2-10: *Line Regulation (HLL).*

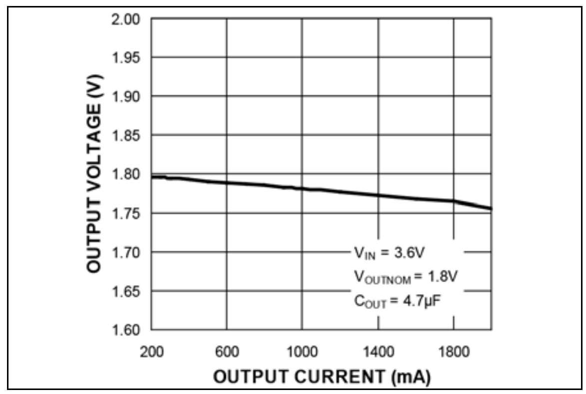


FIGURE 2-11: *Load Regulation (CCM).*

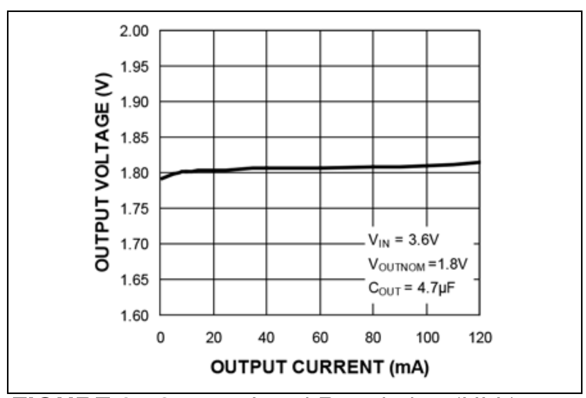


FIGURE 2-12: *Load Regulation (HLL).*

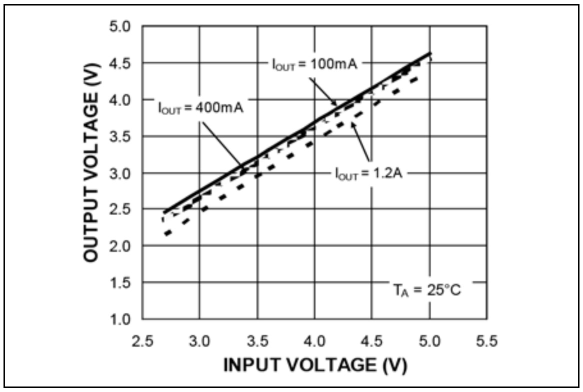


FIGURE 2-13: *Maximum Output Voltage vs. Input Voltage.*

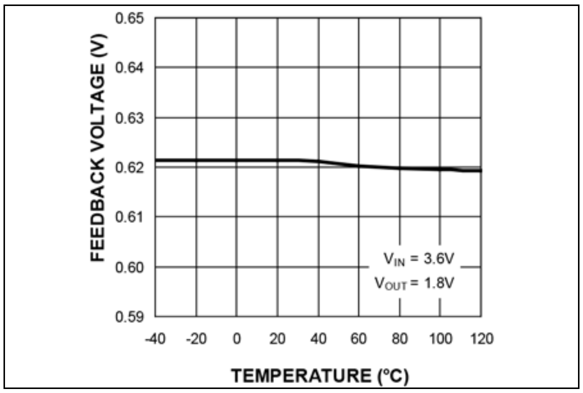


FIGURE 2-14: *Feedback Voltage vs. Temperature.*

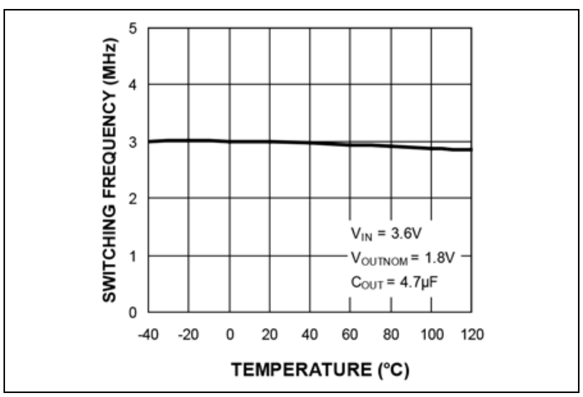


FIGURE 2-15: *Switching Frequency vs. Temperature.*

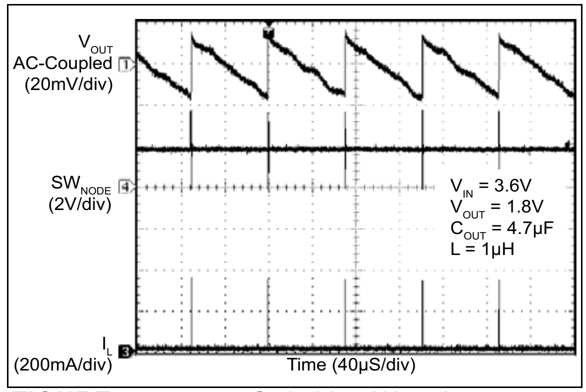


FIGURE 2-16: *Switching Waveform Discontinuous Mode (1 mA).*

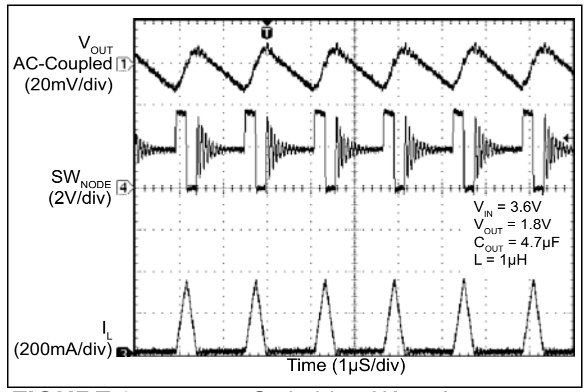


FIGURE 2-17: *Switching Waveform Discontinuous Mode (50 mA).*

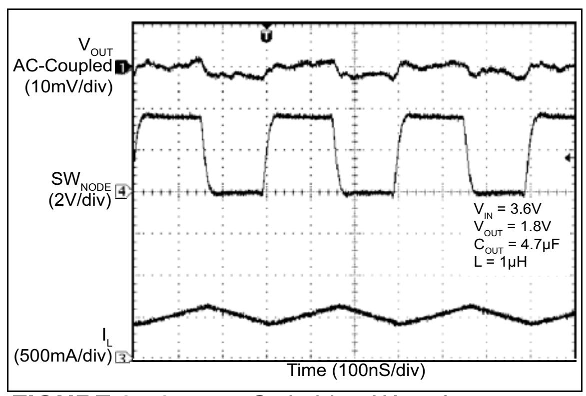


FIGURE 2-18: *Switching Waveform Continuous Mode (500 mA).*

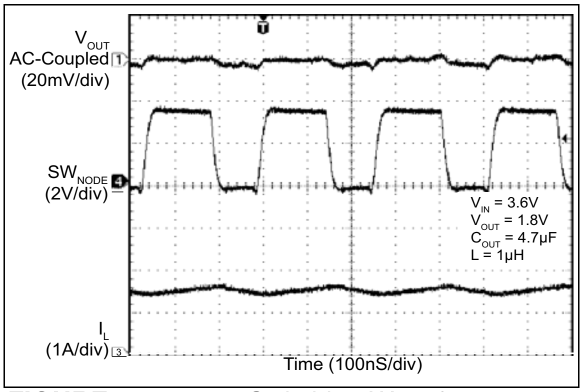


FIGURE 2-19: *Switching Waveform Continuous Mode (1.5A).*

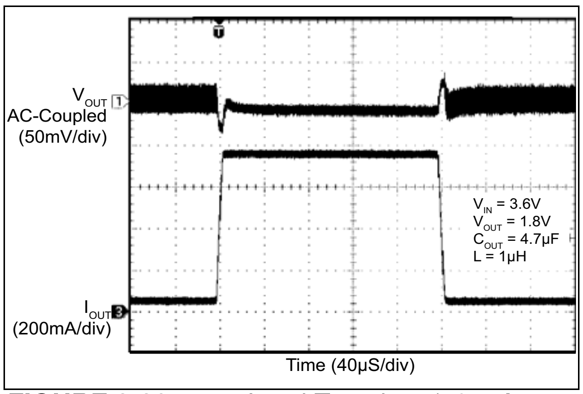


FIGURE 2-20: *Load Transient (50 mA to 750 mA).*

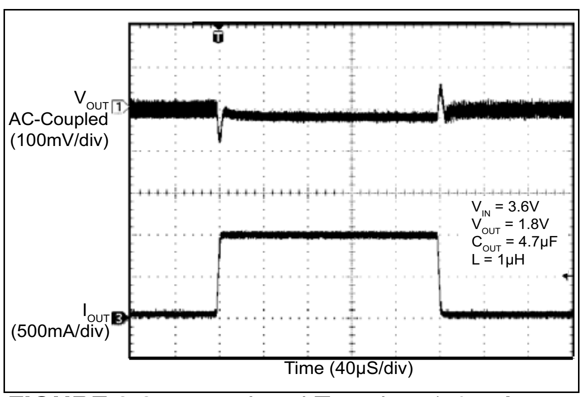


FIGURE 2-21: *Load Transient (50 mA to 1A).*

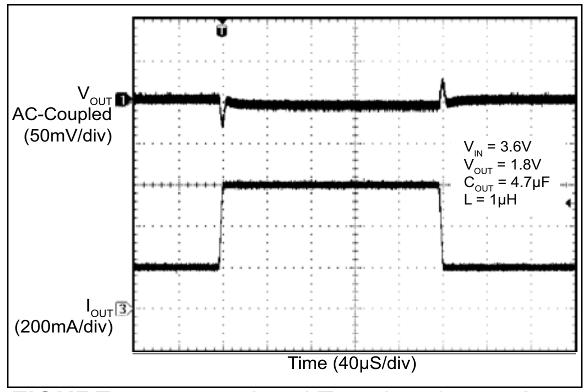


FIGURE 2-22: *Load Transient (200 mA to 600 mA).*

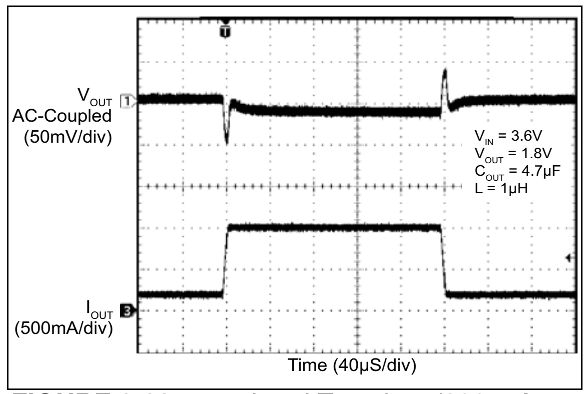


FIGURE 2-23: *Load Transient (200 mA to 1A).*

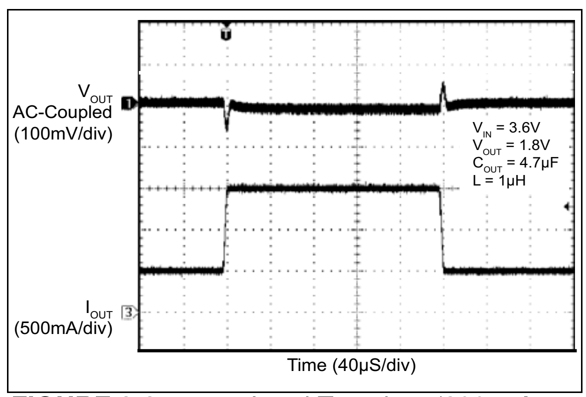


FIGURE 2-24: *Load Transient (200 mA to 1.5A).*

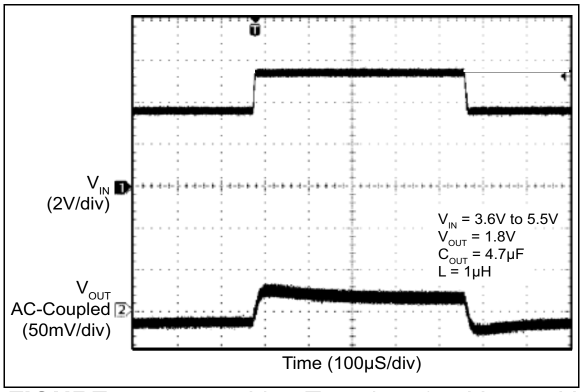


FIGURE 2-25: *Line Transient (3.6V to 5.5V at 1.5A).*

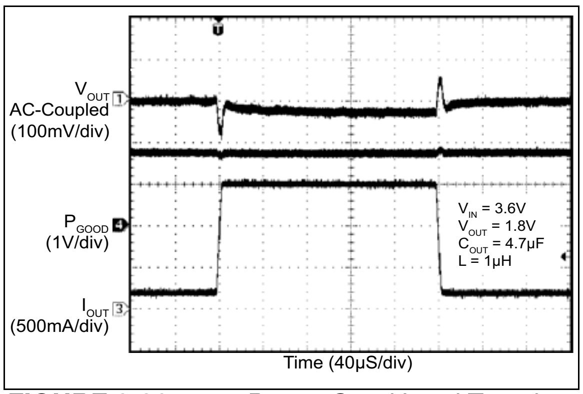


FIGURE 2-26: *Power Good Load Transient (200 mA to 1.5A).*

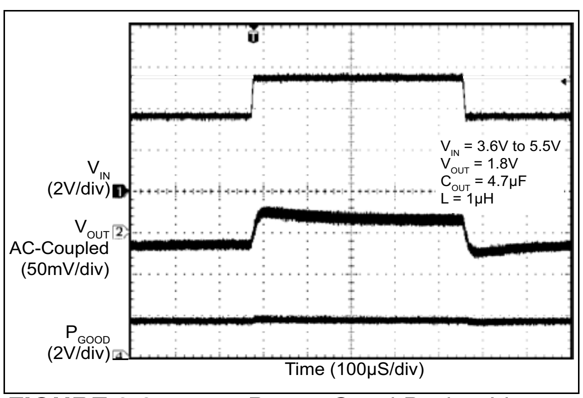


FIGURE 2-27: *Power Good During Line Transient (3.6V to 5.5V at 1.5A).*

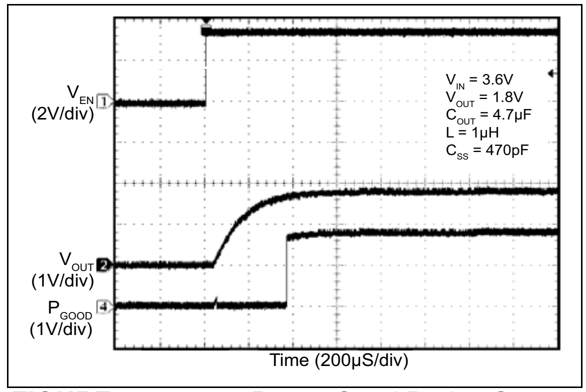


FIGURE 2-28: *Power Good During Startup.*

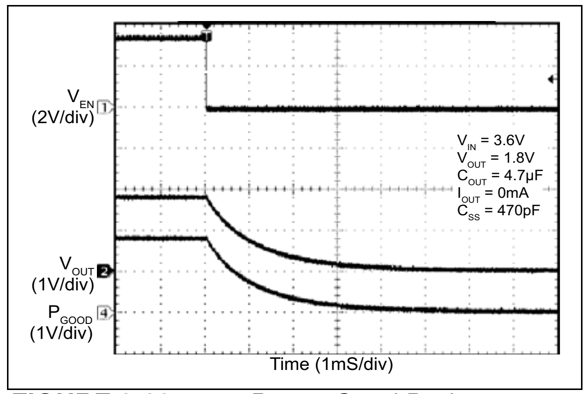


FIGURE 2-29: *Power Good During Shutdown (MIC23159).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (Adjustable)	Pin Name	Description
1	VIN1	Power Input Voltage for Regulator 1. Connect a capacitor to ground to decouple noise and switching transients.
2	PGND1	Power Ground for Regulator 1.
3	SW1	Switch (Output): Internal power MOSFET output switches for regulator 1.
4	SW2	Switch (Output): Internal power MOSFET output switches for regulator 2.
5	PGND2	Power Ground for Regulator 2.
6	VIN2	Power Input Voltage for Regulator 2. Connect a capacitor to ground to decouple noise and switching transients.
7	AVIN2	Analog Input Voltage for Regulator 2. Tie to VIN2 and connect a capacitor to ground to decouple noise.
8	AGND2	Analog Ground for Regulator 2. Connect to a central ground point where all high current paths meet (C_{IN}, C_{OUT}, PGND2) for best operation.
9	EN2	Enable Input for Regulator 2. Logic high enables operation of regulator 2. Logic low will shut down regulator 2. Do not leave floating.
10	SNS2	Sense Input for Regulator 2. Connect to the output of regulator 2 as close to the output capacitor as possible to accurately sense the output voltage.
11	FB2	Feedback Input for Regulator 2. Connect a resistor divider from the output of regulator 2 to ground to set the output voltage.
12	PG2	Power Good Output for Regulator 2. Open drain output for the power good indicator for output 2. Use a pull-up resistor between this pin and VOUT2 to indicate a power good condition.
13	SS2	Soft-Start for Regulator 2. Connect a minimum of 200 pF capacitor to ground to set the turn-on time of regulator 2. Do not leave floating.
14	SS1	Soft-Start for Regulator 1. Connect a minimum of 200 pF capacitor to ground to set the turn-on time of regulator 1. Do not leave floating.
15	PG1	Power Good Output for Regulator 1. Open drain output for the power good indicator for output 1. Use a pull-up resistor between this pin and VOUT1 to indicate a power good condition.
16	FB1	Feedback Input for Regulator 1. Connect a resistor divider from the output of regulator 1 to ground to set the output voltage.
17	SNS1	Sense Input for Regulator 1. Connect to the output of regulator 1 as close to the output capacitor as possible to accurately sense the output voltage.
18	EN1	Enable Input for Regulator 1. Logic high enables operation of regulator 1. Logic low will shut down regulator 1. Do not leave floating.
19	AGND1	Analog Ground for Regulator 1. Connect to a central ground point where all high current paths meet (C_{IN}, C_{OUT}, PGND1) for best operation.
20	AVIN1	Analog Input Voltage for Regulator 1. Tie to VIN1 and connect a capacitor to ground to decouple noise.
EP	ePAD	Exposed Heat Sink Pad. Connect to PGND.

4.0 FUNCTIONAL DESCRIPTION

4.1 VIN

The input supply (VIN) provides power to the internal MOSFETs for the switch mode regulator section. The VIN operating range is 2.7V to 5.5V. An input capacitor with a minimum voltage rating of 6.3V is recommended. Due to the high switching speed, a minimum 2.2 µF bypass capacitor placed close to VIN and the power ground (PGND) pin is required. Refer to the PCB Layout Recommendations for details.

4.2 AVIN

Analog VIN (AVIN) provides power to the internal control and analog supply circuitry. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN. A 1 µF capacitor as close to AVIN as possible is recommended. Refer to the PCB Layout Recommendations for details.

4.3 EN

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.1 µA. Do not leave the EN pin floating. When disabled, the MIC23159 switches in a 225Ω load from the SNS pin to AGND to discharge the output capacitor.

4.4 SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin, and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes whenever possible.

4.5 SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to the layout recommendations for more details. The SNS pin also provides the output active discharge circuit path to pull down the output voltage when the device is disabled.

4.6 AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the PCB Layout Recommendations for details.

4.7 PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop as applicable. Refer to the layout recommendations for more details.

4.8 PG

The power good (PG) pin is an open-drain output that indicates when the output voltage is within regulation. This is indicated by a logic high signal when the output voltage is above the PG threshold. Connect a pull-up resistor greater than 5 kΩ from PG to VOUT.

4.9 SS

An external soft-start circuitry set by a capacitor on the SS pin reduces inrush current and prevents the output voltage from overshooting at start-up. The SS pin is used to control the output voltage ramp up time and the approximate equation for the ramp time in milliseconds is $296 \times 10^3 \times \ln(10) \times C_{SS}$. For example, for a C_{SS} = 470 pF, $t_{RISE} \approx 300$ µs. Refer to the “VOUT Rise Time vs. CSS” graph in the Typical Characteristics section. The minimum recommended value for C_{SS} is 200 pF.

4.10 FB

The feedback (FB) pin is provided for the adjustable voltage option. This is the control input for setting the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.62V reference within the regulation loop.

The output voltage can be calculated using Equation 4-1:

EQUATION 4-1:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} = 0.62V

TABLE 4-1: RECOMMENDED FB RESISTOR VALUES

V_{OUT}	R1	R2
1.2V	274 kΩ	294 kΩ
1.5V	316 kΩ	221 kΩ
1.8V	301 kΩ	158 kΩ
2.5V	324 kΩ	107 kΩ
3.3V	309 kΩ	71.5 kΩ

5.0 APPLICATION INFORMATION

The MIC23158/9 are high-performance DC/DC step down regulators offering a small solution size. Supporting two outputs of up to 2A each in a 3 mm x 4 mm QFN package. Using the HyperLight Load switching scheme, the MIC23158/9 are able to maintain high efficiency throughout the entire load range while providing ultra fast load transient response. The following sections provide additional device application information.

5.1 Input Capacitor

A 2.2 µF ceramic capacitor or greater should be placed close to the VIN pin and PGND pin for bypassing. A Murata GRM188R60J475KE19D, size 0603, 4.7 µF ceramic capacitor is recommended based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor.

5.2 Output Capacitor

The MIC23158/9 are designed for use with a 2.2 µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the Murata GRM188R60J475KE19D, size 0603, 4.7 µF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended.

5.3 Inductor Selection

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23158/9 are designed for use with a 0.47 µH to 2.2 µH inductor. For faster transient response, a 0.47 µH inductor will yield the best result. For lower output ripple, a 2.2 µH inductor is recommended.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate.

Peak current can be calculated in Equation 5-1:

EQUATION 5-1:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT}\left(\frac{1 - V_{OUT} \div V_{IN}}{2 \times f \times L}\right)\right]$$

As shown by the calculation above, the peak inductor current is inversely proportional to the switching frequency and the inductance. The lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuit for details.

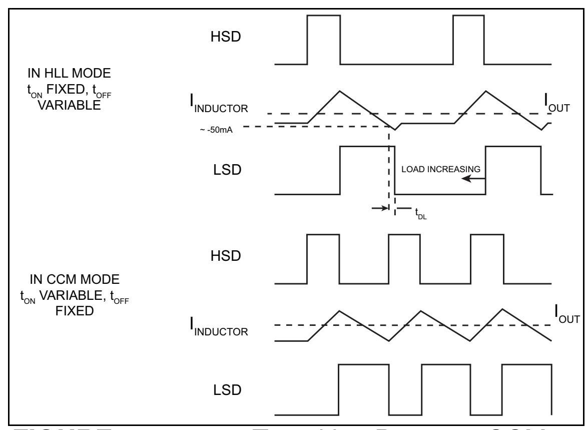


FIGURE 5-1: *Transition Between CCM Mode and HLL Mode.*

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations subsection.

The transition between continuous conduction mode (CCM) to HyperLight Load mode is determined by the inductor ripple current and the load current.

The diagram shows the signals for high-side switch drive (HSD) for t_{ON} control, the inductor current, and the low-side switch drive (LSD) for t_{OFF} control.

In HLL mode, the inductor is charged with a fixed t_{ON} pulse on the high side switch. After this, the low side switch is turned on and current falls at a rate of V_{OUT}/L. The controller remains in HLL mode while the inductor falling current is detected to cross approximately –50 mA. When the LSD (or t_{OFF}) time reaches its minimum, and the inductor falling current is no longer able to reach the threshold, the part is in CCM mode.

Once in CCM mode, the t_{OFF} time will not vary. Therefore, it is important to note that if L is large enough, the HLL transition level will not be triggered.

That inductor is illustrated in Figure 5-1.

EQUATION 5-2:

$$L_{MAX} = \frac{V_{OUT} - 135ns}{2 - 50mA}$$

5.4 Duty Cycle

The typical maximum duty cycle of the MIC23158/9 is 80%.

5.5 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

EQUATION 5-3:

$$Efficiency = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET R_{DSON} multiplied by the switch current squared. During the off cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 3 MHz frequency and the switching transitions make up the switching losses.

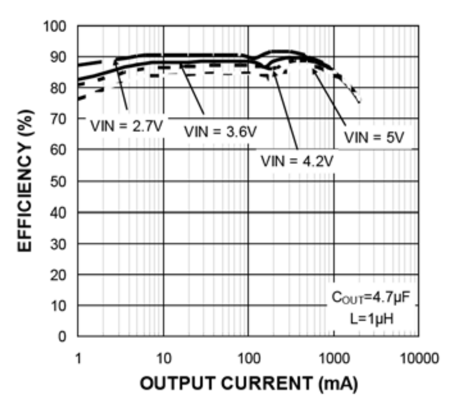


FIGURE 5-2: *Efficiency Under Load.*

Figure 5-2 shows an efficiency curve. From 1 mA load to 2A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23158/9 are able to maintain high efficiency at low output currents.

Over 180 mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 5-4:

EQUATION 5-4:

$$P_{DCR} = I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 5-5:

EQUATION 5-5:

$$Eff_{Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade off between efficiency and size in this case.

5.6 HyperLight Load Mode

The MIC23158/9 use a minimum on and off time proprietary control loop. When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using an NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The synchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23158/9 work in HyperLight Load to regulate the output. As the output current increases, the off time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23158/9 during light load currents by only switching when it is needed.

As the load current increases, the MIC23158/9 go into continuous conduction mode (CCM) and switches at a frequency centered at 3 MHz. The equation to calculate the load when the MIC23158/9 goes into continuous conduction mode may be approximated by the following formula:

EQUATION 5-6:

$$I_{LOAD} > \frac{(V_{IN} - V_{OUT}) \times D}{2L \times f}$$

As shown in Equation 5-6, the load at which the MIC23158/9 transition from HyperLight Load mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 5-3, as the output current increases, the switching frequency also increases until the MIC23158/9 go from HyperLight Load mode to PWM mode at approximately 180 mA. The MIC23158/9 will switch at a relatively constant frequency around 3 MHz once the output current is over 180 mA.

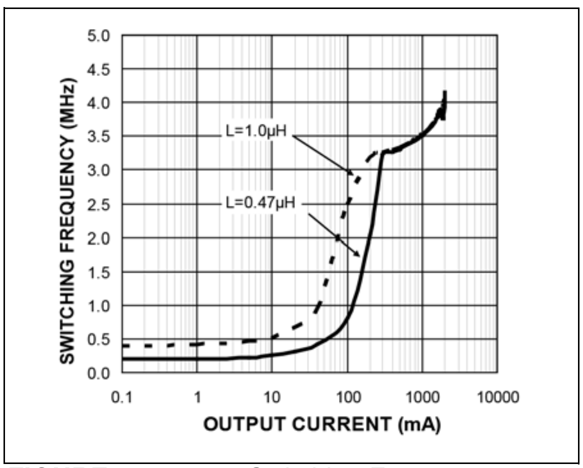
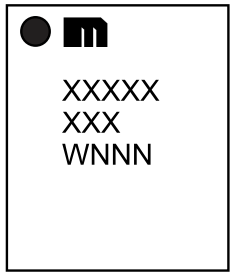


FIGURE 5-3: *Switching Frequency vs. Output Current.*

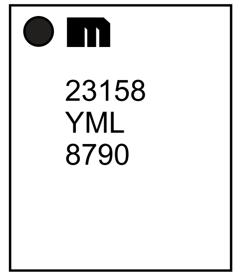
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

20-Lead QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

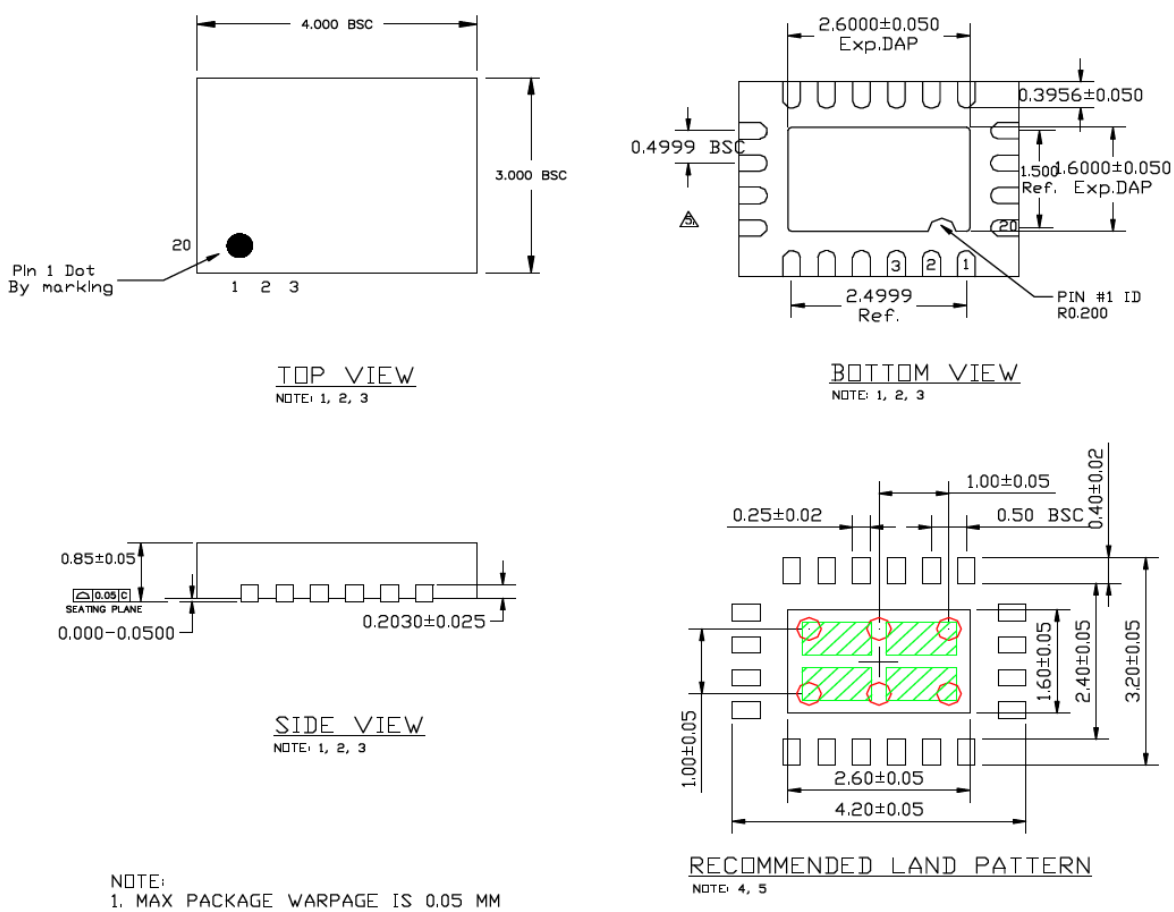
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

20-Lead QFN 3 mm x 4 mm Package Outline and Recommended Land Pattern

TITLE
20 LEAD QFN 3x4mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN34-20LD-PL-1	UNIT	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x0.50 MM IN SIZE, 0.70 MM PITCH.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (May 2018)

- Converted Micrel document MIC23158/9 to Microchip data sheet DS20006020A.
- Minor text changes throughout.
- COUT1,2 corrected to COUT3,4 in Table 1-1.
- Added V_{REF} qualifier in Equation 4-1.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC23158:	3 MHz PWM Dual 2A Buck Regulator with HyperLight Load and Power Good
	MIC23159:	3 MHz PWM Dual 2A Buck Regulator with HyperLight Load and Power Good with Auto-Discharge
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS-Compliant
Package:	ML =	20-Lead 3 mm x 4 mm QFN
Media Type:	T5 =	500/Reel
	TR =	5,000/Reel

Examples:

a) MIC23158YML-T5: MIC23158, –40°C to +125°C Temperature Range, 20-Lead QFN, 500/Reel

b) MIC23158YML-TR: MIC23158, –40°C to +125°C Temperature Range, 20-Lead QFN, 5,000/Reel

c) MIC23159YML-T5: MIC23159, Auto-Discharge Feature, –40°C to +125°C Temperature Range, 20-Lead QFN, 500/Reel

d) MIC23159YML-TR: MIC23159, Auto-Discharge Feature, –40°C to +125°C Temperature Range, 20-Lead QFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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