

N-Channel Power MOSFET

100V, 70A, 13mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low gate charge for fast power switching
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

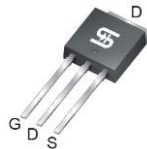
APPLICATION

- Synchronous Rectifier in SMPS
- LED lighting application
- 48V Battery System

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	100	V
$R_{DS(on)}$ (max)	13	mΩ
Q_g	145	nC



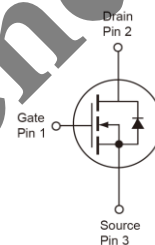
TO-251 (IPAK)



TO-251S (IPAK SL)



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 3)	I_D	$T_C = 25^\circ\text{C}$	70
		$T_C = 70^\circ\text{C}$	61
		$T_A = 25^\circ\text{C}$	12
		$T_A = 70^\circ\text{C}$	9
Drain Current-Pulsed (Note 1)	I_{DM}	150	A
Avalanche Current, $L=0.5\text{mH}$	I_{AS}, I_{AR}	25	A
Avalanche Energy, $L=0.5\text{mH}$	E_{AS}, E_{AR}	156	mJ
Maximum Power Dissipation (Note 2)	I_D	$T_C = 25^\circ\text{C}$	120
		$T_C = 70^\circ\text{C}$	80
		$T_A = 25^\circ\text{C}$	8.3
		$T_A = 70^\circ\text{C}$	5.3
Storage Temperature Range	T_{STG}	- 55 to +150	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	Limit	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1	$^{\circ}\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	40	$^{\circ}\text{C/W}$

ELECTRICAL SPECIFICATIONS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	100	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	$R_{DS(ON)}$	--	10	13	$\text{m}\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	2	3	4	V
Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Dynamic						
Total Gate Charge	$V_{DS} = 50\text{V}, I_D = 30\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	145	--	nC
Gate-Source Charge		Q_{gs}	--	25	--	
Gate-Drain Charge		Q_{gd}	--	43	--	
Input Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	4300	--	pF
Output Capacitance		C_{oss}	--	300	--	
Reverse Transfer Capacitance		C_{rss}	--	120	--	
Switching						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 50\text{V},$ $R_G = 3\Omega,$	$t_{d(on)}$	--	27	--	ns
Turn-On Rise Time		t_r	--	13	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15	--	
Turn-Off Fall Time		t_f	--	42	--	
Source-Drain Diode						
Forward On Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	V_{SD}	--	0.8	1.3	V
Reverse Recovery Time	$I_S = 30\text{A}, T_J = 25^{\circ}\text{C}$ $di_f/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	165	--	ns
Reverse Recovery Charge		Q_{rr}	--	175	--	nC

Notes:

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4PCB in still air.
- The maximum current is limited by package.

ORDERING INFORMATION

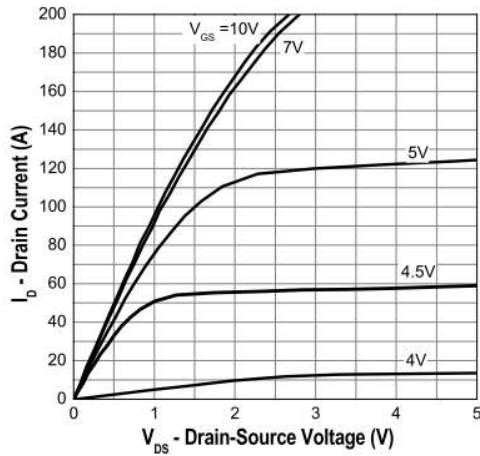
PART NO.	PACKAGE	PACKING
TSM70N10CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel
TSM70N10CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM70N10CH X0G	TO-251S (IPAK SL)	75pcs / Tube

Not Recommended

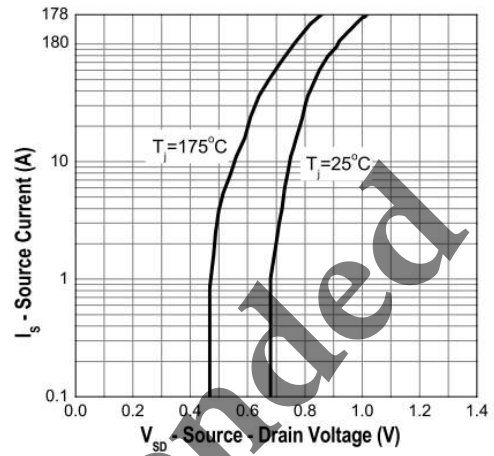
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

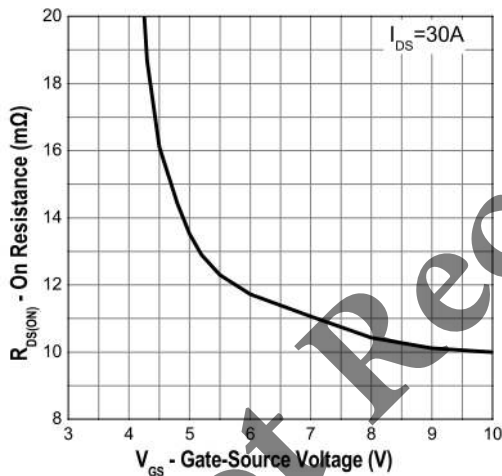
Output Characteristics



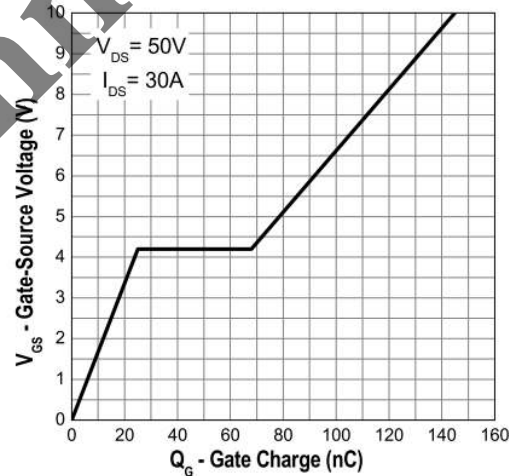
Transfer Characteristics



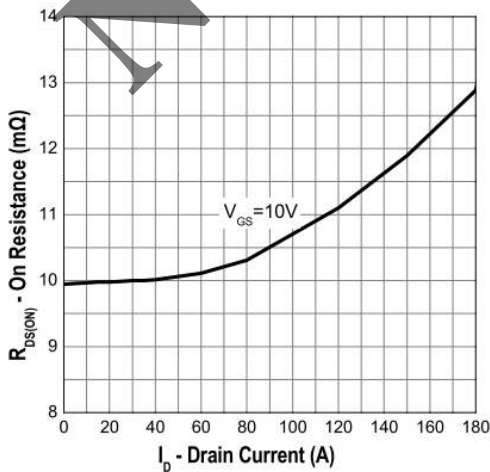
On-Resistance vs. Gate-Source Voltage



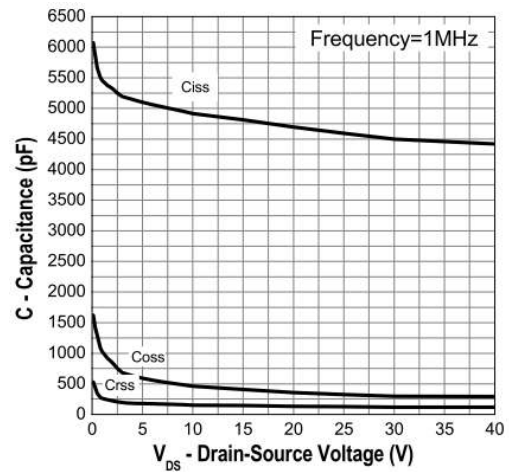
Gate Charge



On-Resistance vs. Junction Temperature



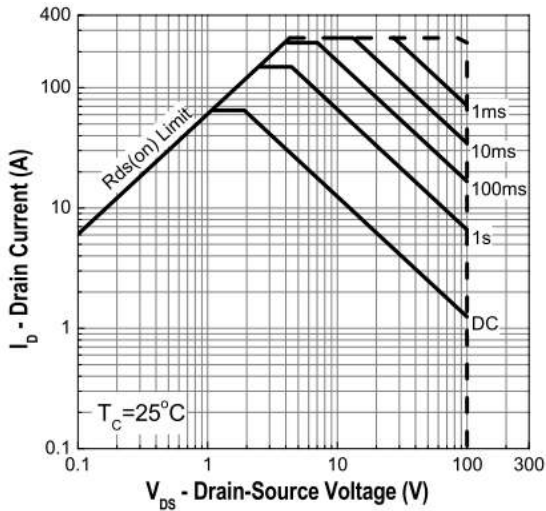
Capacitance



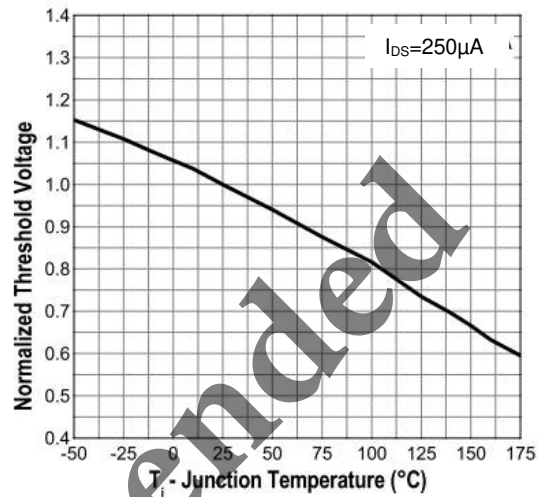
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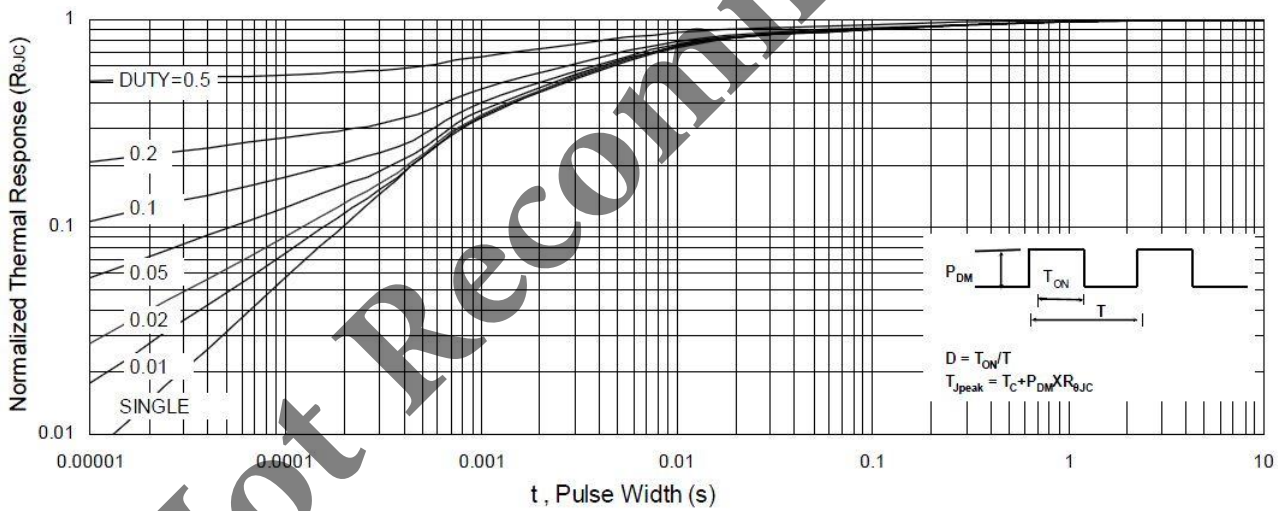
Maximum Safe Operating Area



Threshold Voltage vs. Temperature

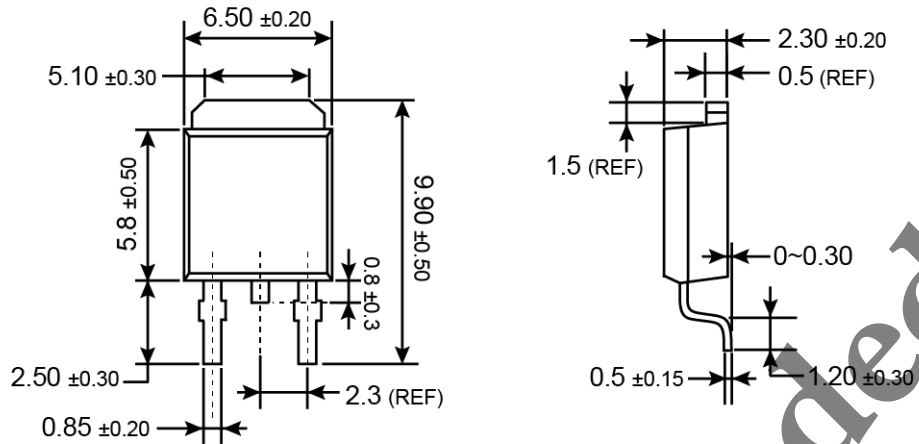


Normalized Thermal Transient Impedance, Junction-to-Ambient

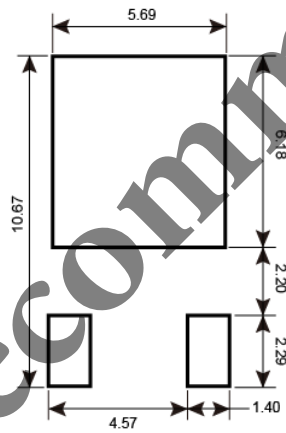


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

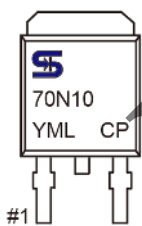
TO-252



SUGGESTED PAD LAYOUT (Unit: Millimeters)



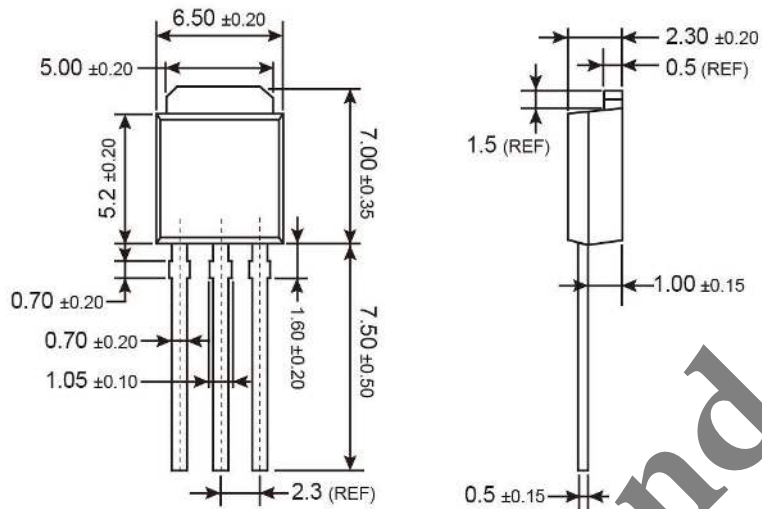
MARKING DIAGRAM



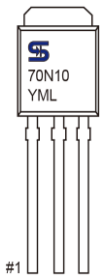
Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
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L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251



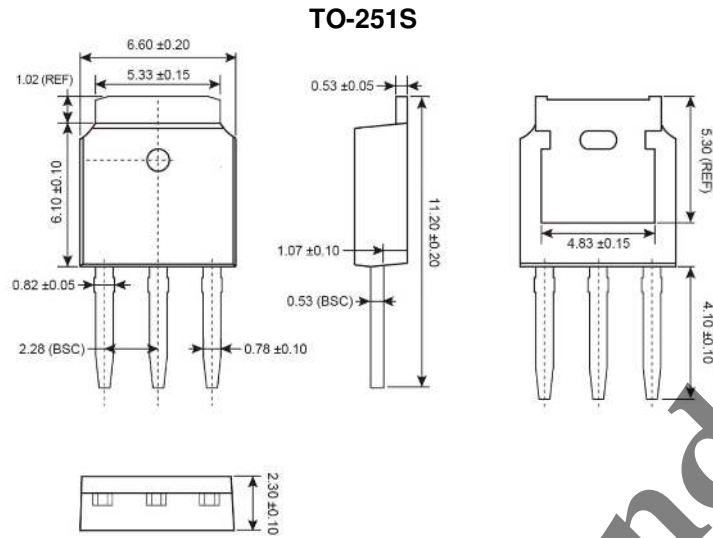
MARKING DIAGRAM



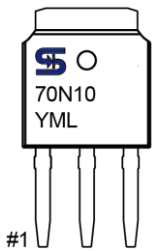
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Not Recommended

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