NTD78N03

Power MOSFET

25 V, 78 A, Single N−Channel, DPAK

Features

- Low $R_{DS(on)}$
- Optimized Gate Charge
- Pb−Free Packages are Available

Applications

- Desktop VCORE
- DC−DC Converters
- Low Side Switch

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_C = 25°C	I_D	14.8	A
		T_C = 85°C		11.5	
Power Dissipation (Note 1)		T_C = 25°C	P_D	2.3	W
Continuous Drain Current (Note 2)		T_C = 25°C	I_D	11.4	A
		T_C = 85°C		8.8	
Power Dissipation (Note 2)		T_C = 25°C	P_D	1.4	W
Continuous Drain Current ($R_{\theta JC}$)		T_C = 25°C	I_D	78	A
		T_C = 85°C		56	
Power Dissipation ($R_{\theta JC}$)		T_C = 25°C	P_D	64	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	210	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	45	A
Drain to Source dV/dt			dV/dt	8.0	V/ns
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	78	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 24 V, V_{GS} = 10 V, L = 5.0 mH, I_L(pk) = 17 A, R_G = 25 Ω)			E_{AS}	722.5	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)			T_L	260	°C

THERMAL RESISTANCE

Junction−to−Case (Drain)	$R_{\theta JC}$	1.95	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	65	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	110	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface−mounted on FR4 board using the minimum recommended pad size.

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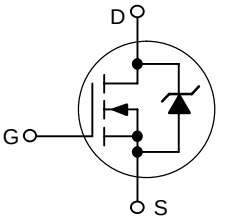
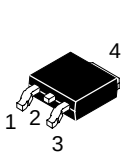
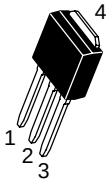
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	4.6 @ 10 V	78 A
	6.5 @ 4.5 V	



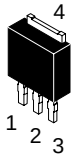
N−Channel



CASE 369AA
DPAK
(Bend Lead)
STYLE 2

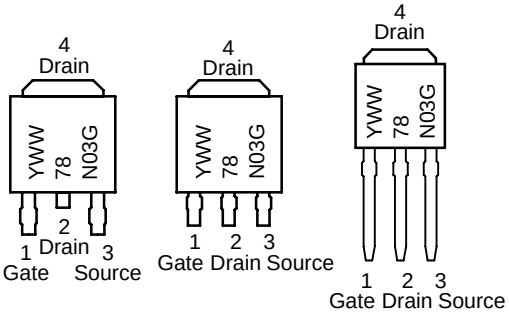


CASE 369D
DPAK
(Straight Lead)
STYLE 2



CASE 369AD
IPAK
(Straight Lead)

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
78N03 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				24		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1.5	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.6	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 78 A			4.6	6.0	mΩ
		V_{GS} = 4.5 V, I_D = 36 A			6.5	7.8	
Forward Transconductance	gFS	V_{DS} = 10 V, I_D = 15 A			22		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			1920	2250	pF
Output Capacitance	C_{oss}				960		
Reverse Transfer Capacitance	C_{rss}				420		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 20 A			25.5	35	nC
Threshold Gate Charge	$Q_{G(TH)}$				2.4		
Gate−to−Source Charge	Q_{GS}				5.3		
Gate−to−Drain Charge	Q_{GD}				18.2		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 20 A, R_G = 3.0 Ω			11		ns
Rise Time	t_r				68		
Turn−Off Delay Time	$t_{d(off)}$				23		
Fall Time	t_f				42		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.83	1.0	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/d_t = 100 A/μs, I_S = 20 A			39		ns
Charge Time	ta				17.8		
Discharge Time	tb				21		
Reverse Recovery Time	Q_{RR}				33		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	Ta = 25C			2.49		nH
Drain Inductance	L_D				0.02		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				1.0		Ω

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

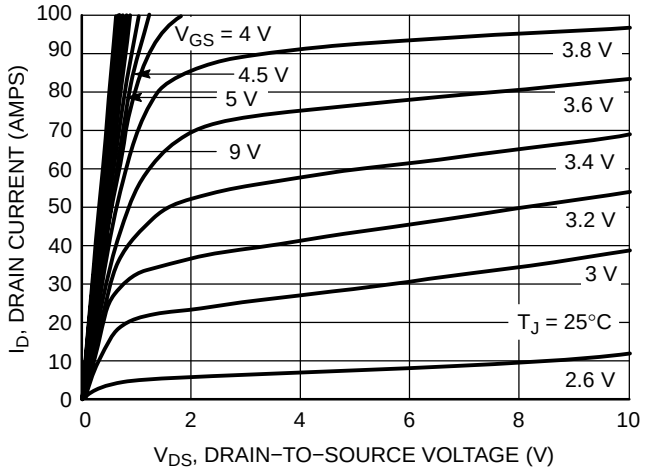


Figure 1. On−Region Characteristics

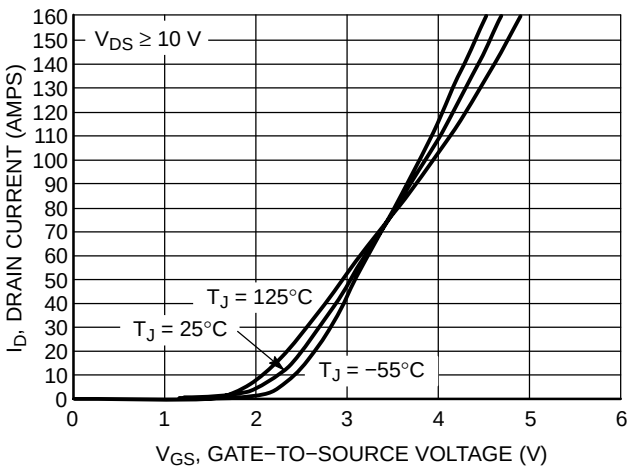


Figure 2. Transfer Characteristics

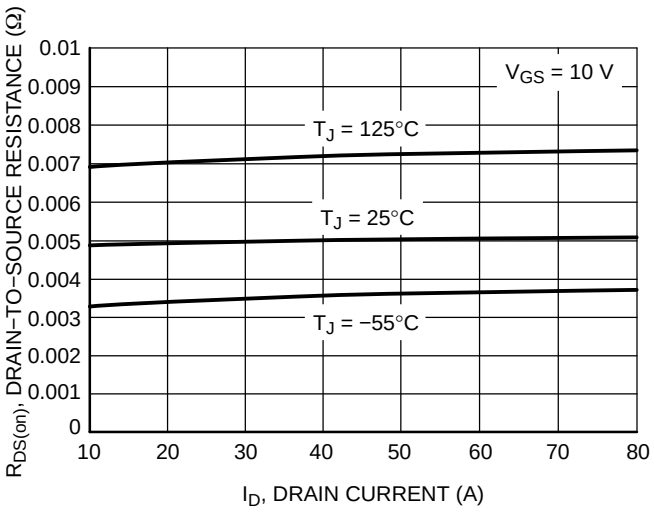


Figure 3. On−Resistance versus Drain Current and Temperature

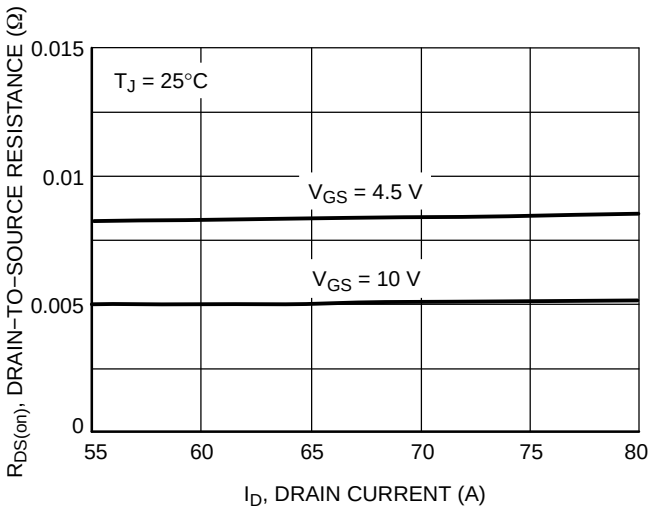


Figure 4. On−Resistance versus Drain Current and Gate Voltage

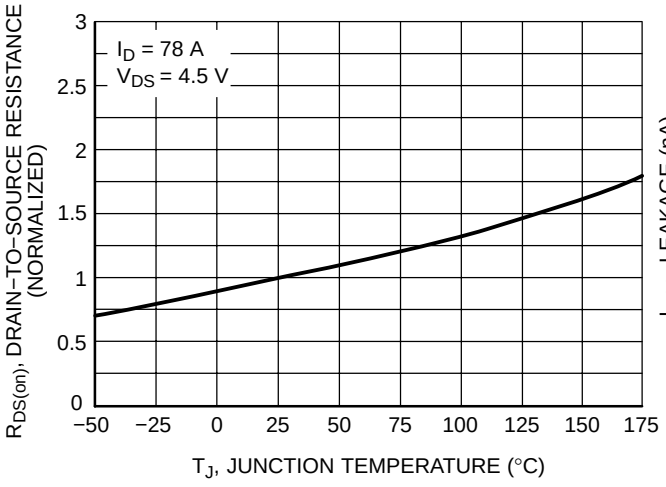


Figure 5. On−Resistance Variation with Temperature

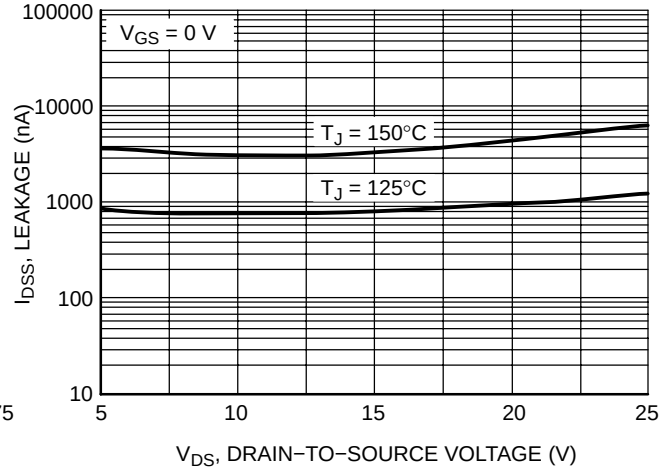


Figure 6. Drain−To−Source Leakage Current versus Voltage

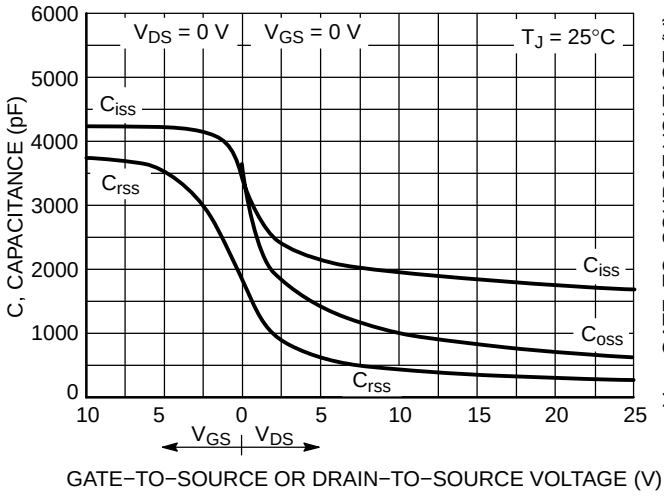


Figure 7. Capacitance Variation

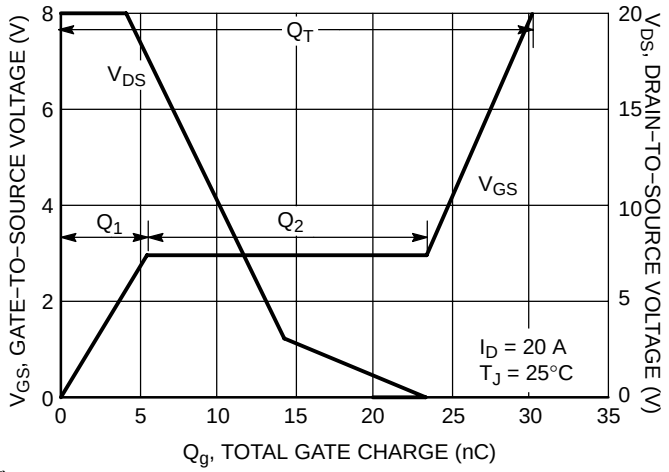


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

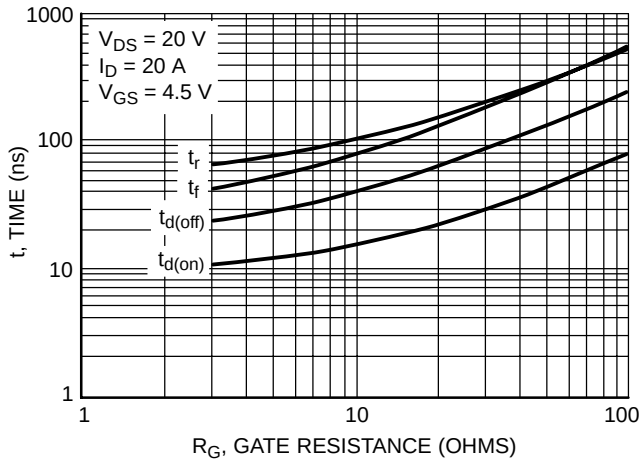


Figure 9. Resistive Switching Time Variation versus Gate Resistance

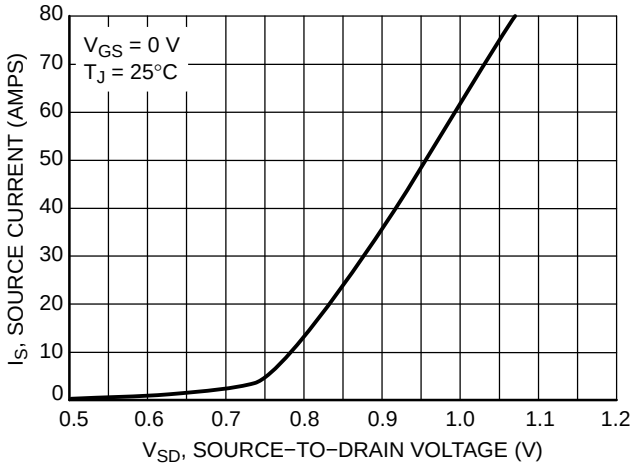


Figure 10. Diode Forward Voltage versus Current

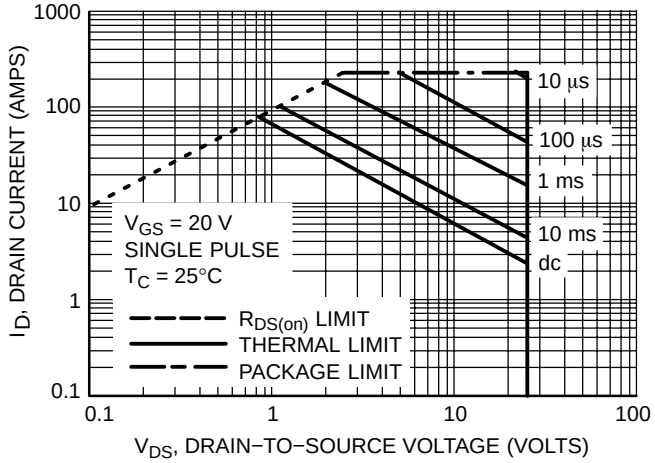


Figure 11. Maximum Rated Forward Biased Safe Operating Area

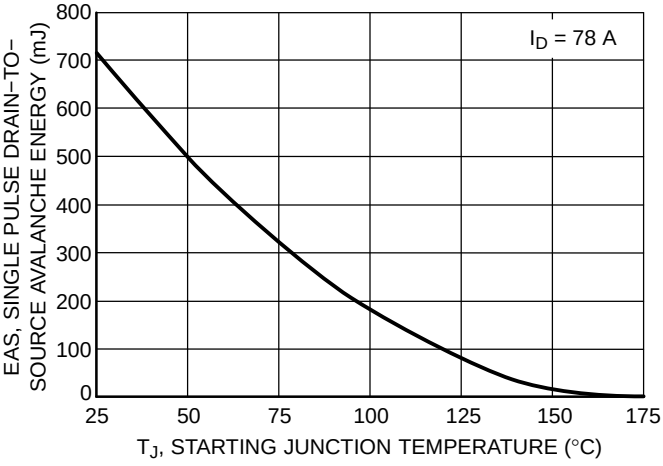


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

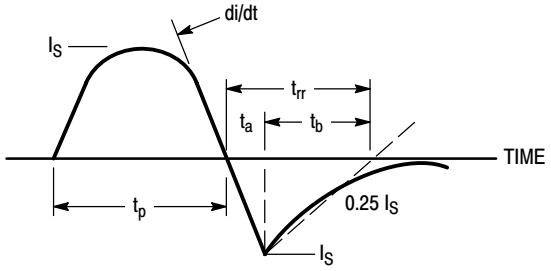


Figure 13. Diode Reverse Recovery Waveform

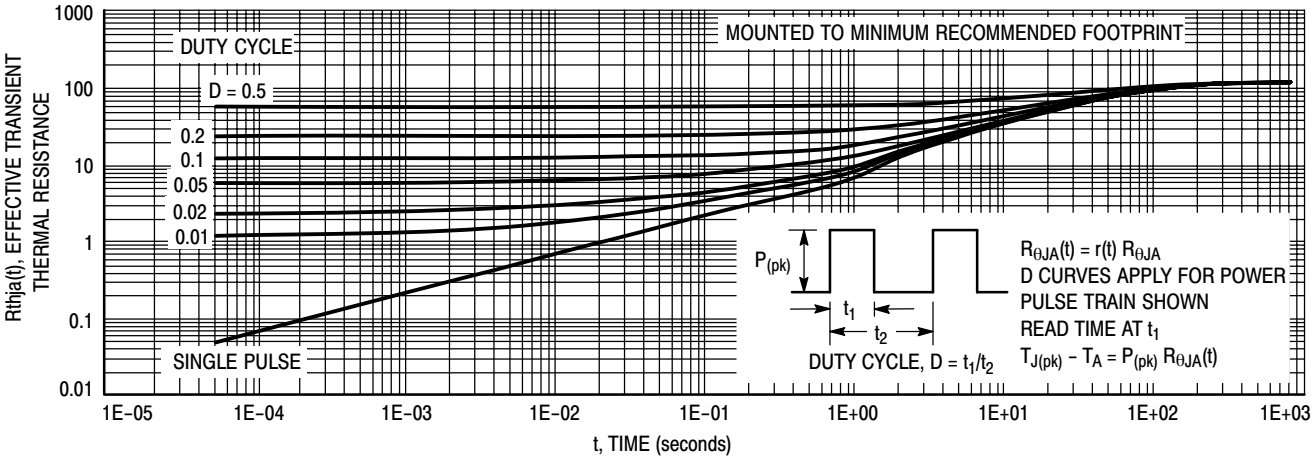
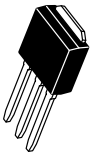


Figure 14. Thermal Response − Various Duty Cycles

ORDERING INFORMATION

Order Number	Package	Shipping†
NTD78N03	DPAK	75 Units/Rail
NTD78N03G	DPAK (Pb−Free)	75 Units/Rail
NTD78N03T4	DPAK	2500 Tape & Reel
NTD78N03T4G	DPAK (Pb−Free)	
NTD78N03−1	DPAK Straight Lead	75 Units/Rail
NTD78N03−1G	DPAK Straight Lead (Pb−Free)	
NTD78N03−35	DPAK−3 Straight Lead (3.5 ± 0.15 mm)	75 Units/Rail
NTD78N03−35G	DPAK−3 Straight Lead (3.5 ± 0.15 mm) (Pb−Free)	

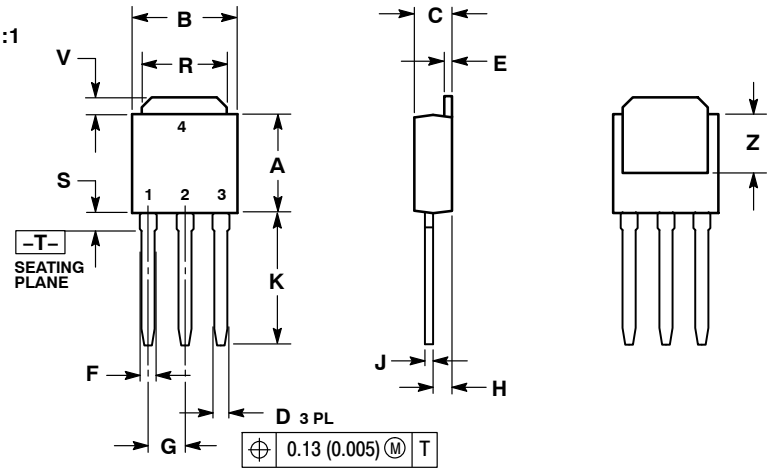
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



IPAK
CASE 369D–01
ISSUE C

DATE 15 DEC 2010

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

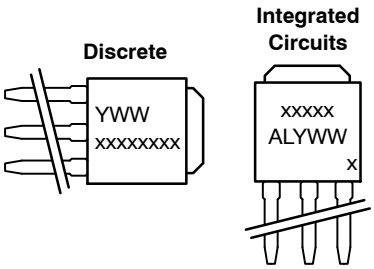
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MARKING DIAGRAMS

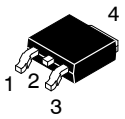


xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

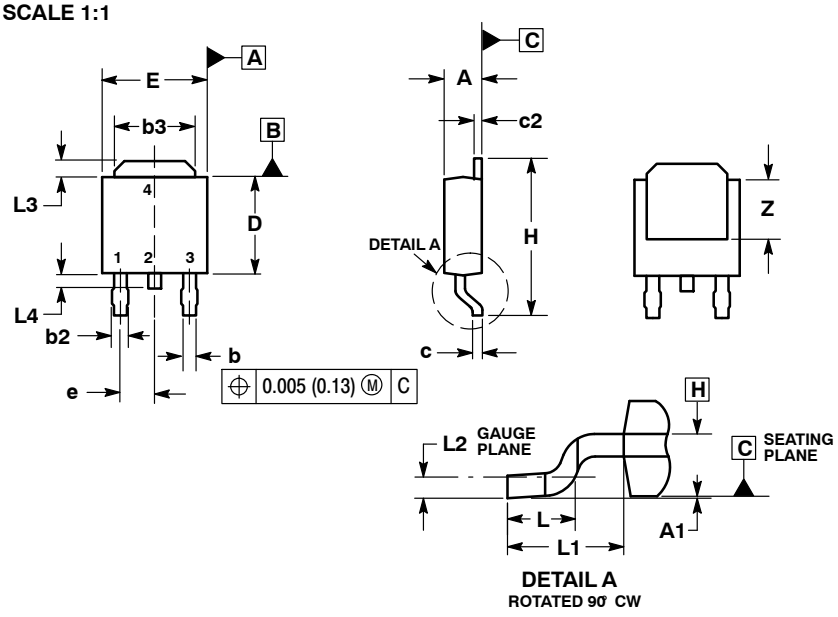
ON Semiconductor®



SCALE 1:1

DPAK (SINGLE GUAGE)
CASE 369AA−01
ISSUE B

DATE 03 JUN 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	−−−	0.040	−−−	1.01
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

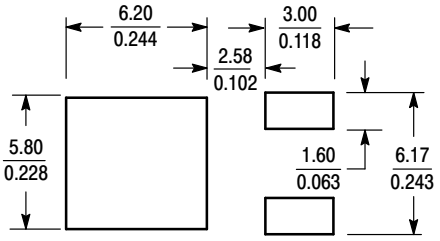
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

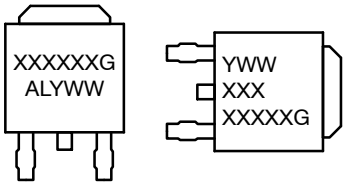
SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **Discrete**

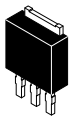
XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

DOCUMENT NUMBER:	**98AON13126D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**DPAK (SINGLE GAUGE)**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

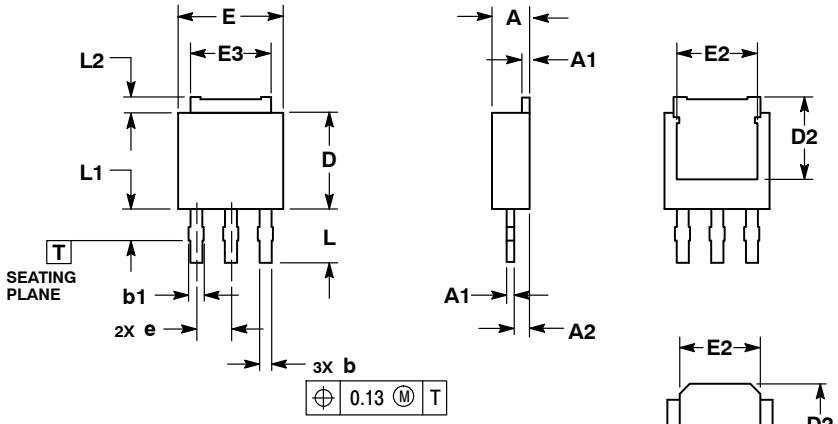
ON Semiconductor®



3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD
ISSUE B

DATE 18 APR 2013

SCALE 1:1



NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

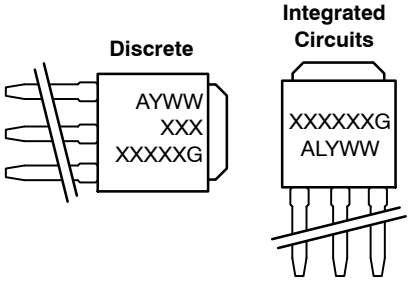
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAMS*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**3.5 MM IPAK, STRAIGHT LEAD**	**PAGE 1 OF 1**

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