bq25871 14-V, 7-A, Battery Switch Charger with Integrated 10-bit ADC

1 Features

- Adapter Input Voltage Range: 3 V to 14 V
  - Allow up to 14-V Adaptor Voltage
- Highly Integrated 7-A Battery Switch
  - Integrated MOSFETs and Current Sensing
  - Low $R_{DS(on)}$ (13-mΩ) MOSFETs for High Current Operation
- Integrated High Accuracy ADC for System Monitor
  - VBUS, VBAT, VOUT, VDROP Voltage
  - Input and Battery Current
  - Battery and VBUS Connector Temperature
- Linear Regulation (LDO) Mode Operation
  - Four Linear Regulation Loops: IBUS, IBAT, VBAT and VOUT
  - Programmable Linear Regulation Thresholds
- Programmable Safety Protections
  - VBUS, VOUT, and VBAT Over Voltage Protections (OVP)
  - IBUS and IBAT Over Current Protection (OCP)
  - IBUS Reverse Current Protection (RCP)
  - VDROP (VBUS-VOUT) OVP
  - VBUS Connector and Battery Thermal Protection
  - Thermal Shutdown
- Interrupt Status Output For Host Processor Alert
- Up To 1-MHz I^2C Read and Write Speed
- Low Battery Leakage Current in Battery Only Mode
- WCSP Package for Small Footprint

2 Applications

- Smart Phone
- Tablet PC

3 Description

The device is a 7-A battery switch charger with an integrated 10-bit ADC. The high-current battery switch charger is a 13-mΩ MOSFET with reverse current blocking designed for high efficiency and minimal voltage drop. The high-charge current capability of the device makes it ideal for smartphones, tablets, and other portable devices with large battery capacity.

The integrated 10-bit ADC can measure input voltage and current, battery voltage and current, as well as battery temperature and input connector temperature. This allows the user application to continuously monitor the power input and battery charging parameters to ensure the safety of the battery charging. The flexible OVP and OCP thresholds for VBUS, VOUT, and battery can be modified via I^2C registers as the battery goes through constant current (CC) and constant voltage (CV) mode.

The I^2C serial interface of the device can operate at speeds up to 1 MHz and allows access to the ADC's measurements of the different charging parameters and also allows for flexible software control of the device. The $\overline{INT}$ pin provides instantaneous feedback to the host in case of a fault condition. I^2C status registers allow the host to read the current status of all faults and events.

The device comes in a DSBGA package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25871	YFF (42)	2.5 mm x 3.1 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

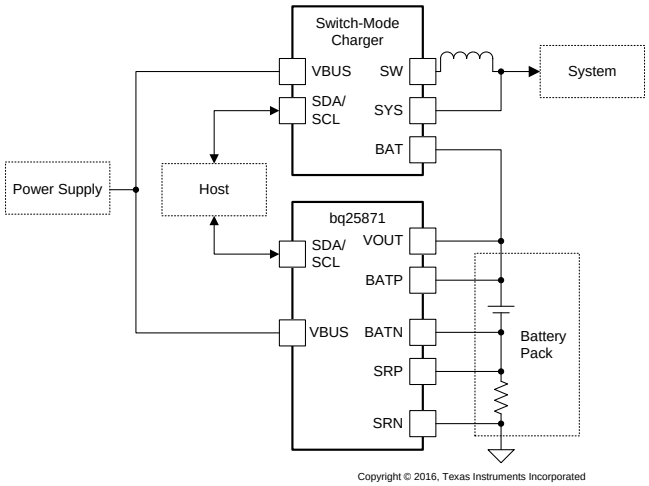


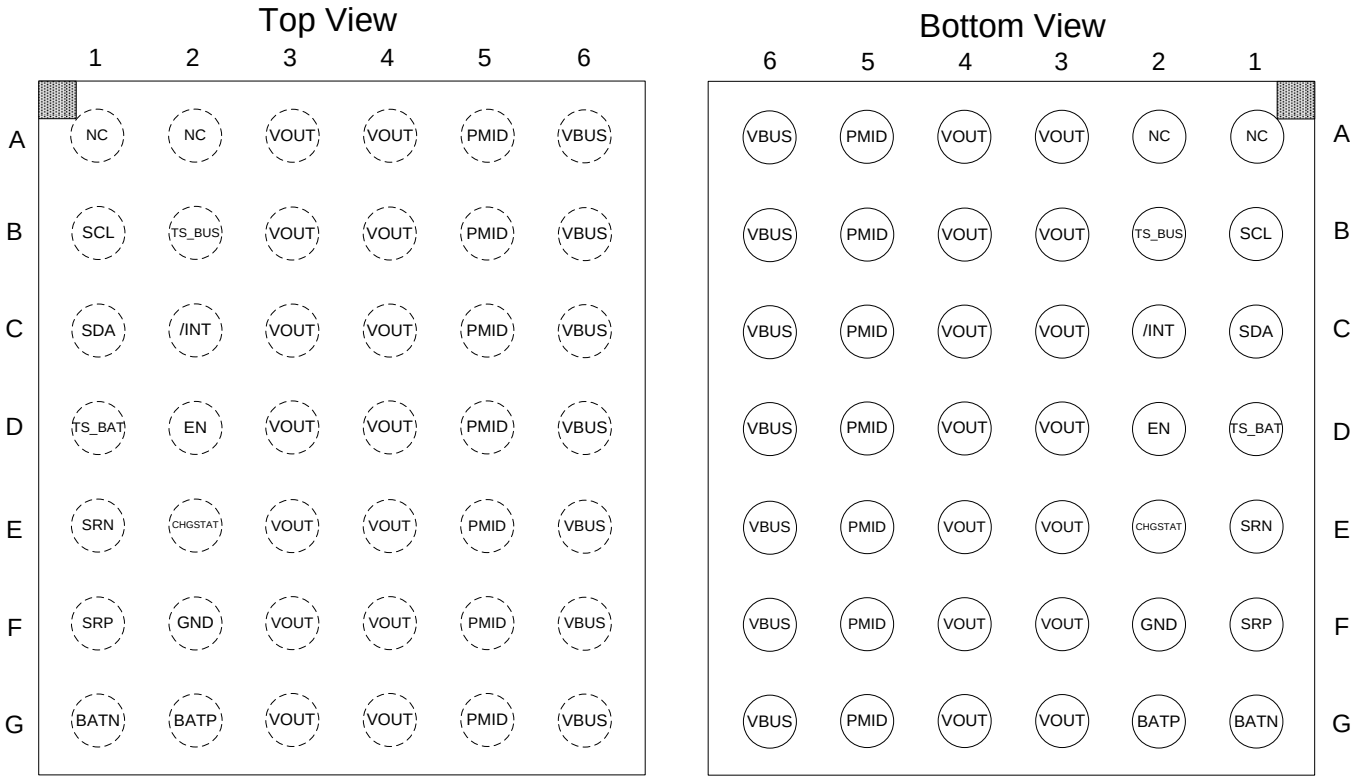
Table of Contents

4 Revision History

DATE	REVISION	NOTES
October 2016	*	Initial release.

5 Pin Configuration and Functions

DSBGA Package
42 Pin YYF
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A3-G3, A4-G4	P	Device power output. Connected to the drain of Q2.
PMID	A5-G5	P	Tie pins to each other and leave floating. Do not connect to any other pins. Connected to the drain of Q1 and source of Q2.
TS_BUS	B2	AI	VBUS connector temperature qualification voltage input. Requires external resistor divider and voltage reference.
GND	F2	P	Device ground.
TS_BAT	D1	AI	Battery temperature qualification voltage input. Requires external resistor divider and voltage reference.
BATN	G1	AI	Negative input for battery voltage sensing. Connect to negative terminal of battery pack. Place 100-Ω/1-kΩ series resistance between pin and negative terminal.
BATP	G2	AI	Positive input for battery voltage sensing. Connect to positive terminal of battery pack. Place 100-Ω/1-kΩ series resistance between pin and positive terminal.
SRN	E1	AI	Negative input for battery current sensing. Place R_{SENSE} between SRN and SRP for battery current sensing.
SRP	F1	AI	Positive input for battery current sensing. Place R_{SENSE} between SRN and SRP for battery current sensing.
VBUS	A6, B6, C6, D6, E6, F6, G6	P	Device power input.
EN	D2	DI	Active high device enable. Pull low to disable device. ADC not available when device is disabled.
$\overline{\text{CHGSTAT}}$	E2	DI	Open drain, active low battery switch indicator. Connect to pull-up voltage via 10-kΩ pull-up resistor. This pin will assert low if battery switch is enabled and will go high when battery switch is disabled (due to fault or charge disabled or POR event).
$\overline{\text{INT}}$	C2	DO	Open drain, active low interrupt output. Connect to pull-up voltage via 10-kΩ pull-up resistor. Normally low, the $\overline{\text{INT}}$ pin asserts low to report status and faults. Keep constant low until the host reads this register 0x03, 0x04.
SDA	C1	DIO	I^2C interface data. Connect to pull-up voltage via 1-kΩ pull-up resistor.
SCL	B1	DI	I^2C interface clock. Connect to pull-up voltage via 1-kΩ pull-up resistor.
NC	A1, A2	AO	Not connected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (EN = Low, or CHG_EN = '0')	–2	22	V
	VOUT (EN = Low, or CHG_EN = '0')	–0.3	7	V
	SRP, SRN, BATP, BATN	–0.3	7	V
	$\overline{INT}$, SDA, SCL, EN, $\overline{CHGSTAT}$	–0.3	7	V
	TS_BUS, TS_BAT	–0.3	5	V
Maximum voltage difference	SRP – SRN	–0.5	0.5	V
	VOUT– VBUS	–22	7	V
Output sink current	$\overline{INT}$		6	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBUS	EN = high, or CHG_EN = '1'	2.8		6	V
VOUT	EN = high, or CHG_EN = '1'	2.8		6	V
BATP, BATN		0		6	V
SRP – SRN	Differential voltage between SRP and SRN	–0.2		0.2	V
TS_BUS, TS_BAT	TS pin voltage range	0		3	V
SDA, SCL, ADDR, $\overline{INT}$, EN	TS pin voltage range	0		5	V
IOUT	Maximum current from VBUS to VOUT	–3		7	A
T_J	Operating junction temperature range	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq25871 YFF (DSBGA) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over operating ambient temperature range –40 °C ≤ T_A ≤ 85 °C. Typical values are for T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_OP}	VBUS operation quiescent current	ADC disabled (ADC_EN = 0), charge disabled (CHG_EN = 0), EN = low, V_{VBUS}= 3.6 V, VOUT floating, current into VBUS		100	125	µA
		ADC enabled (ADC_EN = 1), charge disabled (CHG_EN = 0), EN = high, V_{VBUS}= 3.6 V, VOUT floating, current into VBUS		1.75	2.0	mA
I_{Q_BAT}	Battery quiescent current	ADC disabled (ADC_EN = 0), charge disabled (CHG_EN = 0), EN = low, V_{VOUT} = 3.6 V, current into VOUT		20	30	µA
		ADC disabled (ADC_EN = 0), charge disabled (CHG_EN = 0), EN = high, V_{VOUT} = 3.6 V, current into VOUT		80	120	µA
		ADC enable (ADC_EN = 1), charge disabled (CHG_EN = 0), EN = high, V_{VOUT} = 3.6 V, current into VOUT		1.35	1.75	mA
RESISTANCE AND LEAKAGE						
R_{ON}	VBUS to VOUT resistance	V_{VBUS} = 3.6 V, T_A = 25 °C		13	16	mΩ
		V_{VBUS} = 3.6 V, –40 °C ≤ T_A ≤ 85 °C		13	22	mΩ
V_{VBUS_PD}	VBUS pull-down resistance	VBUS_PD_EN = '1'	0.5	1.0	1.35	kΩ
INTERNAL THRESHOLDS						
$V_{BUS\_PRESENT}$	Rising				2.8	V
	Falling hysteresis			120		mV
V_{BAT_INSERT}	Rising				2.8	V
	Falling hysteresis			120		mV
T_{SHUT}	Internal thermal shutdown- rising			150		°C
T_{SHUT_HYS}	TSHUT falling hysteresis			30		°C
I_{RCP}	Current from VOUT to VBUS	RCP_SET = '0'	0.10	0.25	0.40	A
		RCP_SET = '1'	2.75	3.00	3.25	A
I_{SCP}	Short circuit current from VBUS to VOUT			10		A
PROTECTION THRESHOLD and ACCURACY						
V_{DROP_OVP}	VDROP OVP range	VBUS – VOUT. Programmable range	0		1000	mV
	VDROP OVP step size	0 mV ≤ VDROP_OVP ≤ 640 mV		10		mV
		700 mV < VDROP_OVP ≤ 1000 mV		100		mV
	VDROP OVP comparator accuracy	VDROP_OVP = 80 mV	–8.0%		8.0%	
		VDROP_OVP = 160 mV	–5.0%		5.0%	
V_{DROP_ALM}	VDROP ALM range	VBUS – VOUT. Programmable range	0		1000	mV
	VDROP ALM step size	0 mV ≤ VDROP_OVP ≤ 640 mV		10		mV
		700 mV < VDROOP_OVP ≤ 1000 mV		100		mV
	VDROP ALM comparator accuracy	VDROP_ALM = 80 mV	–8.0%		8.0%	
		VDROP_ALM = 160 mV	–5.0%		5.0%	
	VDROP ALM falling hysteresis			10		mV

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over operating ambient temperature range –40 °C ≤ T_A ≤ 85 °C. Typical values are for T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_OVP}	VBUS OVP range	Programmable range	4.20		6.51	V
	VBUS OVP step size			30		mV
	VBUS OVP comparator accuracy	VBUS_OVP = 4.20 V	–1.25%		1.25%	
		VBUS_OVP = 4.50 V	–1.25%		1.25%	
		VBUS_OVP = 5.49 V	–1.25%		1.25%	
	VBUS OVP falling hysteresis	VBUS_OVP = 4.20 V		50		mV
I_{BUS_REG}	IBUS REG range	Programmable range	0		6.3	A
	IBUS REG step size			100		mA
	IBUS REG accuracy	IBUS_REG = 1.5 A, –40 °C ≤ T_A ≤ 85 °C	–20%		20%	
		IBUS_REG = 1.5 A, T_A = 25 °C	–10%		10%	
I_{BUS_OCP}	IBUS OCP range	Programmable range	0		7.5	A
	IBUS OCP step size			500		mA
	IBUS OCP comparator accuracy	IBUS_OCP = 1.5 A	–20%		20%	
I_{BAT_REG}	IBAT REG range	Programmable range	0		6.35	A
	IBAT REG step	R_{sense} = 10 mΩ		50		mA
	IBAT REG accuracy	IBAT_REG = 2 A, R_{sense} = 10 mΩ	–6.5%		6.5%	
		IBAT_REG = 5 A, R_{sense} = 10 mΩ	–4%		2%	
I_{BAT_OCP}	IBAT OCP rising threshold	Percentage of IBAT_REG threshold, IBAT_REG = 6 A		105%		
	IBAT OCP falling threshold	Percentage of IBAT_REG threshold, IBAT_REG = 6 A		102.5%		
V_{BAT_REG}	VBAT REG range	Programmable range	4.2		4.975	V
	VBAT REG step size			12.5		mV
	VBAT REG accuracy	VBAT_REG = 4.35 V	–1.5%		1.0%	
		VBAT_REG = 4.40 V	–1.5%		1.0%	
V_{BAT_OVP}	VBAT OVP rising threshold	Percentage of VBAT_REG threshold, VBAT_REG = 4.40 V		104%		
	VBAT OVP falling threshold	Percentage of VBAT_REG threshold, VBAT_REG = 4.40 V		102%		
V_{OUT_REG}	VOUT REG range	Programmable range	4.2		4.975	V
	VOUT REG step size			25		mV
	VOUT REG accuracy	VOUT_REG = 4.35 V	–0.5%		0.5%	
		VOUT_REG = 4.40 V	–0.5%		0.5%	
V_{OUT_OVP}	VOUT OVP rising threshold	Percentage of VOUT_REG threshold, VOUT_REG = 4.40 V		104%		
	VOUT OVP falling threshold	Percentage of VOUT_REG threshold, VOUT_REG = 4.40 V		102%		
TS_{BUS_FLT}	TS_BUS pin voltage range	Programmable range	0.2		1.4	V
	TS_BUS step size			25		mV
	TS_BUS comparator accuracy	TS_BUS = 0.4 V	–4.0%		4.0%	
		TS_BUS = 0.7 V	–4.0%		4.0%	
	TS_BUS hysteresis			1%		

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over operating ambient temperature range –40 °C ≤ T_A ≤ 85 °C. Typical values are for T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{BAT_FLT}	TS_BAT pin voltage range	Programmable range	0.2		1.4	V
	TS_BAT step size			25		mV
	TS_BAT comparator accuracy	TS_BAT = 0.4 V	–2.5%		2.5%	
		TS_BAT = 0.6 V	–2.5%		2.5%	
	TS_BAT hysteresis			1%		

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over operating ambient temperature range –40 °C ≤ T_A ≤ 85 °C. Typical values are for T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTEGRATED ADC: temperature range: 0°C ≤ T_A ≤ 85°C						
ADC_{RES}	Resolution				10	bits
t_{ADC_CONV}	ADC individual measurement and conversion time			30		µs
t_{ADC_INT}	ADC samples interval in averaging mode			300		µs
$RANGE_{IBAT}$	IBAT current measurement range		0		7.504	A
RES_{IBAT}	IBAT current LSB			8		mA
ACC_{IBAT}	IBAT accuracy	IBAT = 6 A	–2%		2%	
$RANGE_{IBUS}$	IBUS current measurement range		0		7.504	A
RES_{IBUS}	IBUS current LSB			8		mA
ACC_{IBUS}	IBUS accuracy	IBUS = 1.6 A	–5%		5%	
ACC_{IBUS}	IBUS accuracy	IBUS = 5 A	–4.5%		4.5%	
$RANGE_{VBUS}$	VBUS voltage measurement range		2.048		6.140	V
RES_{VBUS}	VBUS voltage LSB			4		mV
ACC_{VBUS}	VBUS accuracy	VBUS = 4.5 V	–20		20	mV
$RANGE_{VBAT}$	VBAT voltage measurement range		2.048		6.140	V
RES_{VBAT}	VBAT voltage LSB			4		mV
ACC_{VBAT}	VBAT accuracy	VBAT = 4.4 V	-12		12	mV
$RANGE_{VOUT}$	VOUT voltage measurement range		2.048		6.140	V
RES_{VOUT}	VOUT voltage LSB			4		mV
ACC_{VOUT}	VOUT accuracy	VOUT = 4.4 V	-12		12	mV
$RANGE_{VDROP}$	VDROP voltage measurement range		0		1000	mV
RES_{VDROP}	VDROP voltage LSB			1		mV
ACC_{VDROP}	VDROP accuracy	VDROP = 200 mV	-10		10	mV
$RANGE_{TS\_BUS}$	TS_BUS voltage measurement range		0		2.420	V
RES_{TS_BUS}	TS_BUS voltage LSB			4		mV
ACC_{TS_BUS}	TS_BUS accuracy	TS_BUS = 400 mV	-13.4		13.4	mV
$RANGE_{TS\_BAT}$	TS_BAT voltage measurement range		0		2.420	V
RES_{TS_BAT}	TS_BAT voltage LSB			4		mV
ACC_{TS_BAT}	TS_BAT accuracy	TS_BAT = 400 mV	-13.4		13.4	mV

Electrical Characteristics (continued)

Unless otherwise noted, the specification in the following table applies over operating ambient temperature range –40 °C ≤ T_A ≤ 85 °C. Typical values are for T_A = 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC I/O THRESHOLD (EN, $\overline{INT}$, ADDR)						
V_{IL}	Input low threshold level	I_{SINK} = 5 mA			0.4	V
V_{IH}	Input high threshold level	I_{SINK} = 5 mA	1.3			V
I_{LEAK} ($\overline{INT}$)	High level leakage current	$V_{PULL-UP}$ = 3.3 V			5	µA
I_{LEAK} ($\overline{CHGSTAT}$)	High level leakage current	$V_{PULL-UP}$ = 3.3 V			5	µA
I_{LEAK} (EN)	High level leakage current	$V_{PULL-UP}$ = 3.3 V			10	µA
I^2C TIMINGS						
V_{IL}	Input low threshold level	$V_{PULL-UP}$ = 1.8 V, SDA and SCL			0.4	V
V_{IH}	Input high threshold level	$V_{PULL-UP}$ = 1.8 V, SDA and SCL	1.3			V
V_{OL}	Output low threshold level	I_{OL} = 20 mA			0.4	V
I_{BIAS}	High-level leakage current	$V_{PULL-UP}$ = 1.8 V, SDA and SCL			5	µA
f_{SCL}	SCL clock frequency				1	MHz

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
PROTECTION						
OSC	Oscillator frequency		1.8	2	2.4	MHz
t_{VBUS_OVP}	VBUS OVP deglitch time, VBUS_OVP_DLY = 0			8		µs
t_{VBUS_OVP}	VBUS OVP deglitch time, VBUS_OVP_DLY = 1			128		µs
$t_{IBUS\_OCP\_BLANK}$	IBUS OCP deglitch time, OCP_RES = 0			8		µs
t_{IBUS_OCP}	IBUS OCP deglitch time in hiccup mode, OCP_RES = 1			8		µs
$t_{IBUS\_OCP\_HP}$	Retry wait time for IBUS OCP in hiccup mode, OCP_RES = 1			100		ms
$t_{IBUS\_OCP\_RST}$	Hiccup count reset timer			400		ms
t_{IBAT_OCP}	IBAT OCP deglitch time			512		µs
t_{VDROP_OVP}	VDROP deglitch time			64		µs
t_{VBAT_OVP}	VBAT OVP deglitch time			64		µs
t_{VOUT_OVP}	VOUT OVP deglitch time			64		µs
t_{LDO_RES}	LDO response time for IBUS, IBAT, VBAT, VOUT			1		ms
t_{LDO_ACTIVE}	LDO active signal deglitch time			128		µs
T_{TS_OTP}	TS_BAT and TS_BUS deglitch time			100		ms
t_{IREV}	Reverse current protection (RCP) deglitch time			8		µs
t_{SCP}	Short circuit protection (RCP) deglitch time			2		µs
t_{ON_VOUT}	VOUT soft-start rise time			0.5		ms
t_{OFF_FET}	Battery switch turn off time			1		µs
t_{WTDG}	Watchdog timer	WATCHDOG[3:2] = 01		0.5		s
		WATCHDOG[3:2] = 10		1		s
		WATCHDOG[3:2] = 11		2		s

7 Typical Characteristics

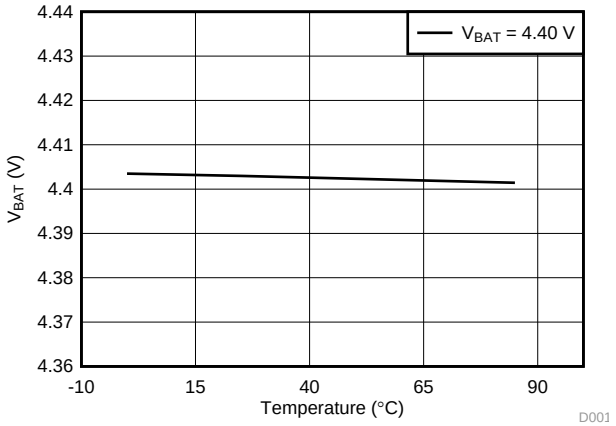


Figure 1. VBAT ADC vs Temperature at 4.4 V

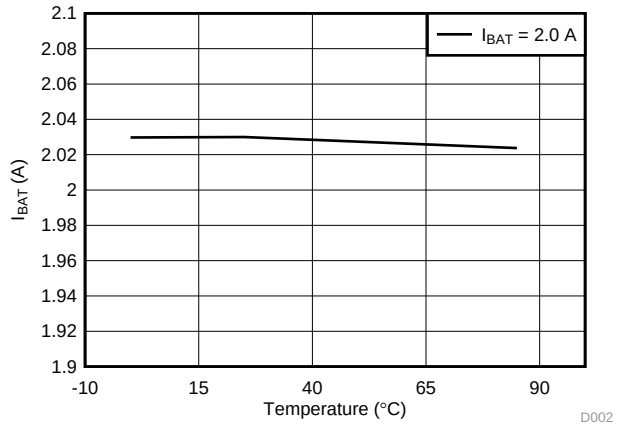


Figure 2. IBAT ADC vs Temperature at 2 A

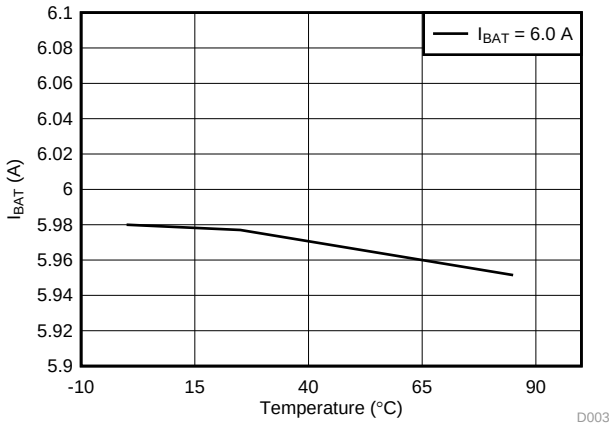


Figure 3. IBAT ADC vs Temperature at 6 A

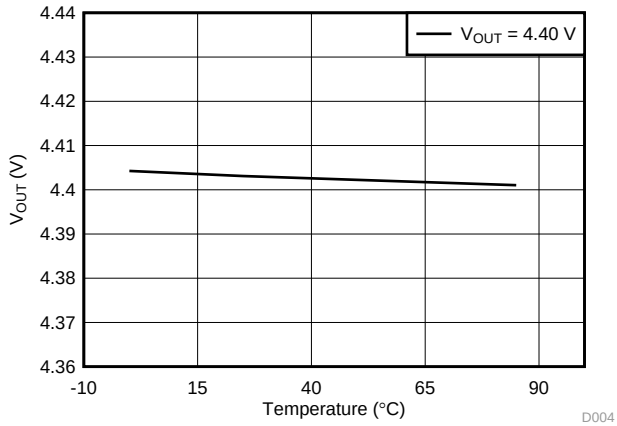


Figure 4. VOUT ADC vs Temperature at 4.4 V

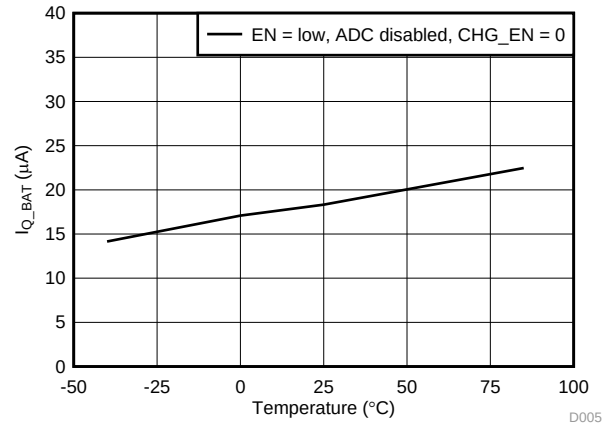


Figure 5. Quiescent Current with Battery Only vs Temperature

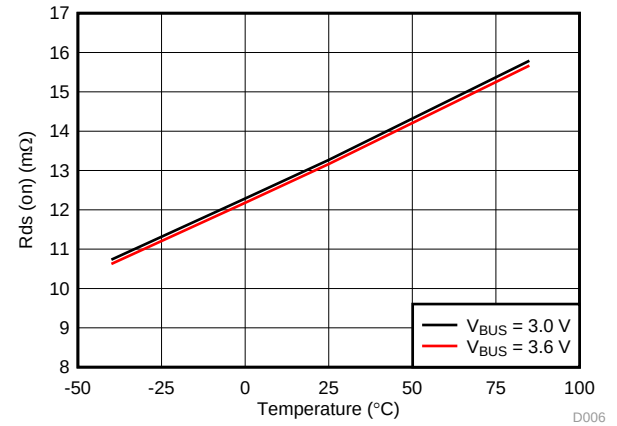


Figure 6. R_{dson} vs Temperature

Typical Characteristics (continued)

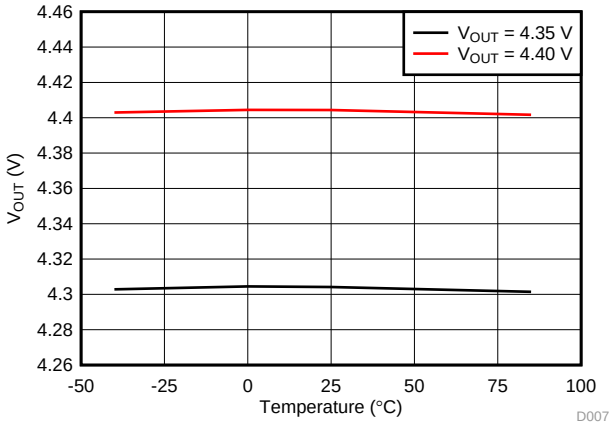


Figure 7. VOUT Regulation vs Temperature

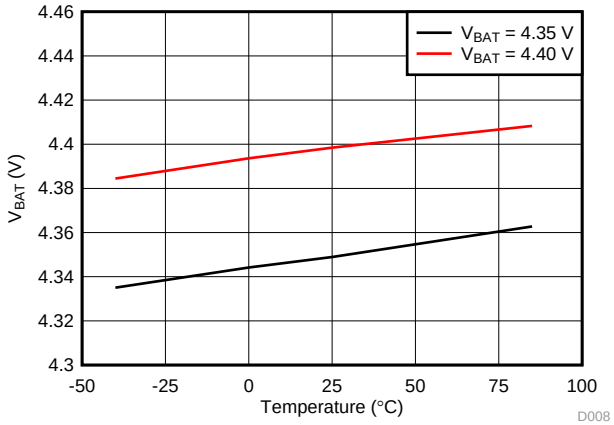


Figure 8. VBAT Regulation vs Temperature

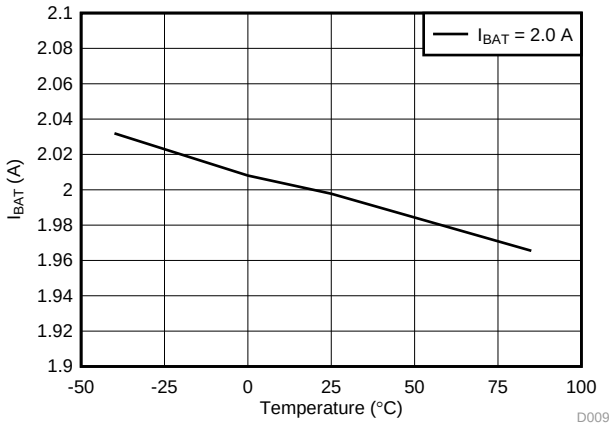


Figure 9. IBAT Regulation vs Temperature at 2 A

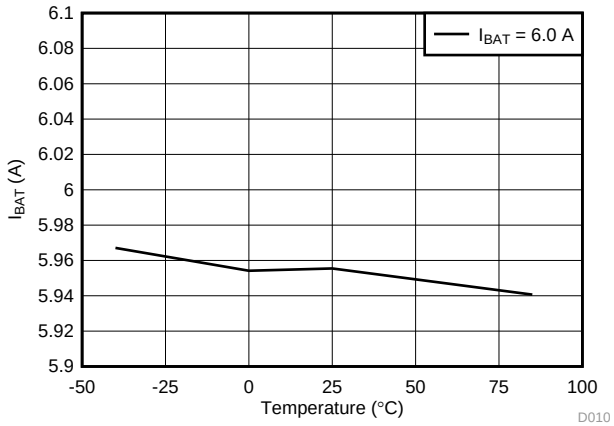


Figure 10. IBAT Regulation vs Temperature at 6 A

8 Detailed Description

8.1 Overview

The bq25871 is an I²C controlled device and a single cell Li-Ion battery charger. The device allows 7-A charging current with 13-mΩ MOSFETs for minimum power loss. A 10 -bit ADC, four linear regulation loops and multiple OVP and OCP are integrated for host monitoring and safe operation of the device.

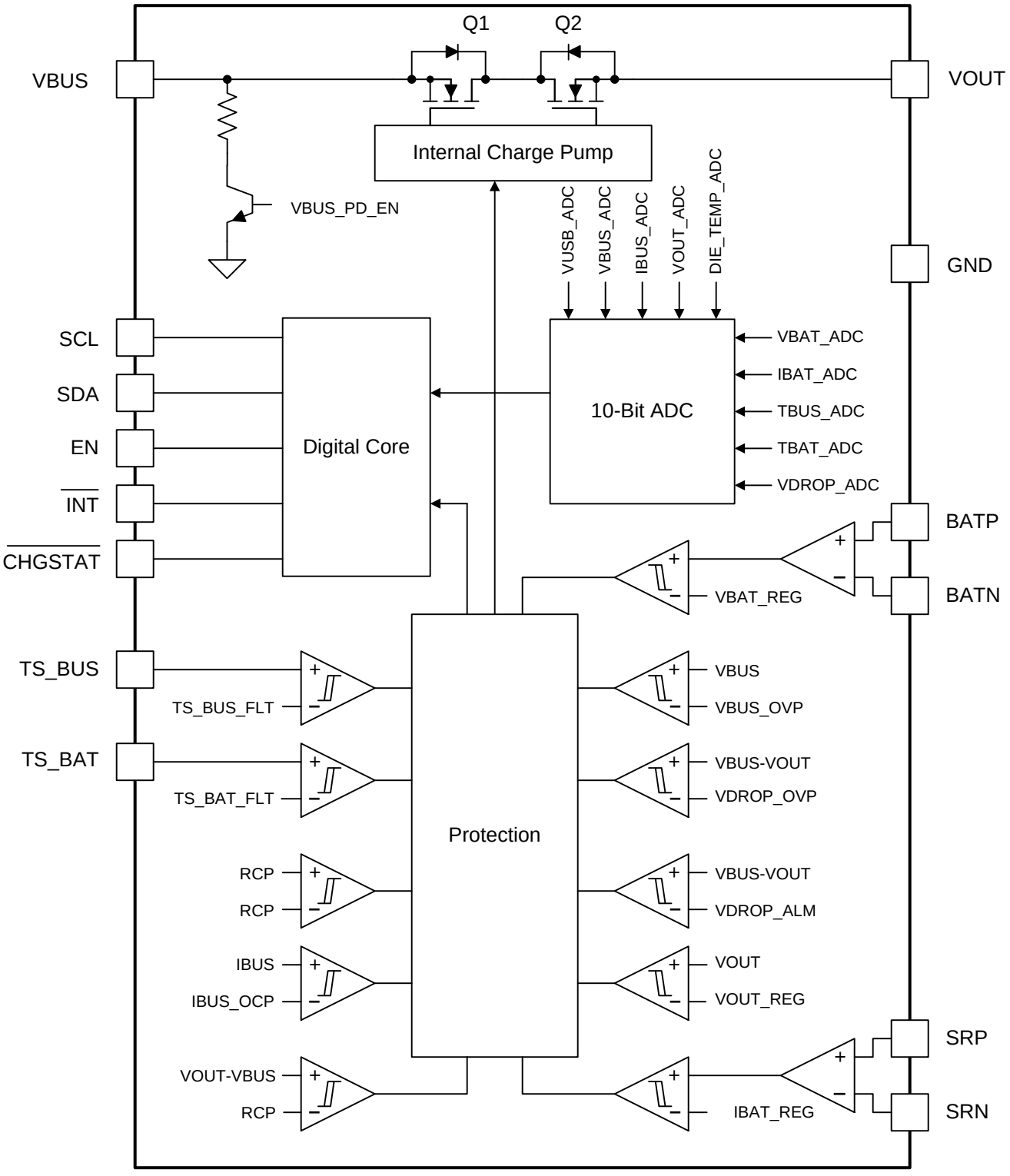
8.1.1 Device Protection Overview

The following table summarizes the protection features implemented in the device.

Table 1. Protection Features Overview

PROTECTION NAME	DESCRIPTION	RESPOND
VBUS_OVP	Monitors VBUS voltage and compares to the threshold programmed in REG 0A	Turn off load switch after a deglitch time of t_{VBUS_OVP}
VOUT_REG	Monitors VOUT voltage and compares to the threshold programmed in REG 0B	Enable linear regulation of battery switch within a response time of t_{LDO_RES}
VOUT_OVP	Monitors VOUT voltage and compares to 1.04 times of the threshold programmed in REG 0B	Turn off load switch after a deglitch time of t_{VOUT_OVP}
VDROP_OVP	Monitors voltage difference between VBUS and VOUT (VBUS – VOUT) and compares to the threshold programmed in REG 0C	Turn off load switch after a deglitch time of t_{VDROP_OVP}
VDROP_ALM	Monitors voltage difference between VBUS and VOUT (VBUS – VOUT) and compares to the threshold programmed in REG 0D	$\overline{INT}$ is asserted low to alert host
VBAT_REG	Monitors VBAT voltage and compares to the threshold programmed in REG 0E	Enable linear regulation of battery switch within a response time of t_{LDO_RES}
VBAT_OVP	Monitors VBAT voltage and compares to 1.04 times of the threshold programmed in REG 0E	Turn off load switch after a deglitch time of t_{VBAT_OVP}
IBAT_REG	Monitors battery current measured by sensing resistor and compares to the threshold programmed in REG 0F	Enable linear regulation of battery switch within a response time of t_{LDO_RES}
IBAT_OCP	Monitors VBAT voltage and compares to 1.05 times of the threshold programmed in REG 0E	Turn off load switch after a deglitch time of t_{VBAT_OVP}
IBUS_OCP	Monitors input current and compares to the threshold programmed in REG 09	Turn off load switch after a deglitch time of t_{IBUS_OCP}
IBUS_REG	Monitors input current and compares to the threshold programmed in REG 10	Enable linear regulation of battery switch within a response time of t_{LDO_RES}
IBUS_RCP	Monitors current flowing from battery to adaptor and compares to the threshold selected in REG 06	Turn off load switch after a deglitch time of t_{IBUS_RCP}
TS_BUS_OTP	Monitors temperature based on voltage measured by a negative temperature coefficient (NTC) resistor at VBUS and compares to the threshold programmed in REG 11	Turn off load switch after a deglitch time of t_{TS_OTP}
TS_BAT_OTP	Monitors temperature based on voltage measured by a negative temperature coefficient (NTC) resistor at battery and compares to the threshold programmed in REG 12	Turn off load switch after a deglitch time of t_{TS_OTP}

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power Up

The internal bias circuits of the device are powered from higher of the two voltages between VBUS and VOUT as long as one of the pins is above its respective PRESENT threshold ($VBUS_{PRESENT}$, or $VOUT_{PRESENT}$) . Once either V_{VBUS} > $VBUS_{PRESENT}$, or V_{VOUT} > $VOUT_{PRESENT}$ is qualified, the device is considered to have a valid power supply. However, the device will begin to draw current from VBUS or VOUT (depending upon which supply is present) once either supply is above its respective UVLO threshold.

8.3.2 Battery Switch (Q1 + Q2)

The device contains an integrated 13mΩ battery switch that is capable of handling up to 7 A of current. This battery switch can be controlled by the host via CHG_EN I^2C bit. The device can be disabled, including the battery switch and the I^2C core, by pulling the EN pin low. To turn on the battery switch charger for conduction, the EN pin must be pulled high, CHG_EN bit must be set to '1', and no fault conditions must be present (unless they have been disabled in EVENT_1_EN register). See EVENT_1 and EVENT_2 registers for a list of faults/events. In the event of a fault/event, the battery switch will be automatically disabled, and the host will be notified via the $\overline{INT}$ for error reporting if the corresponding event bit is unmasked in the EVENT_x_MASK registers.

In order to ensure that the IBUS OCP threshold is not falsely tripped during turn-on of the battery switch, the device employs a soft-start scheme where the battery switch is slowly turned to minimize the inrush current. The rise time of VOUT is t_{ON_VOUT}.

8.3.3 Integrated 10-bit ADC for Monitoring

With the integrated 10-bit ADC of the device, the user application can monitor , the voltage and current of VBUS, voltage of VOUT , and the voltage and current of the battery. The ADC is also used for temperature reporting of the internal junction temperature, battery temperature (via external resistor divider and NTC thermistor), and VBUS connector temperature (via external resistor divider and NTC thermistor). The integrated ADC has a conversion time of t_{ADC_CONV} for each parameter (except IBAT_ADC which has conversion time of 2 x t_{ADC_CONV}). The total conversion time of all parameters (in 1-shot mode) is between 80 µs and 140 µs. The rate at which the ADC output registers are updated depends on the settings of ADC_AVG_EN, ADC_SAMPLES, and the parameter conversions that have been enabled in the ADC_MASK register.

To enable the ADC, the ADC_EN bit must be set to '1'. The ADC is allowed to operate if either V_{VBUS} > $VBUS_{PRESENT}$ or V_{VOUT} > $VOUT_{PRESENT}$ is valid. If ADC_EN is set to '1' before VBUS or VOUT reach their respective PRESENT threshold, then ADC conversion will be postponed until one of the power supplies reaches their respective PRESENT threshold. If EN pin is asserted low, then ADC conversion is not allowed.

The integrated ADC has two conversion rate options – 1-shot conversion (only one conversion) and continuous conversion (back-to-back conversions). To select the appropriate conversion rate, the ADC_RATE bit must be set accordingly ('0' for 1-shot, '1' for continuous). If ADC_AVG_EN is set to '0', the ADC will convert instantaneous measurements. If ADC_AVG_EN is set to '1', the average measurement of a parameter (in both continuous and 1-shot mode) will be determined by the setting of ADC_SAMPLES. If the user reads the output registers before the ADC averaging is complete, then the read-back value would be unchanged from the previous converted measurement. However, the value in the register will not change during the read-back of the register(s). If the measured signal is outside of the range of the ADC output register in question, the reported value in the ADC will be clamped to the min/max of the range specified. When ADC_EN is changed from 1 to 0, the ADC registers will maintain their values from the previous converted measurement.

Feature Description (continued)

The user application has the option of selecting which parameters (voltage, current, temperature) the ADC needs to convert when the ADC is set to continuous conversion mode (ADC_RATE is set to '1') or in 1-shot mode (ADC_RATE is set to '0'). By default, all parameters (IBUS_ADC, VBUS_ADC, IBAT_ADC, VBAT_ADC, VOUT_ADC, VDROP_ADC, TBUS_ADC, TBAT_ADC, TDIE_ADC) will be converted in 1-shot and continuous conversion mode unless disabled in the ADC_MASK register. If an ADC parameter is masked (by setting the corresponding bit in the ADC_MASK_x register), then the value in that register will be from the last valid ADC conversion or the default POR value (which is all zeros if no conversions have taken place). If an ADC parameter is masked in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter in the current conversion cycle and will not convert that parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are masked off, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC_MASK register is set to '0'.

The ADC_DONE bit signals when a 1-shot mode conversion is completed. During continuous conversion mode, this bit is always set to '0'.

The ADC_EN bit controls when the ADC is enabled for a conversion. Upon enabling the ADC, the ADC conversion will follow the settings in ADC_AVG_EN, ADC_SAMPLE, and ADC_RATE.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (that causes the battery switch to be disabled), and the host must set ADC_EN = '0' to disable ADC.

ADC readings are only valid for DC states of the signals, not for transients.

8.3.4 Linear Regulation Mode (LDO)

The device employs LDO mode that helps regulate VOUT voltage, battery voltage, input current and battery current. In an event that the VOUT_REG, VBAT_REG, IBUS_REG or IBAT_REG threshold is exceeded, the battery switch will act as an LDO and will regulate VOUT, VBAT, IBUS and IBAT (depending upon which threshold is exceeded). The purpose of LDO mode is to provide temporary protection until the host is able to read the EVENT_x registers (upon $\overline{INT}$ trigger), ADC output registers, and then update the adapter voltage accordingly.

When VOUT_REG, VBAT_REG, or IBAT_REG threshold is exceeded, the response time of the LDO will be 1ms. Depending upon which LDO mode event occurs, the corresponding bit (VBAT_REG_LDO, IBAT_REG_LDO, VOUT_REG_LDO) will be set in EVENT_1 register and $\overline{INT}$ will be asserted low to alert the host (if the corresponding bit is not masked in EVENT_1_MASK register).

Feature Description (continued)

8.3.5 Protection Features

The device contains various protection features that are active depending upon the states of various inputs:

- If V_{VBUS} > $VBUS_{PRESENT}$, V_{VOUT} > $VOUT_{PRESENT}$, EN asserted high, and CHG_EN = '1'
  - Active protection: VBUS_OVP, IBUS_OCP, VOUT_OVP, VBAT_OVP, IBAT_OCP, SCP, RCP, VDROP_OVP
- If V_{VBUS} > $VBUS_{PRESENT}$, V_{VOUT} > $VOUT_{PRESENT}$, EN asserted high, and CHG_EN = '0'
  - Active protection: VBUS_OVP, IBUS_OCP, VOUT_OVP, IBAT_OCP, SCP, RCP, VDROP_OVP
  - VBAT_OVP active until VBAT OVP condition is over (protection becomes inactive on falling threshold of VBAT_OVP, which is 102% of VBAT_REG setting)

Tripping any of these protection faults will cause the battery switch to be disabled (unless the protection is disabled in EVENT_1_EN and EVENT_2_EN registers) and an interrupt to be issued on the $\overline{INT}$ pin (see $\overline{INT}$ Pin, EVENT_x Registers, EVENT_x_MASK Registers section for details of when $\overline{INT}$ is toggled).

8.3.5.1 Reverse Current Protection (RCP)

The device monitors the current flow from VBUS to VOUT to ensure there is no reverse current (current flow from VOUT to VBUS). In an event that a reverse current flow is detected, the battery switch is disabled within t_{OFF_FET} after a deglitch time of t_{IREV} and CHG_EN is set to '0'. Host intervention is required to set CHG_EN to '1' to enable the power switch again. The RCP threshold is set by the RCP_SET bit.

Reverse current protection is always active when the device has valid power. The RCP threshold is based on the RCP_SET bit setting in the CONTROL register. It has a response delay of t_{IREV}. When RCP is tripped, IBUS_IREV_FLT bit in the EVENT_1 register is set to '1', and $\overline{INT}$ is asserted low to alert the host (unless masked by IBUS_IREV_MASK).

8.3.5.2 Internal Thermal Shutdown

The device monitors the die junction temperature and the battery switch is disabled when device junction temperature reaches TSHUT within t_{OFF_FET} and CHG_EN is set to '0' . When the internal thermal shutdown is triggered, $\overline{INT}$ is asserted low to alert the host, and the device temperature must drop by TSHUT_HYS before the battery switch can be enabled again (host must enable battery switch). While the TSHUT condition persists (and before the junction temperature dropped by TSHUT_HYS), all other functions are unaffected.

If the DIE_TEMP_FLT threshold has been crossed, TSHUT_FLT bit in EVENT_2 register is set to '1', and $\overline{INT}$ will assert low to alert the host (no mask bit for TSHUT_FLT). After the TSHUT_FLT is cleared by the host with a register read, it is possible the TSHUT_FLT bit is set again if the die junction temperature has not reduced by TSHUT_HYS.

DIE_TEMP_FLT allows the user to select TSHUT thresholds between different junction temperatures as the thermal shutdown point. DIE_TEMP_ADC is the die (junction) temperature of the device that is measured via the 10-bit ADC.

The ADC measurement (DIE_TEMP_ADC) is independent of the TSHUT fault that triggers TSHUT_FLT in the EVENT_x register. Therefore, it is possible to have the ADC output value be a higher value that the DIE_TEMP_FLT threshold, while the TSHUT fault has not yet been triggered.

Feature Description (continued)

8.3.5.3 IBUS and VBUS Protection

Over-current protection on VBUS (IBUS_OCP) monitors the current flow from VBUS to VOUT pins. IBUS_OCP protection is always active when the battery switch is enabled, and the protection has a deglitch time that depends on the OCP_RES setting as described below.

If OCP_RES = '0' (blanking mode), the device will wait $t_{IBUS\_OCP\_BLANK}$ before disabling the battery switch within t_{OFF_FET} and setting CHG_EN to '0'. When the battery switch is disabled, IBUS_OCP_FLT is set to '1'. If during the $t_{IBUS\_OCP\_BLANK}$ duration a short circuit protection scenario occurs, then the device will follow the behavior as listed in short circuit protection (SCP). Once the battery switch is disabled, CHG_EN is set to '0' and host intervention is required to set CHG_EN to '1' to enable the battery switch again.

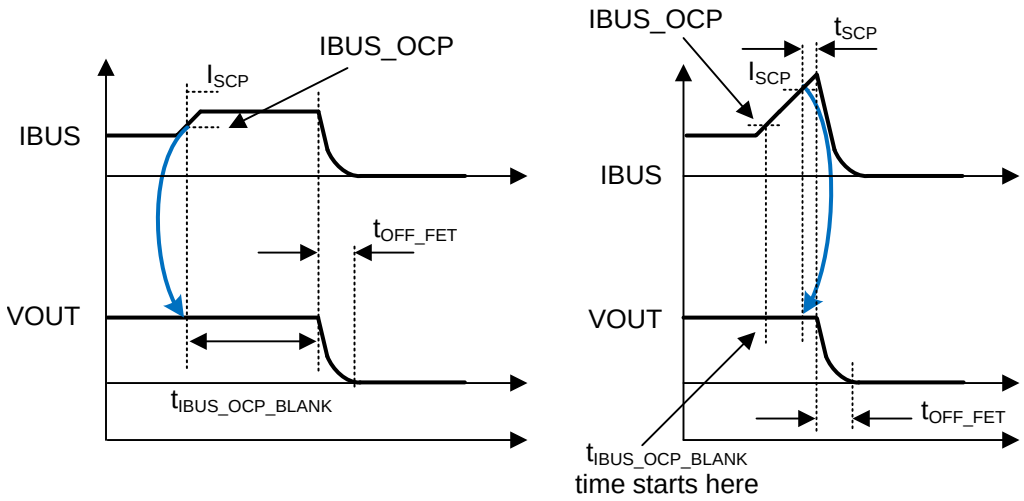


Figure 11. IBUS OCP and SCP

Feature Description (continued)

If OCP_RES = '1' (hiccup mode), the device will turn off the battery switch within t_{IBUS_OCP} and will attempt to turn on the battery switch every $t_{IBUS\_OCP\_HP}$, up to seven times before latching off the battery switch. Upon latching off after the seventh try, IBUS_OCP_FLT is set to '1'. Once the battery switch is latched off, CHG_EN is set to '0' and host intervention is required to set CHG_EN to '1' to enable the battery switch again.

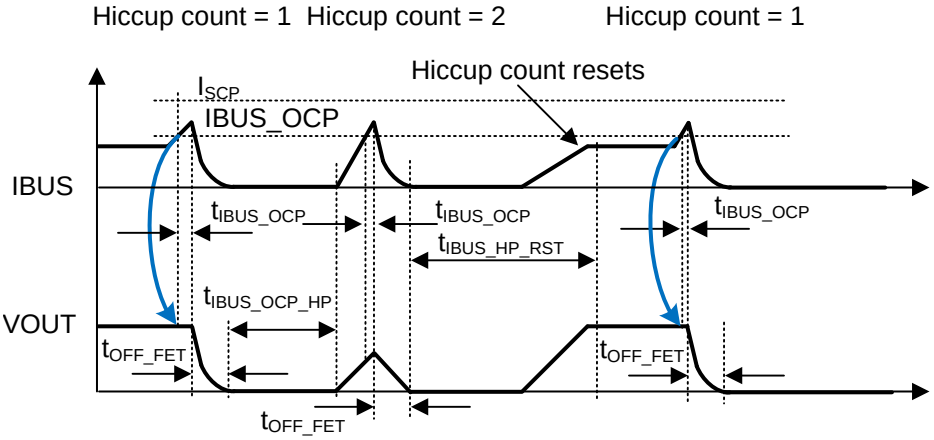


Figure 12. IBUS OCP in Hiccup Mode

VBUS over-voltage protection (VBUS_OVP) monitors the voltage on VBUS. VBUS_OVP protection is always active when the device voltage is above at least one PRESENT level (VBUS or VOUT), and the protection has a selectable deglitch time set by VBUS_OVP_DLY. When VBUS_OVP threshold is reached, the battery switch is turned off in t_{VBUS_OVP} and latched off. If the VBUS_OVP or IBUS_OCP value written to the register is greater than the max defined value for the register, then the corresponding register will be set to the highest defined value.

If a threshold has been crossed (IBUS_OCP or VBUS_OVP), the appropriate bit in the EVENT_1 register is updated (set to '1' if threshold is crossed, '0' if threshold is not crossed). If the EVENT_1_MASK bit is not set to '1' for the corresponding bit in the EVENT_1 register, then $\overline{INT}$ will assert low to alert the host of a fault.

Feature Description (continued)

8.3.5.4 IBAT and VBAT Protection

The device monitors current through the battery by monitoring the voltage across the external, series battery sense resistor. The differential voltage of this sense resistor is measured on SRP and SRN. A 10-mΩ series resistor is recommended for battery current monitoring. A lower resistor value can be used, but it will result in lower measurement accuracy. A higher resistor value can be used, but it will result in decreased charging efficiency.

When the IBAT_REG threshold is reached, the device will go into LDO mode to regulate the battery current at the IBAT_REG threshold. See LDO mode section for more details about the device operation during LDO mode. If the IBAT_OCP threshold is reached and IBAT_OCP protection has been enabled, the battery switch will be disabled within t_{OFF_FET} after a deglitch time of t_{IBAT_OCP} and CHG_EN is set to '0'. Host intervention is required to set CHG_EN to '1' to enable the battery switch again.

The device monitors battery voltage by measuring the differential voltage on BATP and BATN pins. When the VBAT_REG threshold is reached, the device will go into LDO mode to regulate the battery voltage at the VBAT_REG threshold. See LDO mode section for more details about the device operation during LDO mode. If the VBAT_OVP threshold is reached and VBAT_OVP protection is enabled, the battery switch will be disabled within t_{OFF_FET} after a deglitch time of t_{VBAT_OVP} and CHG_EN is set to '0'. Host intervention is required to set CHG_EN to '1' to enable the battery switch again. If the VBAT_REG or IBAT_REG value written to the register is greater than the max defined value for the register, then the corresponding register will be set to the highest defined value.

If a threshold has been reached (IBAT_REG, VBAT_REG, IBAT_OCP or VBAT_OVP), the appropriate bit in the EVENT_x register is updated (set to '1' if threshold is crossed, '0' if threshold is not crossed). If the EVENT_x_MASK bit is not set to '1' for the corresponding bit in the EVENT_x register, then $\overline{INT}$ will assert low to alert the host of a fault.

8.3.5.5 VOUT Protection

The device monitors voltage on VOUT when the device has a valid power supply. When the VOUT_REG threshold is reached, the device will go into LDO mode to regulate the VOUT voltage at the VOUT_REG threshold. See LDO mode section for more details about the device operation during LDO mode. If the VOUT_OVP threshold is reached and VOUT_OVP protection is enabled, the battery switch will be disabled within t_{OFF_FET} after a deglitch time of t_{VOUT_OVP} and CHG_EN is set to '0'. Host intervention is required to set CHG_EN to '1' to enable the battery switch again. If the VOUT_REG value written to the register is greater than the max defined value for the register, then VOUT_REG will be set to the highest defined value for the register.

If a threshold has been reached (VOUT_REG or VOUT_OVP), the appropriate bit in the EVENT_1 register is updated (set to '1' if threshold is crossed, '0' if threshold is not crossed). If the EVENT_x_MASK bit is not set to '1' for the corresponding bit in the EVENT_x register, then $\overline{INT}$ will assert low to alert the host of a fault.

Feature Description (continued)

8.3.5.6 VDROP Protection

VDROP is the voltage difference from VBUS to VOUT and can be used to monitor the health of MOSFET and power loss of the device. There are two VDROP thresholds, VDROP alarm (VDROP_ALM) and VDROP fault (VDROP_FLT). VDROP_ALM is an indicator (via I^2C register bit and $\overline{INT}$) to alert the host that the voltage differential between VBUS and VOUT is higher than normal, and that the host to should take action to reduce this drop. VDROP_OVP is a fault threshold that results in the battery switch being disabled within t_{OFF_FET} after a deglitch time of t_{VDROP_OVP} and CHG_EN set to '0' when VDROP_OVP protection is enabled. Host intervention is required to set CHG_EN to '1' to enable the battery switch again. If the VDROP_OVP or VDROP_ALM value written to the register is greater than the max defined value for the register, then the corresponding register will be set to the highest defined value.

If a threshold has been reached (VDROP_ALM or VDROP_OVP), the appropriate bit in the EVENT_1 register is updated (set to '1' if threshold is crossed, '0' if threshold is not crossed). If the EVENT_x_MASK bit is not set to '1' for the corresponding bit in the EVENT_x register, then $\overline{INT}$ will assert low to alert the host of a fault.

VDROP_ALM does not affect the state of the battery switch and only causes $\overline{INT}$ to assert low when the threshold is crossed. VDROP_OVP does turn off the battery switch and causes $\overline{INT}$ to assert low if this threshold is crossed. Therefore, if VDROP_ALM threshold is set higher than the VDROP_OVP threshold accidentally (user error), then VDROP_ALM functionality is never triggered since VDROP_OVP threshold will turn off the battery switch and assert $\overline{INT}$ low.

NOTE

The threshold of VDROP_OVP and VDROP_ALM is around 13 mV lower than the actual setting when VDROP ADC is enabled.

8.3.5.7 VBUS Temperature (TS_BUS_FLT) and Battery Temperature (TS_BAT_FLT)

TBUS_OTP and TBAT_OTP protection is active whenever the device has a valid power supply. The purpose of VBUS temperature is to have connector temperature monitor to improve user experience. TS_BUS and TS_BAT both rely on a resistor divider that has an external pull-up voltage. Internally, the TS_BUS and TS_BAT pins are clamped to 2.42 V. Place a negative coefficient thermistor in parallel to the low-side resistor. A fault on the TS_BUS and TS_BAT pin is triggered on the falling edge of the voltage threshold (signifying a "hot" temperature).

If the TBUS_OTP or TBAT_OTP threshold is reached, the battery switch will be disabled within t_{OFF_FET} after a deglitch time of t_{TS_OTP} and CHG_EN is set to '0'. Host intervention is required to set CHG_EN to '1' to enable the battery switch again. If the TS_BUS_FLT or TS_BAT_FLT value written to the register is greater than the max defined value for the register, then the corresponding register will be set to the highest defined value.

For TS_BUS_FLT and TS_BAT_FLT, if a threshold has been crossed, the appropriate bit in the EVENT_x register is updated (set to '1' if threshold is crossed, '0' if threshold is not crossed). If the EVENT_x_MASK bit is not set to '1' for the corresponding bit in the EVENT_1 register, then $\overline{INT}$ will toggle to alert the host of a fault.

NOTE

TS_BUS_FLT will not trip when TS_BUS ADC is enabled.

Feature Description (continued)

8.3.6 I²C Serial Interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²C communication to the device is available as long as V_{VBUS} > $VBUS_{UVLO}$or V_{VOUT} > $VOUT_{UVLO}$. I²C™ is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required, a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address set by the ADDR pin. The device receives control inputs from the master device like micro controller or a digital signal processor through REG00-REG29 and REG40. Register read between REG29 and REG39 beyond REG40 returns 0xFF. The I²C interface supports standard mode (up to 100 kbit/s), fast mode (up to 400 kbit/s), and fast mode plus (up to 1 Mbit/s). Connect the SDA and SCL pins to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The SDA and SCL pins are open drain.

The device supports 7-bit addressing. The 8th bit will change depending upon the command (read or write) that is issued. The device's 7-bit address is defined as shown in the image below.

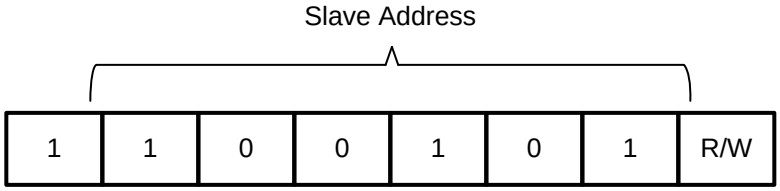


Figure 13. Slave Address

8.3.6.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

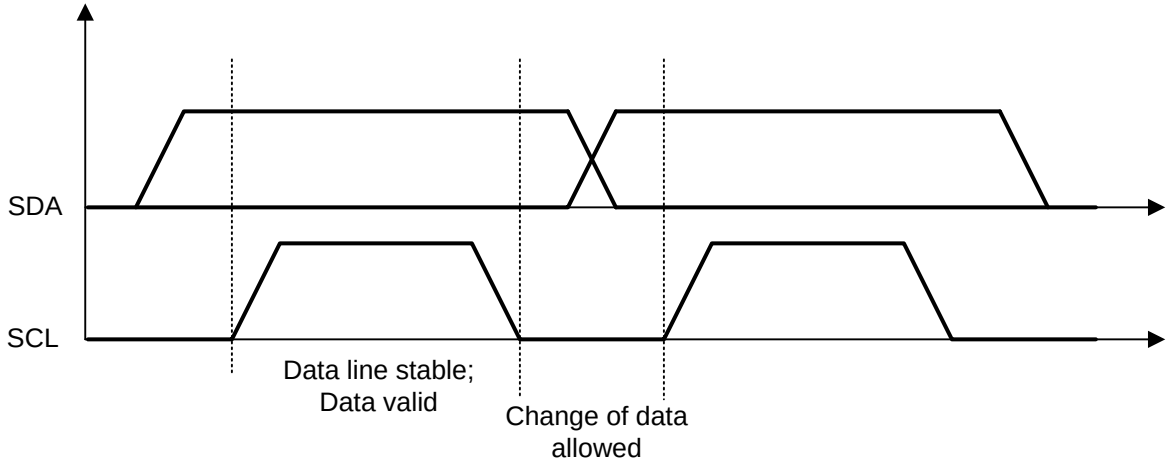


Figure 14. Bit Transfer on the I²C Bus

Feature Description (continued)

8.3.6.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

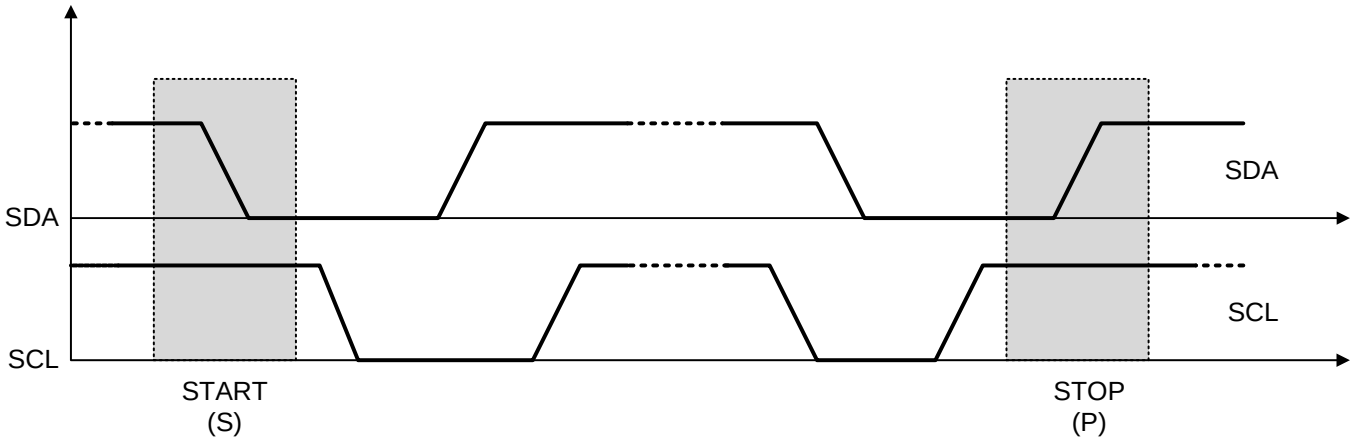


Figure 15. START and STOP Conditions

8.3.6.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

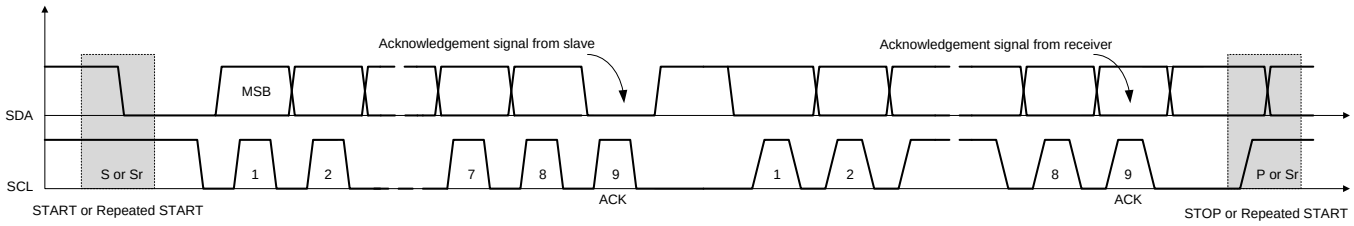


Figure 16. Data Transfer on the I²C Bus

8.3.6.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Feature Description (continued)

8.3.6.5 Slave Address and Data Direction bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

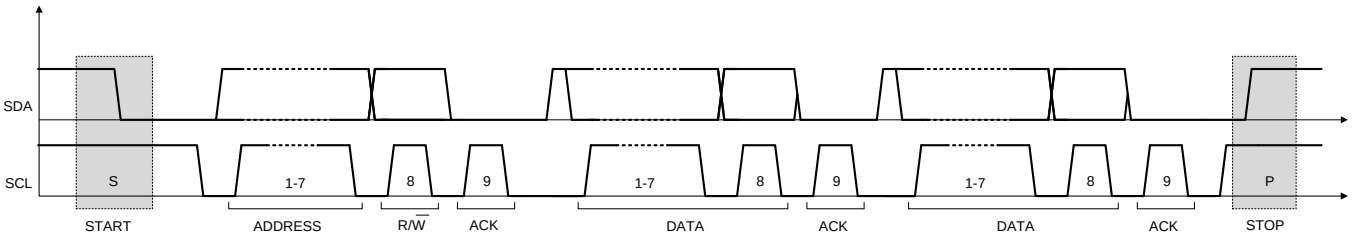


Figure 17. Complete Data Transfer

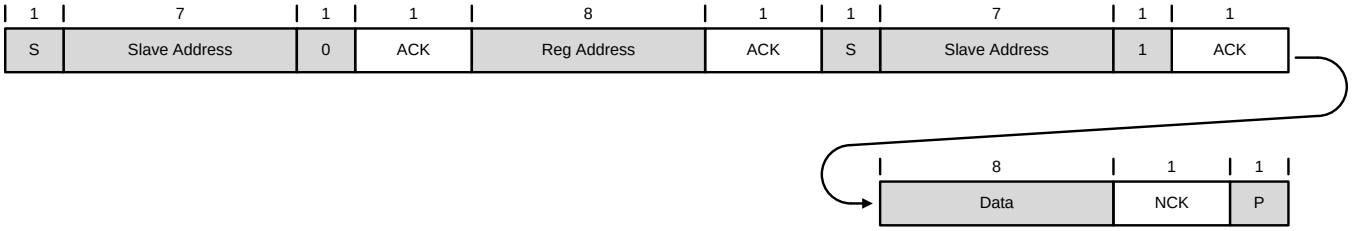


Figure 18. Single Read

If the register address is not defined, the charger device send back NACK and go back to the idle state.

8.3.6.6 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

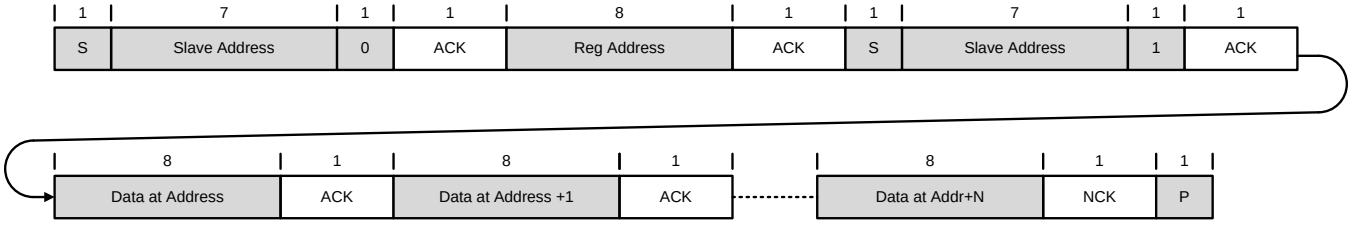


Figure 19. Multi-Read

EVENT_1, EVENT_2, and EVENT_3 keep all the information from last read until the host issues a new read. For example, if VBUS_OVP fault occurs but recovers later, the fault register EVENT_1 reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read EVENT_1, EVENT_2, and EVENT_3 for the second time.

8.4 Device Functional Modes

The device is a host controlled device. After power-on-reset, all the registers are in the default settings. All the device parameters can be programmed by the host. Writing 1 to REG 06 [0] will reset all registers to default setting. When watchdog timer expires, charge enable bit (REG06 [4]) and ADC enable bit (REG07 [3]) will be reset to default settings. To prevent watchdog timer expiring, the host has to read or write any register before the watchdog timer expires, or disable watchdog timer by setting REG06 [3:2] = 00.

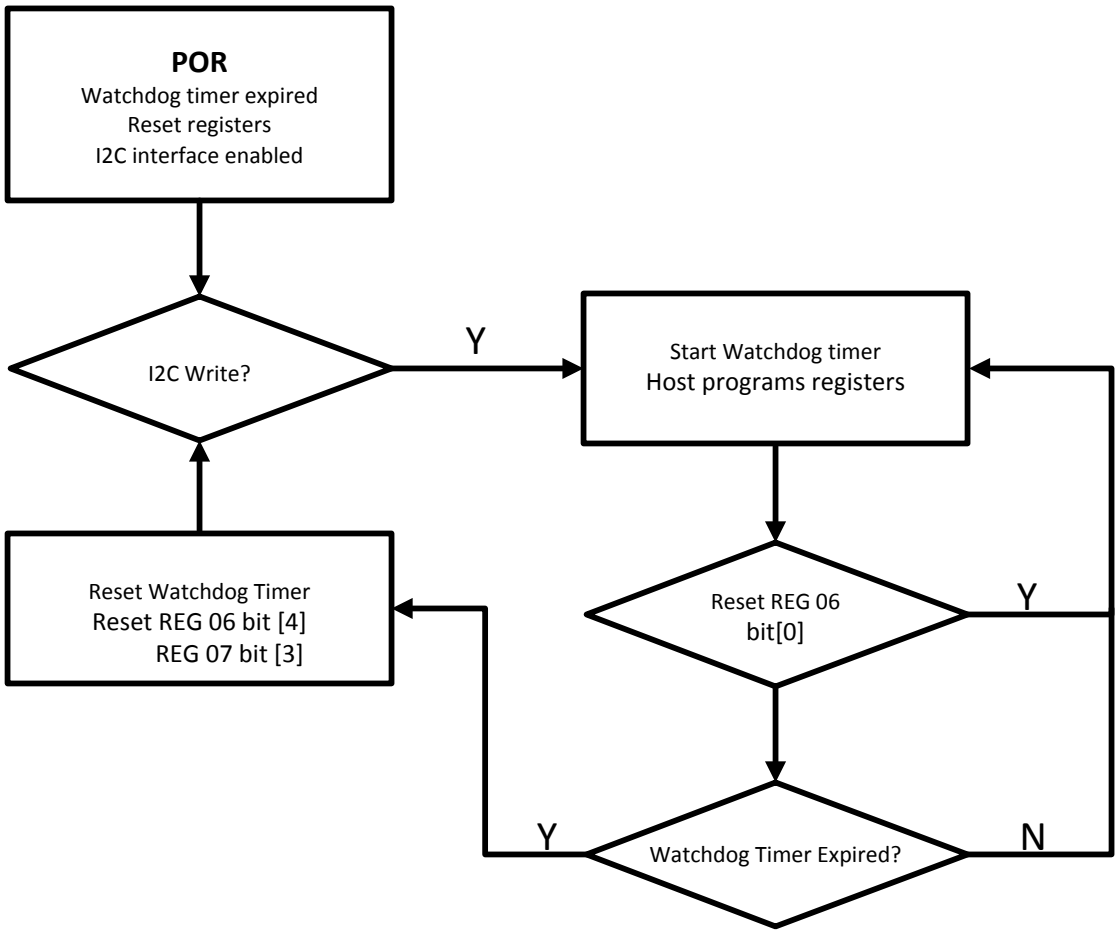


Figure 20. Operation Mode

8.5 I²C Register Maps

8.5.1 I²C Register Summary Table

Table 2. I²C Register Summary Table

I²C ADDRESS	R/W	REGISTER NAME	DESCRIPTION	POR STATE
0x00	R	DEVICE_INFO	Device rev and device ID	0x02
0x01	R/W	EVENT_1_MASK	Masks INT toggle of events in EVENT_1	0x00
0x02	R/W	EVENT_2_MASK	Masks INT toggle of events in EVENT_2	0x00
0x03	R	EVENT_1	First event register	0x00
0x04	R	EVENT_2	Second event register	0x00
0x05	R/W	EVENT_1_EN	Enables/disables protection in EVENT_1 register	0xFE
0x06	R/W	CONTROL	Settings for battery switch, watchdog, reset, and RCP threshold	0x2C
0x07	R/W	ADC_CTRL	Contains ADC control bits such as enable/disable, rate, and number of samples to take	0x87
0x08	R/W	ADC_MASK	Controls which parameters the ADC converts – first set	0xFF
0x09	R/W	PROTECTION	Deglitch setting and VBUS OCP threshold	0xA0
0x0A	R/W	VBUS_OVP	Sets VBUS OVP threshold	5.49 V
0x0B	R/W	VOUT_REG	Sets VOUT voltage regulation threshold	4.4 V
0x0C	R/W	VDROP_OVP	Sets the VDROP OVP threshold	300 mV
0x0D	R/W	VDROP_ALM	Sets the VDROP alarm threshold	100 mV
0x0E	R/W	VBAT_REG	Battery (BATP – BATN) regulation threshold	4.3 V
0x0F	R/W	IBAT_REG	Sets battery current regulation threshold	2 A
0x10	R/W	IBUS_REG	Sets VBUS REG threshold	5 A
0x11	R/W	TS_BUS_FLT	Sets VBUS temperature threshold	0.6 V
0x12	R/W	TS_BAT_FLT	Sets battery temperature threshold	0.7 V
0x13	R	VBUS_ADC	ADC output of VBUS voltage measurement	0x00
0x14	R			0x00
0x15	R	IBUS_ADC	ADC output of VBUS current measurement	0x00
0x16	R			0x00
0x17	R	VOUT_ADC	ADC output of VOUT voltage measurement	0x00
0x18	R			0x00
0x19	R	VDROP_ADC	ADC output of (VBUS – VOUT) voltage measurement	0x00
0x1A	R			0x00
0x1B	R	VBAT_ADC	ADC output of battery voltage measurement	0x00
0x1C	R			0x00
0x1D	R	IBAT_ADC	ADC output of battery current measurement	0x00
0x1E	R			0x00
0x1F	R	TBUS_ADC	ADC output of TS_BUS voltage	0x00
0x20	R			0x00
0x21	R	TBAT_ADC	ADC output of TS_BAT voltage	0x00
0x22	R			0x00
0x23	R	DIE_TEMP_ADC	ADC output of the die temperature	0x00
0x24	R/W	EVENT_3_EN	Enables/disables protection in EVENT_3 register	0x04
0x25	R/W	EVENT_3_MASK	Masks INT toggle of events in EVENT_3	0x00
0x26	R/W	EVNET_3	Third event register	0x00
0x29	R/W	CONTROL_2	Select location of IBAT sensing resistor	0x00
0x40	R/W	TDIE_TEMP_FLT	Setting die over temperature fault threshold	0x03

8.5.2 REG00 (DEVICE_INFO)

Figure 21. REG00 (DEVICE_INFO)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. REG00 (DEVICE_INFO)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
5	DEVICE_REV[2]	R	N/A	N/A	N/A	Device revision.
4	DEVICE_REV[1]	R	N/A	N/A	N/A	Device revision.
3	DEVICE_REV[0]	R	N/A	N/A	N/A	Device revision.
2	DEVICE_ID[2]	R	N/A	N/A	N/A	Device ID 010
1	DEVICE_ID[1]	R	N/A	N/A	N/A	
0	DEVICE_ID[0]	R	N/A	N/A	N/A	

8.5.3 REG01 (EVENT_1_MASK)

Figure 22. REG01 (EVENT_1_MASK)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. REG01 (EVENT_1_MASK)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VBUS_OVP_MASK	R/W	Y	N	Y	VBUS over voltage fault mask 0 – no mask. $\overline{INT}$ will assert low when VBUS_OVP_FLT bit is set (default) 1 – VBUS_OVP_FLT is mask. $\overline{INT}$ will not assert low when VBUS_OVP_FLT is set.
6	LDO_ACTIVE_MASK	R/W	Y	N	Y	LDO active bit mask 0 – no mask. $\overline{INT}$ will assert low when LDO_ACTIVE bit is set (default) 1 – LDO_ACTIVE is mask. $\overline{INT}$ will not assert low when LDO_ACTIVE bit is set.
5	LDO_ACTIVE_MASK	R/W	Y	N	Y	LDO active bit mask 0 – no mask. $\overline{INT}$ will assert low when LDO_ACTIVE bit is set (default) 1 – LDO_ACTIVE is mask. $\overline{INT}$ will not assert low when LDO_ACTIVE is set.
4	LDO_ACTIVE_MASK	R/W	Y	N	Y	LDO active bit mask 0 – no mask. $\overline{INT}$ will assert low when LDO_ACTIVE bit is set (default) 1 – LDO_ACTIVE is mask. $\overline{INT}$ will not assert low when LDO_ACTIVE is set.
3	LDO_ACTIVE_MASK	R/W	Y	N	Y	LDO active bit mask 0 – no mask. $\overline{INT}$ will assert low when LDO_ACTIVE bit is set (default) 1 – LDO_ACTIVE is mask. $\overline{INT}$ will not assert low when LDO_ACTIVE is set.
2	TS_BUS_FLT_MASK	R/W	Y	N	Y	VBUS over temperature fault mask 0 – no mask. $\overline{INT}$ will assert low when TS_BUS_FLT bit is set (default) 1 – TS_BUS_FLT is mask. $\overline{INT}$ will not assert low when TS_BUS_FLT is set.
1	TS_BAT_FLT_MASK	R/W	Y	N	Y	VBUS over temperature fault mask 0 – no mask. $\overline{INT}$ will assert low when TS_BAT_FLT bit is set (default) 1 – TS_BAT_FLT is mask. $\overline{INT}$ will not assert low when TS_BAT_FLT is set.
0	IBUS_REV_MASK	R/W	Y	N	Y	IBUS reverse current fault mask 0 – no mask. $\overline{INT}$ will assert low when IBUS_REV bit is set (default) 1 – IBUS_REV is mask. $\overline{INT}$ will not assert low when IBUS_REV is set.

8.5.4 REG02 (EVENT_2_MASK)

Figure 23. REG02 (EVENT_2_MASK)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. REG02 (EVENT_2_MASK)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
6	ADC_DONE_MASK	R/W	Y	N	Y	ADC_DONE bit mask 0 – no mask. $\overline{INT}$ will assert low when ADC_DONE bit is set (default) 1 – ADC_DONE is mask. $\overline{INT}$ will not assert low when ADC_DONE bit is set.
5	VDROP_ALM_MASK	R/W	Y	N	Y	VDROP_ALM event mask 0 – no mask. $\overline{INT}$ will assert low when VDROP_ALM bit is set (default) 1 – VDROP_ALM is mask. $\overline{INT}$ will not assert low when VDROP_ALM bit is set.
4	VDROP_OVP_MASK	R/W	Y	N	Y	VDROP_OVP event mask 0 – no mask. $\overline{INT}$ will assert low when VDROP_OVP bit is set (default) 1 – VDROP_OVP is mask. $\overline{INT}$ will not assert low when VDROP_OVP is set.
3	VBUS_INSERT_MASK	R/W	Y	N	Y	VBUS_INSERT mask 0 – no mask. $\overline{INT}$ will assert low when VBUS_INSERT bit is set (default) 1 – VBUS_INSERT is mask. $\overline{INT}$ will not assert low when VBUS_INSERT is set.
2	BAT_INSERT_MASK	R/W	Y	N	Y	BAT_INSERT mask 0 – no mask. $\overline{INT}$ will assert low when BAT_INSERT bit is set (default) 1 – BAT_INSERT is mask. $\overline{INT}$ will not assert low when BAT_INSERT is set.
1	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
0	IBUS_OCP_MASK	R/W	Y	N	Y	IBUS over current fault mask 0 – no mask. $\overline{INT}$ will assert low when IBUS_OCP bit is set (default) 1 – IBUS_OCP is mask. $\overline{INT}$ will not assert low when IBUS_OCP is set.

8.5.5 REG03 (EVENT_1)

Figure 24. REG03 (EVENT_1)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. 6.4.5 REG03 (EVENT_1)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VBUS_OVP_FLT	R	Y	N	Y	VBUS over voltage fault. This bit is set when VBUS voltage exceeds the limit set in VBUS_OVP register 0 – no fault (default) 1 – VBUS OVP fault
6	LDO_ACTIVE	R	Y	N	Y	Indicates if the device is in LDO mode 0 – not in LDO mode (default) 1 – in LDO mode
5	LDO_ACTIVE	R	Y	N	Y	Indicates if the device is in LDO mode 0 – not in LDO mode (default) 1 – in LDO mode
4	LDO_ACTIVE	R	Y	N	Y	Indicates if the device is in LDO mode 0 – not in LDO mode (default) 1 – in LDO mode
3	LDO_ACTIVE	R	Y	N	Y	Indicates if the device is in LDO mode 0 – not in LDO mode (default) 1 – in LDO mode
2	TS_BUS_FLT	R	Y	N	Y	VBUS over temperature fault. This bit is set when TS_BUS voltage falls below the limit set in TS_BUS_register. Battery switch is disabled. 0 – no fault (default) 1 – VBUS over temperature fault
1	TS_BAT_FLT	R	Y	N	Y	Battery over temperature fault. This bit is set when TS_BAT voltage falls below the limit set in TS_BAT_register. Battery switch is disabled. 0 – no fault (default) 1 – VBAT over temperature fault
0	IBUS_IREV_FLT	R	Y	N	Y	IBUS reverse current fault. This bit is set when current from VOUT to VBUS is detected. Battery switch is disabled. 0 – no fault (default) 1 – IBUS reverse current fault

8.5.6 REG04 (EVENT_2)

Figure 25. REG04 (EVENT_2)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. REG04 (EVENT_2)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
6	ADC_DONE.	R	Y	N	Y	Indicates if ADC conversion is complete for the required parameters in 1-shot mode only. This bit will change to '0' when an ADC conversion is is requested in 1-shot mode, and it will change back to '1' when the conversion is complete. During continuous conversion mode, this bit will be '0'. 0 – conversion not complete (default) 1 – conversion complete
5	VDROP_ALM	R	Y	N	Y	Indicates if VDROP_ALM threshold is reached 0 – no fault (default) 1 – VDROP_ALM fault
4	VDROP_OVP_FLT	R	Y	N	Y	Indicates if VDROP_OVP threshold is reached. Battery switch is disabled. 0 – no fault (default) 1 – VDROP_OVP fault
3	VBUS_INSERT	R	Y	N	Y	Indicates if VBUS is detected. \INT toggles when VBUS is inserted but does not toggle when VBUS is removed. 0 – VBUS not inserted (default) 1 – VBUS inserted
2	BAT_INSERT	R	Y	N	Y	Indicates if battery is detected. \INT toggles when battery is inserted but does not toggle when battery is removed. 0 – Battery not inserted (default) 1 – Battery inserted
1	TSHUT_FLT	R/W	Y	N	Y	IC thermal shutdown indictator. Battery switch is disabled. 0 – no fault (default) 1 – IC thermal shutdown fault
0	IBUS_OCP_FLT	R/W	Y	N	Y	IBUS over current fault. This bit is set when IBUS exceeds IBUS_OCP register. Battery switch is disabled. 0 – no fault (default) 1 – IBUS over current fault

8.5.7 REG05 (EVENT_1_EN)

Figure 26. REG05 (EVENT_1_EN)

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. REG05 (EVENT_1_EN)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VBUS_OVP_EN	R/W	Y	N	Y	Enables VBUS_OVP protection 0 – disable VBUS_OVP protection 1 – enable VBUS_OVP protection (default)
6	IBUS_REG_EN	R/W	Y	N	Y	Enable IBUS regulation 0 – disable IBUS regulation 1 – enable IBUS regulation (default)
5	VBAT_REG_EN	R/W	Y	N	Y	Enable VBAT regulation 0 – disable VBAT regulation 1 – enable VBAT regulation (default)
4	IBAT_REG_EN	R/W	Y	N	Y	Enable IBAT regulation 0 – disable IBAT regulation 1 – enable IBAT regulation (default)
3	VOUT_REG_EN	R/W	Y	N	Y	Enable VOUT regulation 0 – disable VOUT regulation 1 – enable VOUT regulation (default)
2	TS_BUS_FLT_EN	R/W	Y	N	Y	Enable TS_BUS protection 0 – disable TS_BUS protection 1 – enable TS_BUS protection (default)
1	TS_BAT_FLT_EN	R/W	Y	N	Y	Enable TS_BAT protection 0 – disable TS_BAT protection 1 – enable TS_BAT protection (default)
0	VBUS_PD_EN	R/W	Y	N	Y	Enable the VBUS pull-down resistor (RVBUS_PD) 0 – disable RVBUS_PD (default) 1 – enable RVBUS_PD

8.5.8 REG06 (CONTROL)

Figure 27. REG06 (CONTROL)

7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. REG06 (CONTROL)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VDROP_OVP_EN	R/W	Y	N	Y	Enables VDROP_OVP protection 0 – disable VDROP_OVP protection (default) 1 – enable VDROP_OVP protection
6	VDROP_ALM_EN	R/W	Y	N	Y	Enables VDROP_ALM protection 0 – disable VDROP_ALM protection (default) 1 – enable VDROP_ALM protection
5	SENSE_R	R/W	Y	N	Y	Select the sense resistor value between SRP and SRN 0 – 5 mΩ 1 – 10 mΩ (default)
4	CHG_EN	R/W	Y	Y	Y	Software bit for charge enable. This enables the battery switch. This bit will set to '0' if any fault causes the battery switch to be disabled. 0 – charge disabled (default) 1 – charge enabled
3	WATCHDOG[1]	R/W	Y	N	Y	Watchdog timer setting 00 – disable watchdog timer 01 – 0.5 s 10 – 1.0 s (default) 11 – 2 s
2	WATCHDOG[0]	R/W	Y	N	Y	
1	RCP_SET	R/W	Y	N	Y	Reverse current protection (RCP) threshold setting 0 – RCP set to 0 A (default) 1 – RCP set to -3 A
0	REG_RST	R/W	Y	N	Y	Register reset 0 – no reset (default) 1 – reset all registers to default values

8.5.9 REG07 (ADC_CONTROL)

Figure 28. REG07 (ADC_CONTROL)

7	6	5	4	3	2	1	0
1	0	0	0	0	1	1	1
R/W	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. REG07 (ADC_CONTROL)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	TDIE_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of die junction temperature 0 – disable conversion 1 – enabled conversion (default)
6	Reserved	R	Y	N	Y	Reserved bit. Always read 0.
5	Reserved	R	Y	N	Y	Reserved bit. Always read 0.
4	Reserved	R	Y	N	Y	Reserved bit. Always read 0.
3	ADC_EN	R/W	Y	Y	Y	Enable/ disable ADC 0 – disable ADC (default) 1 – enable ADC
2	ADC_RATE	R/W	Y	N	Y	Set ADC conversion rate 0 – 1-shot conversion 1 – continuous conversion (default)
1	ADC_AVG_EN	R/W	Y	N	Y	Enable/disable ADC measurement averaging 0 – disable averaging, instantaneous measurement 1 – enable averaging (default)
0	ADC_SAMPLES	R/W	Y	N	Y	Set the number of samples to be taken for an ADC conversion 0 – 8 samples taken for averaging 1 – 16 samples taken for averaging (default)

8.5.10 REG08 (ADC_EN)

Figure 29. REG08 (ADC_EN)

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. REG08 (ADC_EN)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VBUS_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of VBUS voltage 0 – disable conversion 1 – enabled conversion (default)
6	IBUS_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of IBUS current 0 – disable conversion 1 – enabled conversion (default)
5	VOUT_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of VOUT voltage 0 – disable conversion 1 – enabled conversion (default)
4	VDROP_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of VDROP voltage 0 – disable conversion 1 – enabled conversion (default)
3	VBAT_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of VBAT voltage 0 – disable conversion 1 – enabled conversion (default)
2	IBAT_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of IBAT current 0 – disable conversion 1 – enabled conversion (default)
1	TS_BUS_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of TS_BUS voltage 0 – disable conversion 1 – enabled conversion (default)
0	TS_BAT_ADC_EN	R/W	Y	N	Y	Enable/ disable conversion of TS_BAT voltage 0 – disable conversion 1 – enabled conversion (default)

8.5.11 REG09 (PROTECTION)

Figure 30. REG09 (PROTECTION)

7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. REG09

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	IBUS_OCP[3]	R/W	Y	N	Y	4 A	VBUS input overcurrent threshold Offset: none Range: 0 A to 7.5 A Default: 5 A (1010)
6	IBUS_OCP[2]	R/W	Y	N	Y	2 A	
5	IBUS_OCP[1]	R/W	Y	N	Y	1 A	
4	IBUS_OCP[0]	R/W	Y	N	Y	0.5 A	
3	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
2	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
1	OCP_RES	R/W	Y	N	Y	Controls the response of the OCP event or IBUS 0 – BLANKING mode; the device will wait 128 µs before the battery switch is disabled and latched off (default) 1 – HICCUP mode; battery switch is disabled instantaneously, and the device will attampt to turn on the battery switch every 100 ms, up to 7 times before latching off.	
0	VBUS_OVP_DLY	R/W	Y	N	Y	Set VBUS fault deglitch time 0 – 8 µs deglitch time (default) 1 – 128 µs deglitch time	

8.5.12 REG0A (VBUS_OVP)

Figure 31. REG0A (VBUS_OVP)

7	6	5	4	3	2	1	0
0	0	1	0	1	0	1	1
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. REG0A (VBUS_OVP)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	VBUS_OVP[6]	R/W	Y	N	Y	1920 mV	VBUS over voltage threshold Offset: 4.2 V Range: 4.2 V to 6.51 V Default: 5.49 V (00101011)
5	VBUS_OVP[5]	R/W	Y	N	Y	960 mV	
4	VBUS_OVP[4]	R/W	Y	N	Y	480 mV	
3	VBUS_OVP[3]	R/W	Y	N	Y	240 mV	
2	VBUS_OVP[2]	R/W	Y	N	Y	120 mV	
1	VBUS_OVP[1]	R/W	Y	N	Y	60 mV	
0	VBUS_OVP[0]	R/W	Y	N	Y	30 mV	

8.5.13 REG0B (VOUT_REG)

Figure 32. REG0B (VOUT_REG)

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. REG0B (VOUT_REG)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	VOUT_OVP[5]	R/W	Y	N	Y	800 mV	VOUT regulation threshold Offset: 4.2 V Range: 4.2 V to 4.975 V Default: 4.4 V (00010000)
5	VOUT_OVP[4]	R/W	Y	N	Y	400 mV	
4	VBUS_OVP[3]	R/W	Y	N	Y	200 mV	
3	VBUS_OVP[2]	R/W	Y	N	Y	100 mV	
2	VBUS_OVP[1]	R/W	Y	N	Y	50 mV	
1	VBUS_OVP[0]	R/W	Y	N	Y	25 mV	
0	Reserved	R/W	Y	N	Y	Reserved bit. Always read 0.	

8.5.14 REG0C (VDROP_OVP)

Figure 33. REG0C (VDROP_OVP)

7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. REG0C (VDROP_OVP)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	VDROP_OVP[6]	R/W	Y	N	Y	640 mV	VDROP OVP threshold Offset: none Range: 0 mV to 1000 mV Default: 300 mV (00111100)
6	VDROP_OVP[5]	R/W	Y	N	Y	320 mV	
5	VDROP_OVP[4]	R/W	Y	N	Y	160 mV	
4	VDROP_OVP[3]	R/W	Y	N	Y	80 mV	
3	VDROP_OVP[2]	R/W	Y	N	Y	40 mV	
2	VDROP_OVP[1]	R/W	Y	N	Y	20 mV	
1	VDROP_OVP[1]	R/W	Y	N	Y	10 mV	
0	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	

8.5.15 REG0D (VDROP_ALM)

Figure 34. REG0D (VDROP_ALM)

7	6	5	4	3	2	1	0
0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. REG0D (VDROP_ALM)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	VDROP_ALM[6]	R/W	Y	N	Y	640 mV	VDROP ALM threshold Offset: none Range: 0 mV to 1000 mV Default: 100 mV (00010100)
6	VDROP_ALM[5]	R/W	Y	N	Y	320 mV	
5	VDROP_ALM[4]	R/W	Y	N	Y	160 mV	
4	VDROP_ALM[3]	R/W	Y	N	Y	80 mV	
3	VDROP_ALM[2]	R/W	Y	N	Y	40 mV	
2	VDROP_ALM[1]	R/W	Y	N	Y	20 mV	
1	VDROP_ALM[1]	R/W	Y	N	Y	10 mV	
0	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	

8.5.16 REG0E (VBAT_REG)

Figure 35. REG0E (VBAT_REG)

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. REG0E (VBAT_REG)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	VBAT_REG[6]	R/W	Y	N	Y	800 mV	Battery voltage regulation threshold Offset: 4.2 V Range: 4.2 V to 4.975 V Default: 4.3 V (00001000)
5	VBAT_REG[5]	R/W	Y	N	Y	400 mV	
4	VBAT_REG[4]	R/W	Y	N	Y	200 mV	
3	VBAT_REG[3]	R/W	Y	N	Y	100 mV	
2	VBAT_REG[2]	R/W	Y	N	Y	50 mV	
1	VBAT_REG[1]	R/W	Y	N	Y	25 mV	
0	VBAT_REG[0]	R/W	Y	N	Y	12.5 mV	

8.5.17 REG0F (IBAT_REG)

Figure 36. REG0F (IBAT_REG)

7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. REG0F (IBAT_REG)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	IBAT_REG[6]	R/W	Y	N	Y	3200 mA	Battery current regulation threshold Offset: 0 A Range: 0 A to 6.35 A Default: 2 A (00101000)
5	IBAT_REG[5]	R/W	Y	N	Y	1600 mA	
4	IBAT_REG[4]	R/W	Y	N	Y	800 mA	
3	IBAT_REG[3]	R/W	Y	N	Y	400 mA	
2	IBAT_REG[2]	R/W	Y	N	Y	200 mA	
1	IBAT_REG[1]	R/W	Y	N	Y	100 mA	
0	IBAT_REG[0]	R/W	Y	N	Y	50 mA	

8.5.18 REG10 (IBUS_REG)

Figure 37. REG10 (IBUS_REG)

7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. REG10 (IBUS_REG)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	IBUS_REG[5]	R/W	Y	N	Y	3200 mA	Battery current regulation threshold Offset: 0 A Range: 0 A to 6.3 A Default: 5 A (01100100)
5	IBUS_REG[4]	R/W	Y	N	Y	1600 mA	
4	IBUS_REG[3]	R/W	Y	N	Y	800 mA	
3	IBUS_REG[2]	R/W	Y	N	Y	400 mA	
2	IBUS_REG[1]	R/W	Y	N	Y	200 mA	
1	IBUS_REG[0]	R/W	Y	N	Y	100 mA	
0	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	

8.5.19 REG11 (TS_BUS_FLT)

Figure 38. REG11 (TS_BUS_FLT)

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. REG11 (TS_BUS_FLT)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	TS_BUS_FLT[6]	R/W	Y	N	Y	1600 mA	TS_BUS voltage threshold Offset: 0 V Range: 0 V to 1.4 V Default: 0.6 V (00011000)
5	TS_BUS_FLT[5]	R/W	Y	N	Y	800 mA	
4	TS_BUS_FLT[4]	R/W	Y	N	Y	400 mA	
3	TS_BUS_FLT[3]	R/W	Y	N	Y	200 mA	
2	TS_BUS_FLT[2]	R/W	Y	N	Y	100 mA	
1	TS_BUS_FLT[1]	R/W	Y	N	Y	50 mA	
0	TS_BUS_FLT[0]	R/W	Y	N	Y	25 mA	

8.5.20 REG12 (TS_BAT_FLT)

Figure 39. REG12 (TS_BAT_FLT)

7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. REG12 (TS_BAT_FLT)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	Y	N	Y	Reserved bit. Always read 0.	
6	TS_BAT_FLT[6]	R/W	Y	N	Y	1600 mA	TS_BAT voltage threshold Offset: 0 V Range: 0 V to 1.4 V Default: 0.7 V (00011100)
5	TS_BAT_FLT[5]	R/W	Y	N	Y	800 mA	
4	TS_BAT_FLT[4]	R/W	Y	N	Y	400 mA	
3	TS_BAT_FLT[3]	R/W	Y	N	Y	200 mA	
2	TS_BAT_FLT[2]	R/W	Y	N	Y	100 mA	
1	TS_BAT_FLT[1]	R/W	Y	N	Y	50 mA	
0	TS_BAT_FLT[0]	R/W	Y	N	Y	25 mA	

8.5.21 REG 13 and REG 14 (VBUS_ADC)

Figure 40. REG 13 and REG 14 (VBUS_ADC)

REG13								REG14							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. REG 13 and REG 14 (VBUS_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG13	7	VBUS_POL	R	Y	N	Y	Indicates polarity of VBUS voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	VBUS_ADC[14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of VBUS voltage. Range: 0 V, and 2.048 V to 6.140 V Default: 0 V (0000000000000000) If VBUS < 0.3 V, VBUS_ADC = 0.3 V
	5	VBUS_ADC[13]	R	Y	N	Y	8192 mV	
	4	VBUS_ADC[12]	R	Y	N	Y	4096 mV	
	3	VBUS_ADC[11]	R	Y	N	Y	2048 mV	
	2	VBUS_ADC[10]	R	Y	N	Y	1024 mV	
	1	VBUS_ADC[9]	R	Y	N	Y	512 mV	
	0	VBUS_ADC[8]	R	Y	N	Y	256 mV	
REG14	7	VBUS_ADC[7]	R	Y	N	Y	128 mV	
	6	VBUS_ADC[6]	R	Y	N	Y	64 mV	
	5	VBUS_ADC[5]	R	Y	N	Y	32 mV	
	4	VBUS_ADC[4]	R	Y	N	Y	16 mV	
	3	VBUS_ADC[3]	R	Y	N	Y	8 mV	
	2	VBUS_ADC[2]	R	Y	N	Y	4 mV	
	1	VBUS_ADC[1]	R	Y	N	Y	2 mV	
	0	VBUS_ADC[0]	R	Y	N	Y	1 mV	

8.5.22 REG15 and REG16 (IBUS_ADC)

Figure 41. REG15 and REG16 (IBUS_ADC)

REG15								REG16							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. REG15 and REG16 (IBUS_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG15	7	IBUS_POL	R	Y	N	Y	Indicates polarity of IBUS current. Always positive. 0 - positive current 1 - negative current	
	6	IBUS_ADC[14]	R	Y	N	Y	16384 mA	Current representation of ADC conversion of VBUS current. Range: 0 A to 7.5 A Default: 0 A (0000000000000000)
	5	IBUS_ADC[13]	R	Y	N	Y	8192 mA	
	4	IBUS_ADC[12]	R	Y	N	Y	4096 mA	
	3	IBUS_ADC[11]	R	Y	N	Y	2048 mA	
	2	IBUS_ADC[10]	R	Y	N	Y	1024 mA	
	1	IBUS_ADC[9]	R	Y	N	Y	512 mA	
	0	IBUS_ADC[8]	R	Y	N	Y	256 mA	
REG16	7	IBUS_ADC[7]	R	Y	N	Y	128 mA	
	6	IBUS_ADC[6]	R	Y	N	Y	64 mA	
	5	IBUS_ADC[5]	R	Y	N	Y	32 mA	
	4	IBUS_ADC[4]	R	Y	N	Y	16 mA	
	3	IBUS_ADC[3]	R	Y	N	Y	8 mA	
	2	IBUS_ADC[2]	R	Y	N	Y	4 mA	
	1	IBUS_ADC[1]	R	Y	N	Y	2 mA	
	0	IBUS_ADC[0]	R	Y	N	Y	1 mA	

8.5.23 REG17 and REG18 (VOUT_ADC)

Figure 42. REG17 and REG18 (VOUT_ADC)

REG17								REG18							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. REG17 and REG18 (VOUT_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG17	7	VOUT_POL	R	Y	N	Y	Indicates polarity of VDROP voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	VOUT_ADC[14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of VDROP voltage. Range: 2.048 V to 6.140 V Default: 0 V (0000000000000000)
	5	VOUT_ADC[13]	R	Y	N	Y	8192 mV	
	4	VOUT_ADC[12]	R	Y	N	Y	4096 mV	
	3	VOUT_ADC[11]	R	Y	N	Y	2048 mV	
	2	VOUT_ADC[10]	R	Y	N	Y	1024 mV	
	1	VOUT_ADC[9]	R	Y	N	Y	512 mV	
	0	VOUT_ADC[8]	R	Y	N	Y	256 mV	
REG18	7	VOUT_ADC[7]	R	Y	N	Y	128 mV	
	6	VOUT_ADC[6]	R	Y	N	Y	64 mV	
	5	VOUT_ADC[5]	R	Y	N	Y	32 mV	
	4	VOUT_ADC[4]	R	Y	N	Y	16 mV	
	3	VOUT_ADC[3]	R	Y	N	Y	8 mV	
	2	VOUT_ADC[2]	R	Y	N	Y	4 mV	
	1	VOUT_ADC[1]	R	Y	N	Y	2 mV	
	0	VOUT_ADC[0]	R	Y	N	Y	1 mV	

8.5.24 REG19 and REG1A (VDROP_ADC)

Figure 43. REG19 and REG1A (VDROP_ADC)

REG19								REG1A							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. REG19 and REG1A (VDROP_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG19	7	VDROP_POL	R	Y	N	Y	Indicates polarity of VDROP voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	VDROP_ADC[14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of VBUS voltage. Range: 0 mV to 1000 mV Default: 0 mV (0000000000000000)
	5	VDROP_ADC[13]	R	Y	N	Y	8192 mV	
	4	VDROP_ADC[12]	R	Y	N	Y	4096 mV	
	3	VDROP_ADC[11]	R	Y	N	Y	2048 mV	
	2	VDROP_ADC[10]	R	Y	N	Y	1024 mV	
	1	VDROP_ADC[9]	R	Y	N	Y	512 mV	
	0	VDROP_ADC[8]	R	Y	N	Y	256 mV	
REG1A	7	VDROP_ADC[7]	R	Y	N	Y	128 mV	
	6	VDROP_ADC[6]	R	Y	N	Y	64 mV	
	5	VDROP_ADC[5]	R	Y	N	Y	32 mV	
	4	VDROP_ADC[4]	R	Y	N	Y	16 mV	
	3	VDROP_ADC[3]	R	Y	N	Y	8 mV	
	2	VDROP_ADC[2]	R	Y	N	Y	4 mV	
	1	VDROP_ADC[1]	R	Y	N	Y	2 mV	
	0	VDROP_ADC[0]	R	Y	N	Y	1 mV	

8.5.25 REG1B and REG1C (VBAT_ADC)

Figure 44. REG1B and REG1C (VBAT_ADC)

REG1B								REG1C							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. REG1B and REG1C (VBAT_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG1B	7	VBAT_POL	R	Y	N	Y	Indicates polarity of VBUS voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	VBAT_ADC[14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of VBAT voltage. Range: 2.048 V to 6.140 V Default: 0 V (0000000000000000)
	5	VBAT_ADC[13]	R	Y	N	Y	8192 mV	
	4	VBAT_ADC[12]	R	Y	N	Y	4096 mV	
	3	VBAT_ADC[11]	R	Y	N	Y	2048 mV	
	2	VBAT_ADC[10]	R	Y	N	Y	1024 mV	
	1	VBAT_ADC[9]	R	Y	N	Y	512 mV	
	0	VBAT_ADC[8]	R	Y	N	Y	256 mV	
REG1C	7	VBAT_ADC[7]	R	Y	N	Y	128 mV	
	6	VBAT_ADC[6]	R	Y	N	Y	64 mV	
	5	VBAT_ADC[5]	R	Y	N	Y	32 mV	
	4	VBAT_ADC[4]	R	Y	N	Y	16 mV	
	3	VBAT_ADC[3]	R	Y	N	Y	8 mV	
	2	VBAT_ADC[2]	R	Y	N	Y	4 mV	
	1	VBAT_ADC[1]	R	Y	N	Y	2 mV	
	0	VBAT_ADC[0]	R	Y	N	Y	1 mV	

8.5.26 REG1D and REG1E (IBAT_ADC)

Figure 45. REG1D and REG1E (IBAT_ADC)

REG1D								REG1E							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. REG1D and REG1E (IBAT_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG1D	7	IBAT_POL	R	Y	N	Y	Indicates polarity of battery current. 0 - positive voltage (default) 1 - negative voltage	
	6	IBAT_ADC[14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of VBUS voltage. Range: 0 A to 7.104 A Default: 0 A(0000000000000000)
	5	IBAT_ADC[13]	R	Y	N	Y	8192 mV	
	4	IBAT_ADC[12]	R	Y	N	Y	4096 mV	
	3	IBAT_ADC[11]	R	Y	N	Y	2048 mV	
	2	IBAT_ADC[10]	R	Y	N	Y	1024 mV	
	1	IBAT_ADC[9]	R	Y	N	Y	512 mV	
	0	IBAT_ADC[8]	R	Y	N	Y	256 mV	
REG1E	7	IBAT_ADC[7]	R	Y	N	Y	128 mV	
	6	IBAT_ADC[6]	R	Y	N	Y	64 mV	
	5	IBAT_ADC[5]	R	Y	N	Y	32 mV	
	4	IBAT_ADC[4]	R	Y	N	Y	16 mV	
	3	IBAT_ADC[3]	R	Y	N	Y	8 mV	
	2	IBAT_ADC[2]	R	Y	N	Y	4 mV	
	1	IBAT_ADC[1]	R	Y	N	Y	2 mV	
	0	IBAT_ADC[0]	R	Y	N	Y	1 mV	

8.5.27 REG1F and REG20 (TS_BUS_ADC)

Figure 46. REG1F and REG20 (TS_BUS_ADC)

REG1F								REG20							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. REG1F and REG20 (TS__BUS_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG1F	7	TS_BUS_POL	R	Y	N	Y	Indicates polarity of TS_BUS voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	TS_BUS_ADC [14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of TS_BUS voltage. Range: 0 V to 2.420 V Default: 0 V (0000000000000000)
	5	TS_BUS_ADC [13]	R	Y	N	Y	8192 mV	
	4	TS_BUS_ADC [12]	R	Y	N	Y	4096 mV	
	3	TS_BUS_ADC [11]	R	Y	N	Y	2048 mV	
	2	TS_BUS_ADC [10]	R	Y	N	Y	1024 mV	
	1	TS_BUS_ADC [9]	R	Y	N	Y	512 mV	
	0	TS_BUS_ADC [8]	R	Y	N	Y	256 mV	
REG20	7	TS_BUS_ADC [7]	R	Y	N	Y	128 mV	
	6	TS_BUS_ADC [6]	R	Y	N	Y	64 mV	
	5	TS_BUS_ADC [5]	R	Y	N	Y	32 mV	
	4	TS_BUS_ADC [4]	R	Y	N	Y	16 mV	
	3	TS_BUS_ADC [3]	R	Y	N	Y	8 mV	
	2	TS_BUS_ADC [2]	R	Y	N	Y	4 mV	
	1	TS_BUS_ADC [1]	R	Y	N	Y	2 mV	
	0	TS_BUS_ADC [0]	R	Y	N	Y	1 mV	

8.5.28 REG21 and REG22 (TS_BAT_ADC)

Figure 47. REG21 and REG22 (TS_BAT_ADC)

REG21								REG22							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. REG21 and REG22 (TS_BAT_ADC)

Register	Bit	Field	Type	Reset			Description	
				REG_RST	Watchdog	EN		
REG21	7	TS_BAT_POL	R	Y	N	Y	Indicates polarity of TS_BAT voltage. Always positive. 0 - positive voltage 1 - negative voltage	
	6	TS_BAT_ADC [14]	R	Y	N	Y	16384 mV	Voltage representation of ADC conversion of TS_BAT voltage. Range: 0 V to 2.420 V Default: 0 V (0000000000000000)
	5	TS_BAT_ADC [13]	R	Y	N	Y	8192 mV	
	4	TS_BAT_ADC [12]	R	Y	N	Y	4096 mV	
	3	TS_BAT_ADC [11]	R	Y	N	Y	2048 mV	
	2	TS_BAT_ADC [10]	R	Y	N	Y	1024 mV	
	1	TS_BAT_ADC [9]	R	Y	N	Y	512 mV	
	0	TS_BAT_ADC [8]	R	Y	N	Y	256 mV	
REG22	7	TS_BAT_ADC [7]	R	Y	N	Y	128 mV	
	6	TS_BAT_ADC [6]	R	Y	N	Y	64 mV	
	5	TS_BAT_ADC [5]	R	Y	N	Y	32 mV	
	4	TS_BAT_ADC [4]	R	Y	N	Y	16 mV	
	3	TS_BAT_ADC [3]	R	Y	N	Y	8 mV	
	2	TS_BAT_ADC [2]	R	Y	N	Y	4 mV	
	1	TS_BAT_ADC [1]	R	Y	N	Y	2 mV	
	0	TS_BAT_ADC [0]	R	Y	N	Y	1 mV	

8.5.29 REG 23 (TDIE_ADC)

Figure 48. REG23 (TDIE_ADC)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. REG23 (TDIE_ADC)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	DIE_TEMP_ADC [7]	R	Y	N	Y	128°C	Temperature representation of ADC conversion of die junction temperature. Range: 25°C to 150°C Default: 0°C (0000000000000000)
6	DIE_TEMP_ADC [6]	R	Y	N	Y	64°C	
5	DIE_TEMP_ADC [5]	R	Y	N	Y	32°C	
4	DIE_TEMP_ADC [4]	R	Y	N	Y	16°C	
3	DIE_TEMP_ADC [3]	R	Y	N	Y	8°C	
2	DIE_TEMP_ADC [2]	R	Y	N	Y	4°C	
1	DIE_TEMP_ADC [1]	R	Y	N	Y	2°C	
0	DIE_TEMP_ADC [0]	R	Y	N	Y	1°C	

8.5.30 REG 24 (EVENT_2_EN)

Figure 49. REG24 (EVENT_2_EN)

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. REG24 (EVENT_2_EN) (0x24 Register)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	VDROP_AMP_DIS	R/W	Y	N	Y	Turn on/ off VDROP AMP 0 – Turn on VDROP AMP (default) 1 – Turn off VDROP AMP
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
5	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
4	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
3	IBUS_OCP_EN	R/W	Y	N	Y	Enable/ disable IBUS over current protection 0 – disable IBUS OCP 1 – enabled IBUS OCP (default)
2	VBAT_OVP_EN	R/W	Y	N	Y	Enable/ disable VBAT over voltage protection 0 – disable VBAT OVP (default) 1 – enabled VBAT OVP
1	IBAT_OCP_EN	R/W	Y	N	Y	Enable/ disable IBAT over current protection 0 – disable IBAT OCP (default) 1 – enabled IBAT OCP
0	VOUT_OVP_EN	R/W	Y	N	Y	Enable/ disable VOUT over voltage protection 0 – disable VOUT OVP protection (default) 1 – enabled VOUT_OVP

8.5.31 REG 25 (EVENT_3_MASK)

Figure 50. REG25 (EVENT_3_MASK)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. REG26 (EVENT_3_MASK) (0x026 Register)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
5	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
4	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
3	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
2	VBAT_OVP_MASK	R/W	Y	N	Y	VBAT over voltage fault mask. 0 – no mask. $\overline{INT}$ will assert low when VBAT_OVP bit is set (default) 1 – VBAT_OVP is masked. $\overline{INT}$ will not assert low when VBAT_OVP bit is set.
1	IBAT_OCP_MASK	R/W	Y	N	Y	IBAT over current fault mask. 0 – no mask. $\overline{INT}$ will assert low when IBAT_OCP bit is set (default) 1 – IBAT_OCP is masked. $\overline{INT}$ will not assert low when IBAT_OCP bit is set.
0	VOUT_OVP_MASK	R/W	Y	N	Y	VOUT over voltage fault mask. 0 – no mask. $\overline{INT}$ will assert low when VOUT_OVP bit is set (default) 1 – VOUT_OVP is masked. $\overline{INT}$ will not assert low when VOUT_OVP bit is set.

8.5.32 REG 26 (EVENT_3)

Figure 51. REG26 (EVENT_3)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. REG26 (EVENT_3) (0x26 Register)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	SCP_FLT	R	Y	N	Y	Indicates if high current from VBUS to VOUT has hit I_{SCP} threshold. Battery switch is disabled 0 – no fault (default) 1 – short circuit fault
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
5	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
4	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
3	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
2	VBAT_OVP_FLT	R	Y	N	Y	Indicates if VBAT_OVP threshold is reached. Battery switch is disabled 0 – no fault (default) 1 – VBAT_OVP fault
1	IBAT_OCP_FLT	R	Y	N	Y	Indicates if IBAT_OCP threshold is reached. Battery switch is disabled 0 – no fault (default) 1 – IBAT_OCP fault
0	VOUT_OVP_FLT	R	Y	N	Y	Indicates if VOUT_OVP threshold is reached. Battery switch is disabled 0 – no fault (default) 1 – VOUT_OVP fault

8.5.33 REG 29 (CONTROL_2)

Figure 52. REG29 (CONTROL_2)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. REG29 (RSENSE) (0x29 Register)

Bit	Field	Type	Reset			Description
			REG_RST	Watchdog	EN	
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
5	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
4	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
3	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
2	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
1	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.
0	R_PLACE	R/W	Y	N	Y	Select location of SRP/SRN sense resistor 0 – low-side placement (default) 1 – high-side placement

8.5.34 REG 40 (DIE_TEMP_FLT)

Figure 53. REG 40 (DIE_TEMP_FLT)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R	R	R	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. REG 40 (DIE_TEMP_FLT) (0x40 Register)

Bit	Field	Type	Reset			Description	
			REG_RST	Watchdog	EN		
7	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
6	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
5	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
4	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
3	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
2	Reserved	R	N/A	N/A	N/A	Reserved bit. Always reads 0.	
1	DIE_TEMP_FLT [1]	R/W	Y	N	Y	30 C	TSHUT temperature threshold Offset: 105°C Range: 105°C to 150°C Default: 150°C (0b11)
0	DIE_TEMP_FLT [0]	R/W	Y	N	Y	15 C	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled device and another switch mode charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. A host controls which charger is enabled during the charging process.

9.2 Typical Application

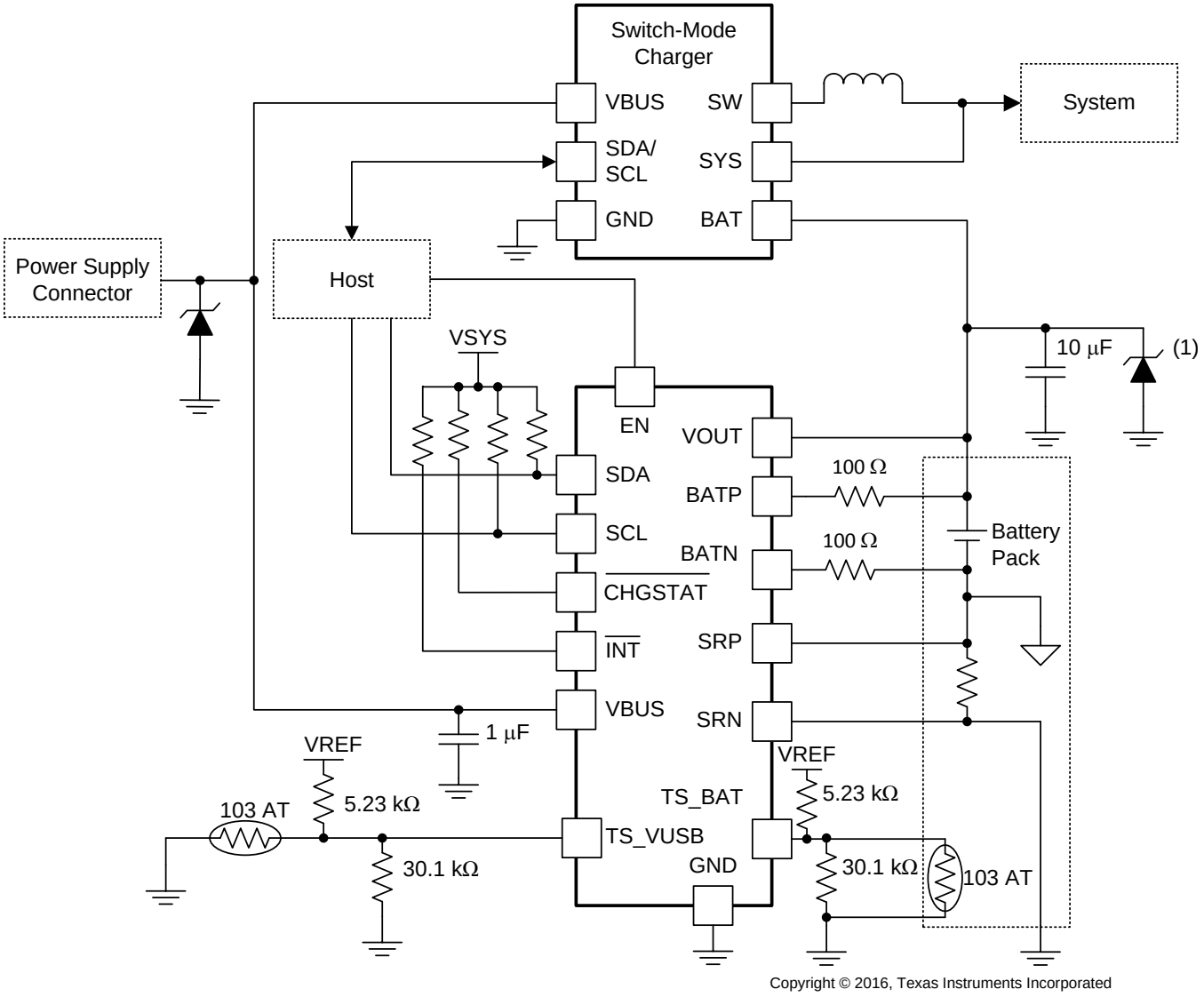


Figure 54. bq25871 Typical Application

Typical Application (continued)

9.2.1 Design Requirements

Table 36. Design Requirement

PARAMETER	VALUE
Input voltage range	3 V to 6 V
Input current limit	0.1 A to 7.5 A
Output voltage range	3 V to 4.975 V

9.2.2 Detailed Design Procedure

The bq25871 continuously monitors battery and adaptor connector temperature by measuring the voltage between TS_BAT pin and TS_BUS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charging cycle, both battery and connector temperatures must be lower than the temperature threshold, else the device suspends charging and waits until both temperatures are blow the threshold.

Assuming a 103 AT NTC thermistor is used on the battery pack, the values RT1 (connected between TS_X pin to VREF) and RT2 (connected between TS_X and ground) can be determined by using the following equations.

$$RT2 = \frac{V_{REF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{REF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REF}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{REF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

where

- RTH_{cold} and V_{LTF} are the resistance of NTC under the cold temperature and the corresponding TS_X pin voltage when charge is allowed, RTH_{hot} and $V_{TCO}$are the resistance of NTC under the hot temperature and the corresponding TS_X pin voltage when charge is allowed. (1)

9.2.3 Application Curves

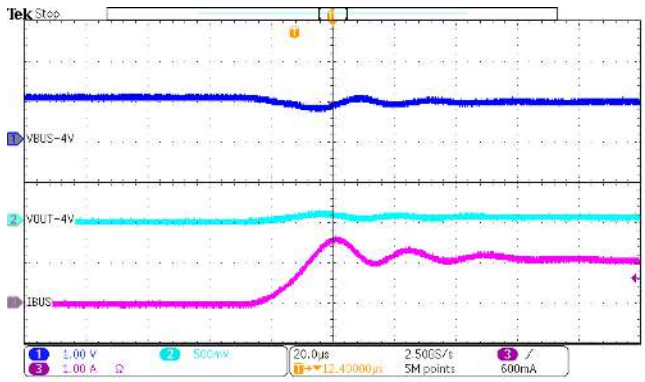


Figure 55. Power Up with IBUS_REG = 1 A

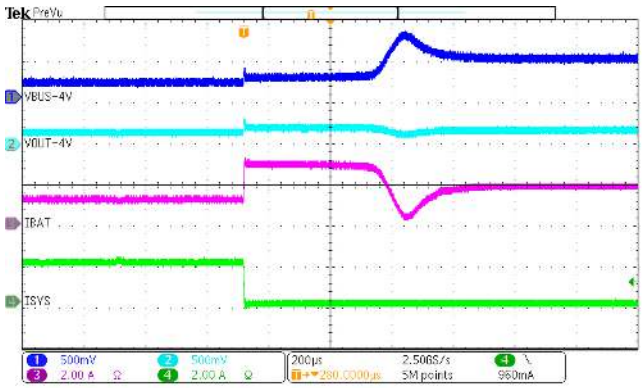


Figure 56. IBAT Regulation During Load Step Down

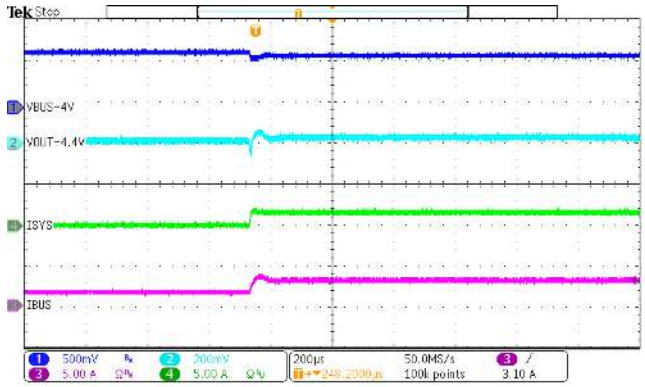


Figure 57. VBAT Regulation During Load Step Down

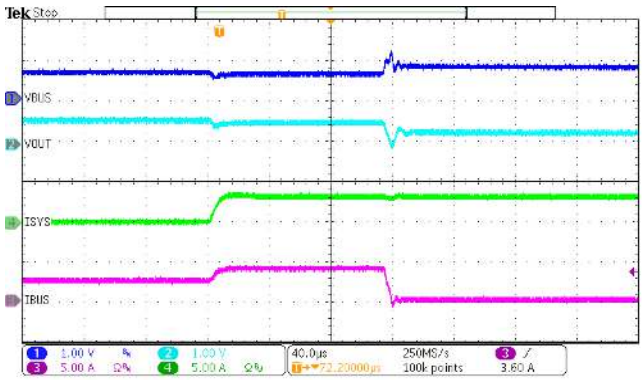


Figure 58. IBUS OCP During Load Transient

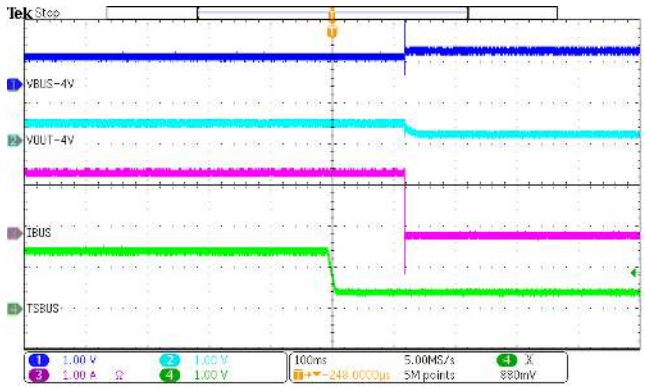


Figure 59. TS BUS OTP

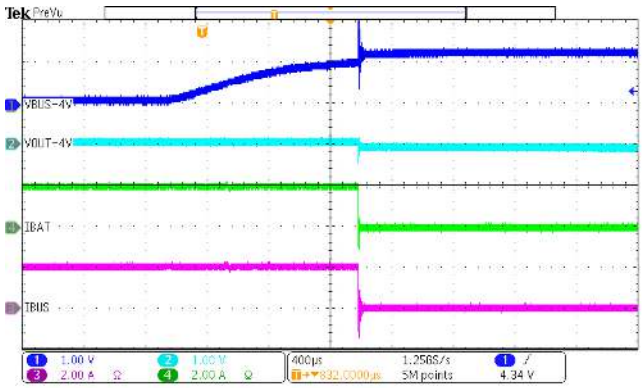


Figure 60. VBUS OVP with IBUS Regulation

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9-V and 14-V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT. The source current rating needs to be at least 7.5 A to meet the current capability of the device.

11 Layout

11.1 Layout Guidelines

bq25871 supports up to 7-A charge current. It is very critical to maximize Cu trace of VBUS and VOUT. Following PCB layout guideline is recommended:

- Use Cu trace of at least 110 mil (2.794 mm) wide for VBUS and VOUT respectively. This allows current flow evenly through all 7 WCSP solder balls.
- Cu trace of VBUS and VOUT should run at least 150 mil (3.81 mm) straight (perpendicular to WCSP ball array) before making turns.
- Use as large as possible Cu pour for VBUS and VOUT trace elsewhere.
- Use as large as possible Cu pour for PGND.
- Place decoupling capacitors of VBUS and VOUT as close as possible to the device.

11.2 Layout Example

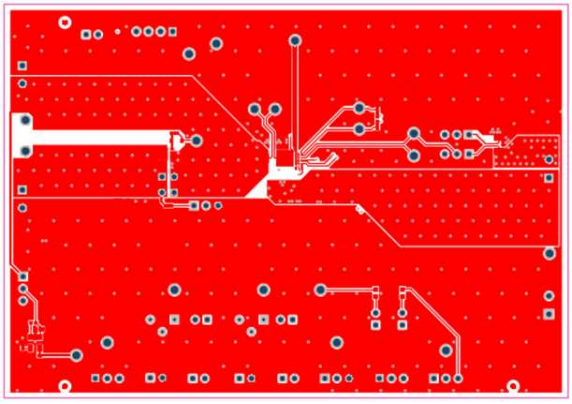


Figure 61. bq25871 Layout Diagram (Top Layer)

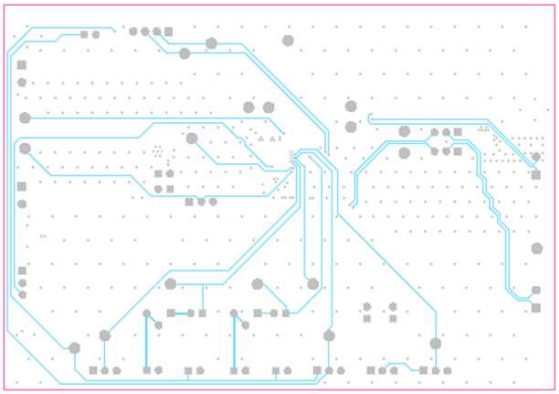


Figure 62. bq25871 Layout Diagram (Mid Layer 2)

Layout Example (continued)

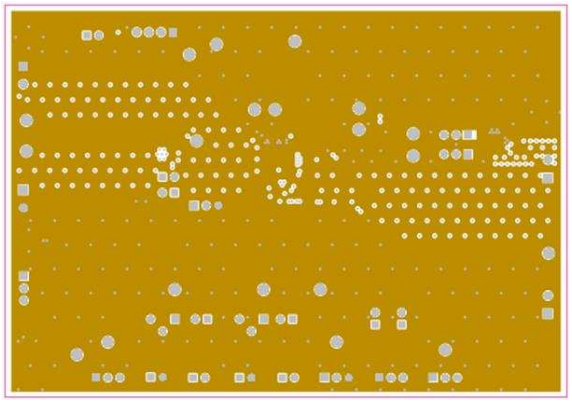


Figure 63. bq25871 Layout Diagram (Mid Layer 1)

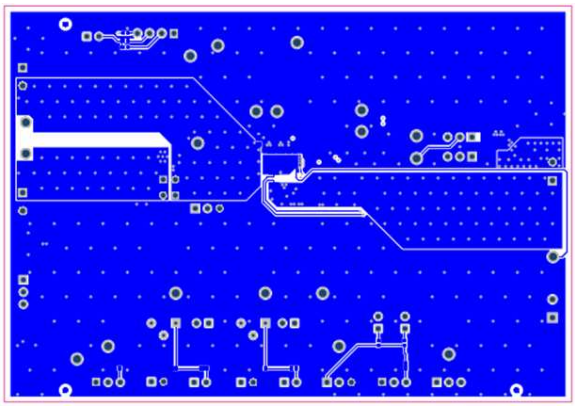


Figure 64. bq25871 Layout Diagram (Bottom 1)

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
I^2C is a trademark of Philips Semiconductor.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25871YFFR	ACTIVE	DSBGA	YFF	42	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25871	Samples
BQ25871YFFT	ACTIVE	DSBGA	YFF	42	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25871	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

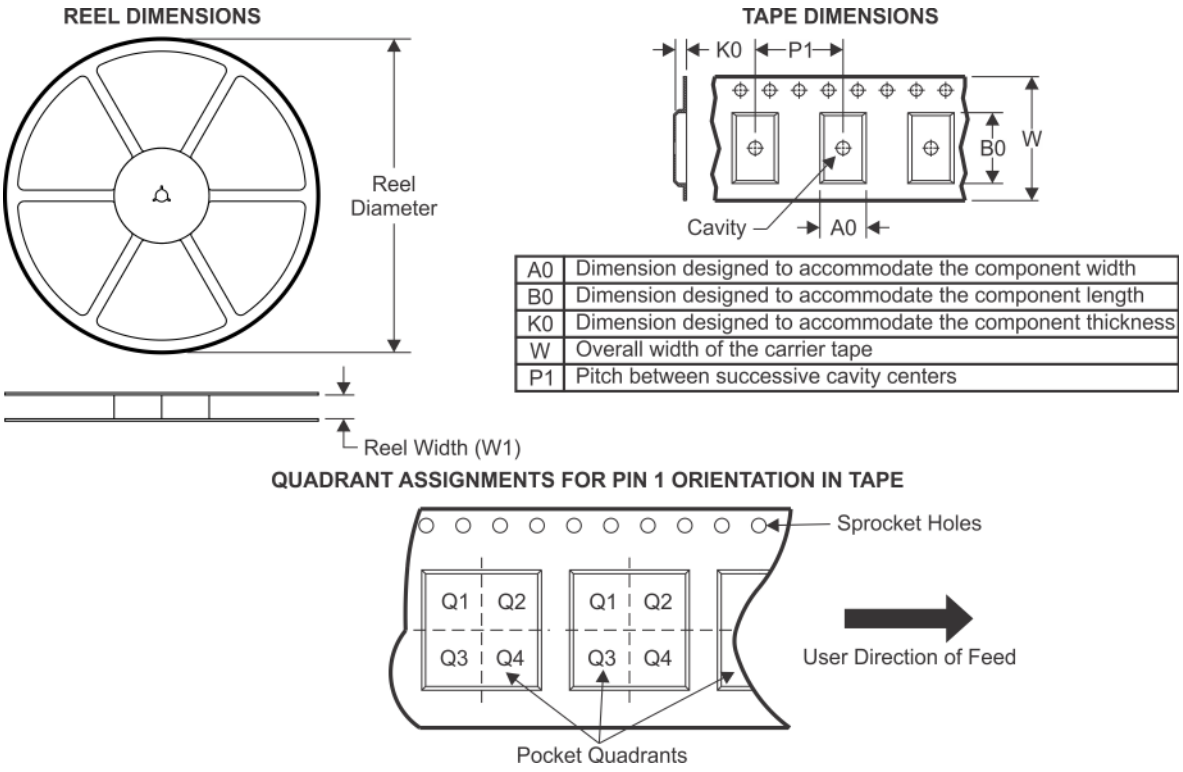
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

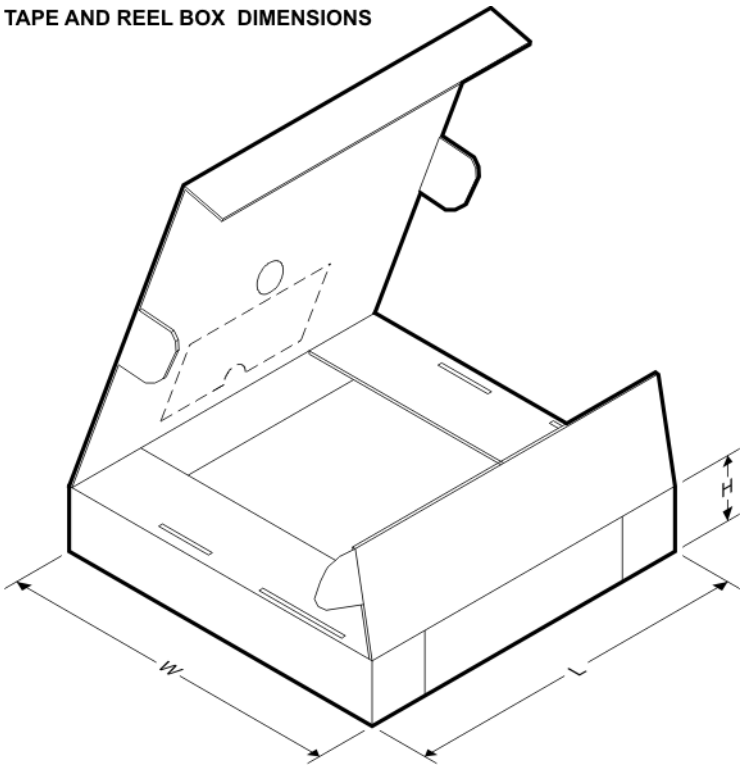


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25871YFFR	DSBGA	YFF	42	3000	330.0	12.4	2.62	3.3	0.81	4.0	12.0	Q1
BQ25871YFFT	DSBGA	YFF	42	250	330.0	12.4	2.62	3.3	0.81	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

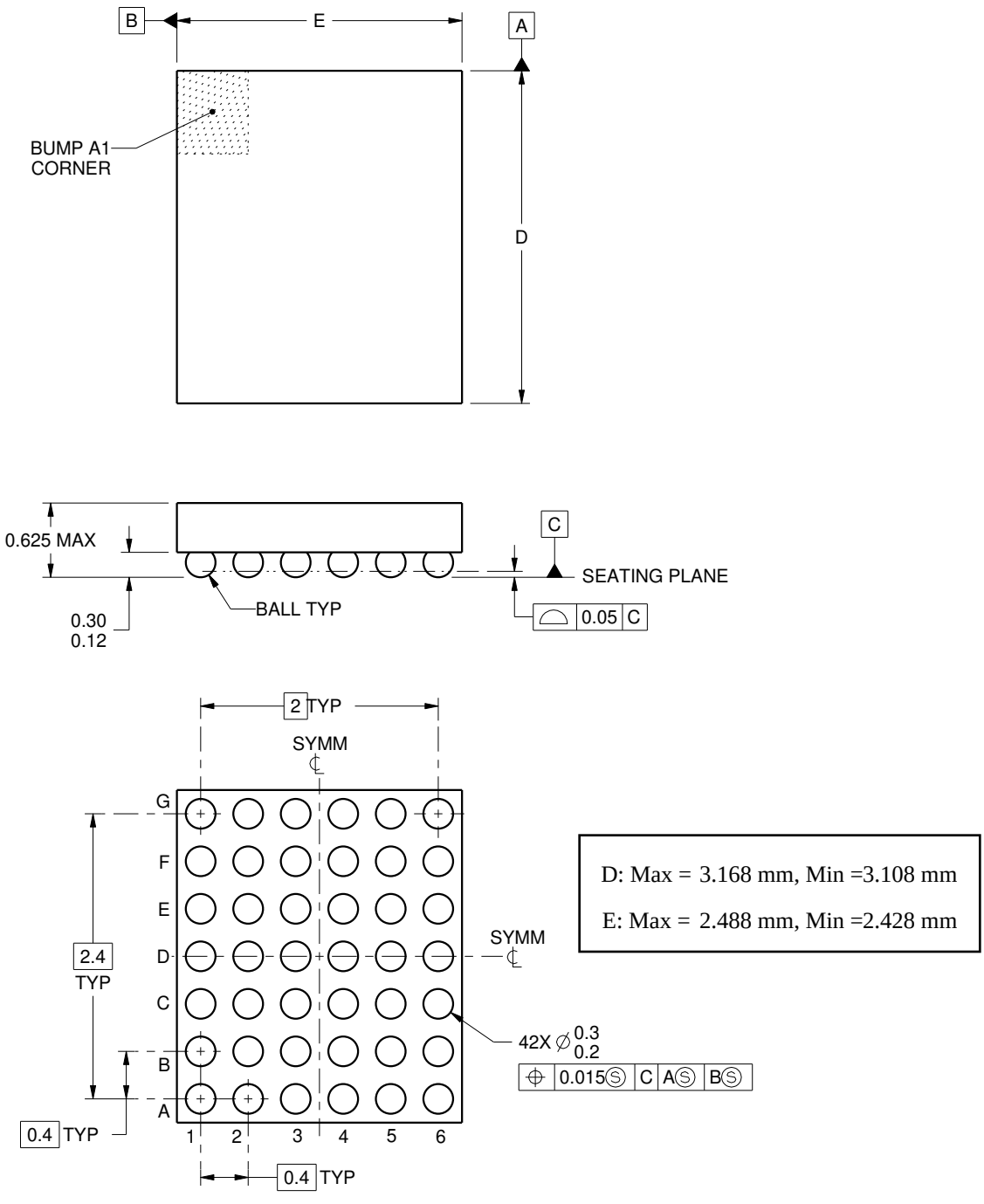
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25871YFFR	DSBGA	YFF	42	3000	335.0	335.0	25.0
BQ25871YFFT	DSBGA	YFF	42	250	335.0	335.0	25.0

PACKAGE OUTLINE

YFF0042

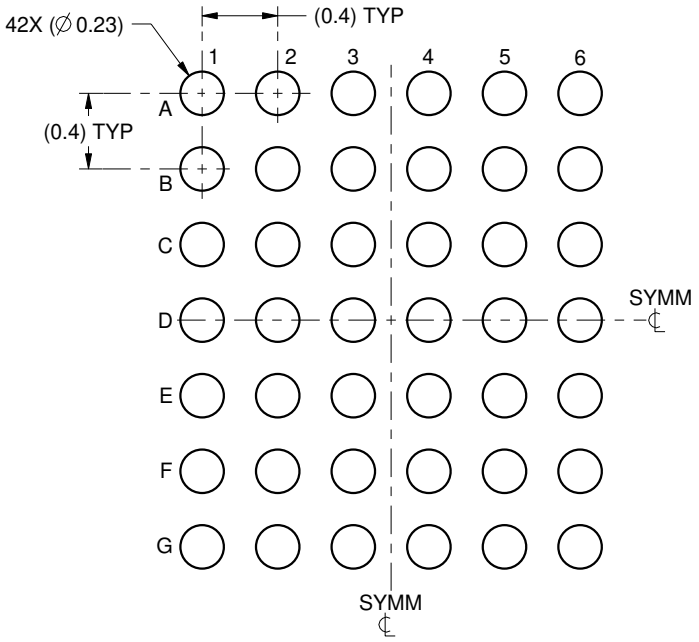
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

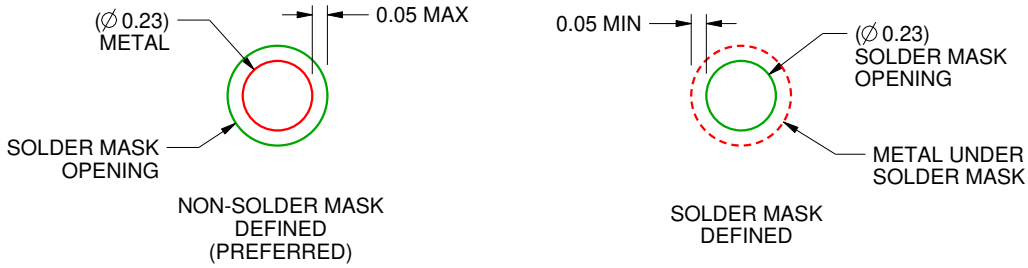


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

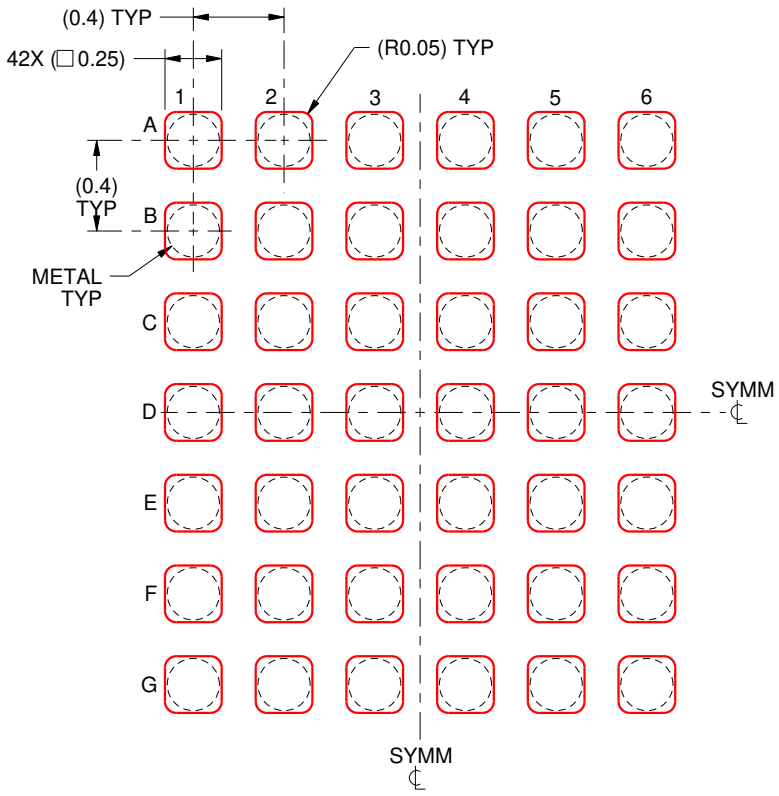


SOLDER MASK DETAILS
NOT TO SCALE

4222067/A 05/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222067/A 05/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265