FAN5242

Voltage Regulator for IMVP-II Notebook Processors

Features

- Powers Intel IMVP-II CPU core
- 0.600V to 1.750V output voltage range
- ±1% reference precision over temperature
- Dynamic VID code change supported
- 5V to 24V input voltage range
- Special controls for Battery Mode and Deeper Sleep Mode
- Meets IMVP-II Load Lines
- High efficiency at all load currents
- Active Droop provides correct load lines
- True differential remote voltage sense
- Current sense uses MOSFETs
- Power Good, Over-current, OV, UVLO
- Space-saving QSOP24

Applications

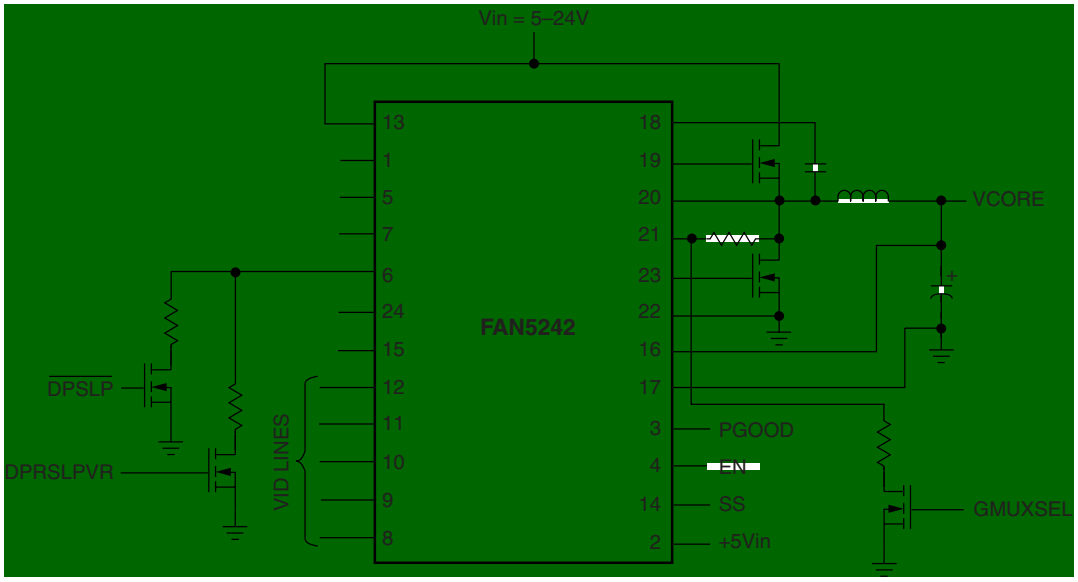
- Notebook CPUs
- Internet appliances

Description

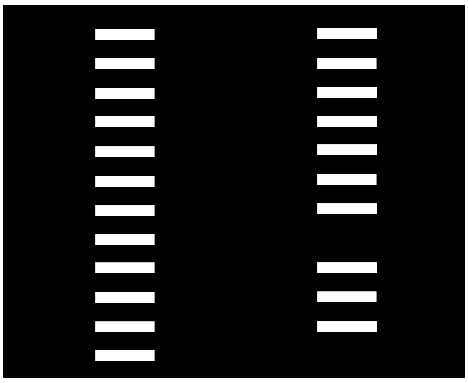
The FAN5242 provides the power, control and protection for the CPU in Intel IMVP-II notebook PC applications. The IC integrates a PWM controller as well as monitoring and protection circuitry into a single 24 lead QSOP package. It provides high efficiency PWM at maximum load and hysteretic conversion at minimum load, and generates Intel specified load lines in both Performance and Battery Mode.

The FAN5242 includes an Intel specified 5-input DAC that adjusts the core PWM output voltage from 600mV to 1.750V in 25mV steps. The DAC setting may be changed during operation, transition occurring in <100µsec. A precision reference, true differential remote sense, and a proprietary architecture with active droop provide excellent static and dynamic core voltage regulation. The FAN5242 includes over-voltage, and over-current protection, and an enable. It is available in a QSOP 24.

Typical Application



Pin Assignments



Pin Description

Pin Number	Pin Name	Pin Function Description
1	AGND	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
2	VCC	**VCC.** Internal IC supply. Connect to system 5V supply, and decouple with a 0.1µF ceramic capacitor.
3	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is not within ±10% of the nominal output voltage setpoint.
4	ENABLE	**Output Enable.** A logic LOW on this pin will disable the output. An internal current source allows for open collector control.
5	FPWM	**Forced PWM.** A logic HIGH on this pin forces the converter to remain in PWM mode.
6	SLP	**Sleep Input.** A resistor to ground on this pin overrides the VID settings.
7	FREQ	**Frequency Set.** Grounding this pin sets the switching frequency to 300KHz. Attaching it to VCC sets the frequency to 600KHz.
8-12	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the range specified in Table 2. Pull-ups are internal to the controller.
13	VBATT	**Battery Voltage Input.** Connect to the main power source.
14	SS	**Soft Start.**
15	ILIM	**Current Limit.** A resistor from this pin to ground sets the over current trip level.
16-17	VCORE, $\overline{\text{VCORE}}$	**Voltage Feedback.** Connect these pins to the desired regulation point at the processor for true differential feedback.
18	BOOT	**Bootstrap.** Input supply for high-side MOSFET.
19	HDRV	**High Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
20	SW	**High side driver source and low side driver drain switching node.** Gate drive return for high side MOSFET, and negative input for low-side MOSFET current sense.
21	ISNS	**Current Sense.** Connect this pin to the SW node through a resistor to sense output current.
22	PGND	**Power Ground.** Return pin for high currents flowing in low-side MOSFET. Connect directly to low-side MOSFET source.
23	LDRV	**Low Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
24	PVCC	**Power VCC.** Provides power to drive low-side MOSFET.

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage:			6.5	V
VBATT			27	V
BOOT, SW, HDRV Pins			33	V
BOOT to SW			6.5	V
All Other Pins	–0.3		VCC+0.3	V
Junction Temperature (T_J)	–10		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VBATT		5		24	V
Ambient Temperature (T_A)		–10		85	°C

Electrical Specifications

(VCC = 5V, VBATT = 5V–24V, and T_A = recommended operating ambient temperature range using circuit of Figure 1 unless otherwise noted.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
VCC Current	Operating, C_L = 10pF		2.7	3.2	mA
	Shut-down (ENABLE=0)		6	30	µA
VBATT Current	Operating		12	20	µA
	Shut-down (ENABLE=0)			1	µA
UVLO Threshold	Rising VCC	4.3	4.65	4.75	V
	Falling	4.1	4.35	4.45	V
Regulator / Control Functions					
Output voltage	per Table 1. Output Voltage VID	0.6		1.75	V
Initial Accuracy		–1		1	% VID
Static Load Regulation		–2		2	% VID
Error Amplifier Gain			86		dB
Error Amplifier GBW			2.7		MHz
Error Amplifier Slew Rate			1		V/µS
ILIM Voltage	R_{ILIM} = 30KΩ	0.89		0.91	V
Over-voltage Threshold		1.9	1.95	2.0	V
Over-voltage Protection delay		1.6		3.2	µS
Under-voltage Shutdown	Disabled during VID code change	72	75	78	% VID
Under-voltage Delay		1.2		1.6	µS
ENABLE, input threshold	Logic LOW			1.2	V
	Logic HIGH	2			V

Electrical Specifications(Continued)

(VCC = 5V, VBATT = 5V–24V, and T_A = recommended operating ambient temperature range using circuit of Figure 1 unless otherwise noted.)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Drivers					
HDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		1.6	3	Ω
LDRV Output Resistance	Sourcing		3.8	5	Ω
	Sinking		0.8	1.5	Ω
Oscillator					
Frequency	FREQ = HIGH	255	300	345	KHz
	FREQ = LOW	510	600	690	KHz
Ramp Amplitude, pk–pk	VBATT = 16V		2		V
Ramp Offset			0.5		V
Ramp Gain	$\frac{\text{Ramp amplitude}}{\text{VIN}}$		125		mV/V
Reference, DAC and Soft-Start					
VID input threshold	Logic LOW			1.21	V
	Logic HIGH	1.62			V
VID pull-up current	to internal 2.5V reference		12		µA
DAC output accuracy		–1		1	%
Soft Start current (I_{SS})	at start-up, V_{SS}.< 0.5	20	26	32	µA
	at start-up, 1.75 > V_{SS}.> 0.5	350	500	650	µA
SLP Current Source		9.5	10	10.5	µA
SLP to VID mode threshold		1.71	1.75	1.78	V
PWRGD					
VCORE Upper Threshold		123		127	% VID
VCORE Lower Threshold	Falling Edge	77		81	% VID
	Rising Edge	87		94	% VID
PWRGD Output Low	I_{PWRGD} = 4mA		0.5		V
Leakage Current	V_{PULLUP} = 5V			1	µA

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
1	1	1	1	1	0.600
1	1	1	1	0	0.625
1	1	1	0	1	0.650
1	1	1	0	0	0.675
1	1	0	1	1	0.700
1	1	0	1	0	0.725
1	1	0	0	1	0.750
1	1	0	0	0	0.775
1	0	1	1	1	0.800
1	0	1	1	0	0.825
1	0	1	0	1	0.850
1	0	1	0	0	0.875
1	0	0	1	1	0.900
1	0	0	1	0	0.925
1	0	0	0	1	0.950
1	0	0	0	0	0.975
0	1	1	1	1	1.000
0	1	1	1	0	1.050
0	1	1	0	1	1.100
0	1	1	0	0	1.150
0	1	0	1	1	1.200
0	1	0	1	0	1.250
0	1	0	0	1	1.300
0	1	0	0	0	1.350
0	0	1	1	1	1.400
0	0	1	1	0	1.450
0	0	1	0	1	1.500
0	0	1	0	0	1.550
0	0	0	1	1	1.600
0	0	0	1	0	1.650
0	0	0	0	1	1.700
0	0	0	0	0	1.750

1 - Logic High or open, 0 = Logic Low

Application Circuit

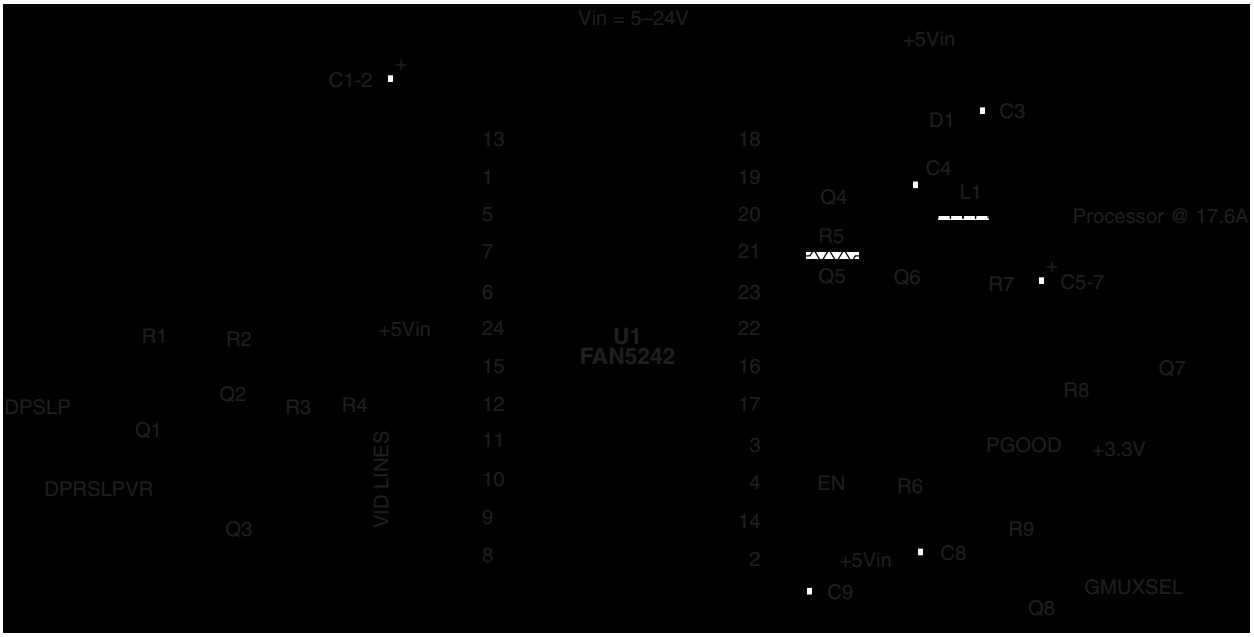


Figure 1. FAN5242 IMVP-II Application Circuit

Table 2. FAN5242 Application Bill of Materials

Reference	Manufacturer, Part #	Quantity	Description	Comments
C1-2	AVX TPSV686*025#0150	2	68µF, 25V Tantalum	
C3, C9	Any	2	1µF Ceramic	
C4, C8	Any	2	220nF, Ceramic	
C5-7	Panasonic EEFUE0D271R	3	270µF, Polymer	
R1, R6	Any	2	10KΩ	
R2	Any	1	117.3KΩ, 1%	
R3	Any	1	698Ω, 1%	
R4	Any	1	2.74KΩ, 1%	
R5	Any	1	5.62KΩ, 1%	
R7	Any	1	10Ω, 1%	
R8	Any	1	1.69KΩ, 1%	
R9	Any	1	TBD KΩ, 1%	
D1	Fairchild MBRD0520	1	0.5A, 20V Schottky	
L1	Coiltronics DR127-1R0	1	1.0µH, 16A Inductor	R < 2.5mΩ
Q1-3, Q8	Fairchild FDV301N	4	N MOSFET	SOT-23
Q4	Fairchild FDS6690A	1	30V N MOSFET	R = 17mΩ
Q5-6	Fairchild FDS6680S	2	30V N MOSFET w/ Schottky	R = 17mΩ
Q7	Fairchild FDV302P	1	P MOSFET	SOT-23
U1	Fairchild FAN5242	1	CPU Controller	

Applications Information

Overview

The FAN5242 is a high efficiency and high precision DC/DC controller for IMVP-II powered notebooks and other portable applications. It provides the voltage necessary for portable applications' processor core. The core voltage is programmed with a 5-bit VID. Utilization of both input and output voltage feedback, and summing-mode compensation, allows for fast loop response over a wide range of input and output variations. This scheme has a superior range of output current operation and is free of the light load instabilities typical of current mode. The IC design allows for a minimum size design of magnetics and discrete transistors for minimum cost and space at maximum performance. Active droop on the CPU output also minimizes the number of output capacitors required. Also included are a number of additional features to make design straightforward, including a pin to set the core voltage during Deep Sleep and Deeper Sleep.

Power Architecture

The power output of the FAN5242 is generated from the unregulated input voltage using synchronous buck converters. Both the high-side and the low-side MOSFET are N-channels to maximize efficiency.

The power output has a pin for setting output overcurrent; two pins for remote voltage-sense feedback; a pin that generates a softstart; and an enable pin that can be used to shutdown the converter.

Loop Description

The control loop of the FAN5242 uses summing-mode control, and requires no external compensation. The control loop measures the current differentially across its low-side MOSFET, subtracting it from the ground voltage, and subtracts the sum from the reference voltage. In addition, it uses voltage feed-forward to guarantee loop rejection of input voltage variation: the ramp amplitude is varied as a function of the input voltage.

Compensation of the control loop amounts to merely selecting suitable output capacitors. Most selections of common Tantalum capacitors will result in a stable loop with adequate phase margin, as will Oscons or Polycaps.

Current Limit

The converter senses the voltage across the low-side N-channel MOSFET (from the SW pin to ground) and compares it to the voltage across a resistor from SW to the ISNS pins; it can also use a discrete resistor in series with the low-side MOSFET for precision. If the voltage drop exceeds the setpoint, the softstart capacitor is discharged, forcing the converter to re-softstart.

Selection of a current-limit resistor must include the tolerance of the current-limit trip point, the MOSFET $R_{DS,on}$ tolerance and temperature coefficient, and the ripple current, in addition to the maximum output current.

Example: Maximum DC output current is 18A, and the inductor is 1.0µH at this current. The MOSFETs have a cumulative $R_{DS,on}$ = 8.5mΩ at V_{GS} = 4.5V, and will be running at 100°C, at which its resistance is 30% higher than at 25°C.

Peak current is DC output current plus peak ripple current:

$$I_{pk} = I_{DC} + \frac{TV_o}{2L} = 18A + \frac{4\mu sec \times 1.25V}{2 \times 1\mu H} = 21A$$

where T is the maximum period, V_O is output voltage, and L is the inductance. The voltage across the MOSFET at this current is

$$V = I_{pk} \times R_{DS,on} \times TC = 21A \times 8.5m\Omega \times 1.3$$
$$= 230mV$$

The current source driving the external resistor is 100µA minimum, so we must use

$$R \geq \frac{V}{I} = \frac{230mV}{100\mu A} = 2.39k\Omega$$

Softstart Timing

Softstart of the converter is accomplished by attaching a capacitor to the SS pin.

Example: To get approximately a 1msec softstart, select a

$$C = \frac{It}{V} = \frac{10\mu A \times 1msec}{1V} = 10nF$$

capacitor.

Light Load Mode

Because the converter is a synchronous buck, it can operate in two quadrants, which means that the ripple current is a constant independent of the load current. At light loads, this ripple current translates into poor efficiency, since it causes circulating current losses in the MOSFETs. To optimize the efficiency at light loads, then, the FAN5242 switches from normal operation to a special light load when the current is low. Light load occurs when the on-state drain-source voltage is less than about 17mV.

In light load mode, the FAN5242 switches from PWM (pulse width modulation) to PFM (pulse frequency modulation), which reduces the gate drive current. It also turns off the low side drive completely, which further saves on gate current; in

this mode, the converter operates non-synchronously, using the output schottky. The switch to this mode of operation can be avoided by pulling the FPWM pin to VCC.

Setting the Switching Frequency

Connecting the FREQ pin to ground sets the switching frequency to 300KHz. Connecting the FREQ pin to VCC sets the switching frequency to 600KHz.

Setting the Voltage with SLP

Deep Sleep and Deeper Sleep voltages can be set with the SLP pin. When the SLP pin is open, the output voltage of the converter is set by the VID pins. When the SLP pin has a resistor to ground, the output voltage of the converter will be equal to 10µA × R. Thus, the DEEPSLEEP voltage of 1.173V can be obtained by turning on a switch with a 117.3KΩ resistor to ground, and the DEEPERSLEEP voltage of 700mV can be obtained by turning on a switch with a 698Ω resistor to ground.

Setting the Load Line with ISNS

The load line can be set with a resistor between the switching node of the power MOSFETs and the ISNS pin, and further adjusted with a resistor from the ISNS pin to ground. The schematic of Figure 3 shows how to obtain the nominal Performance Mode load line of 4mV/A, and how to use a switch connected to the GMUXSEL signal to obtain the Battery Mode load line of 3mV/A.

The ISNS pin can be quite sensitive to stray capacitance, and so it is important to use a low capacitance switch for the resistor to ground, such as the Fairchild FDV301N shown in the Figure.

Overvoltage Protection

When the output voltage of the converter exceeds approximately 120% of nominal, it enters into over-voltage protection, with the goal of protecting the load from damage. In over-voltage protection, the high-side MOSFET is turned off and the low-side MOSFET is turned on, crowbarring the output. Once over-voltage protection is triggered, it remains on until power is recycled.

Power good

Power good is asserted when the output is within its specified tolerance.

ENABLE

The ENBL pin does the on/off control. Pulling this pin low turns off the converter.

Thermal shutdown

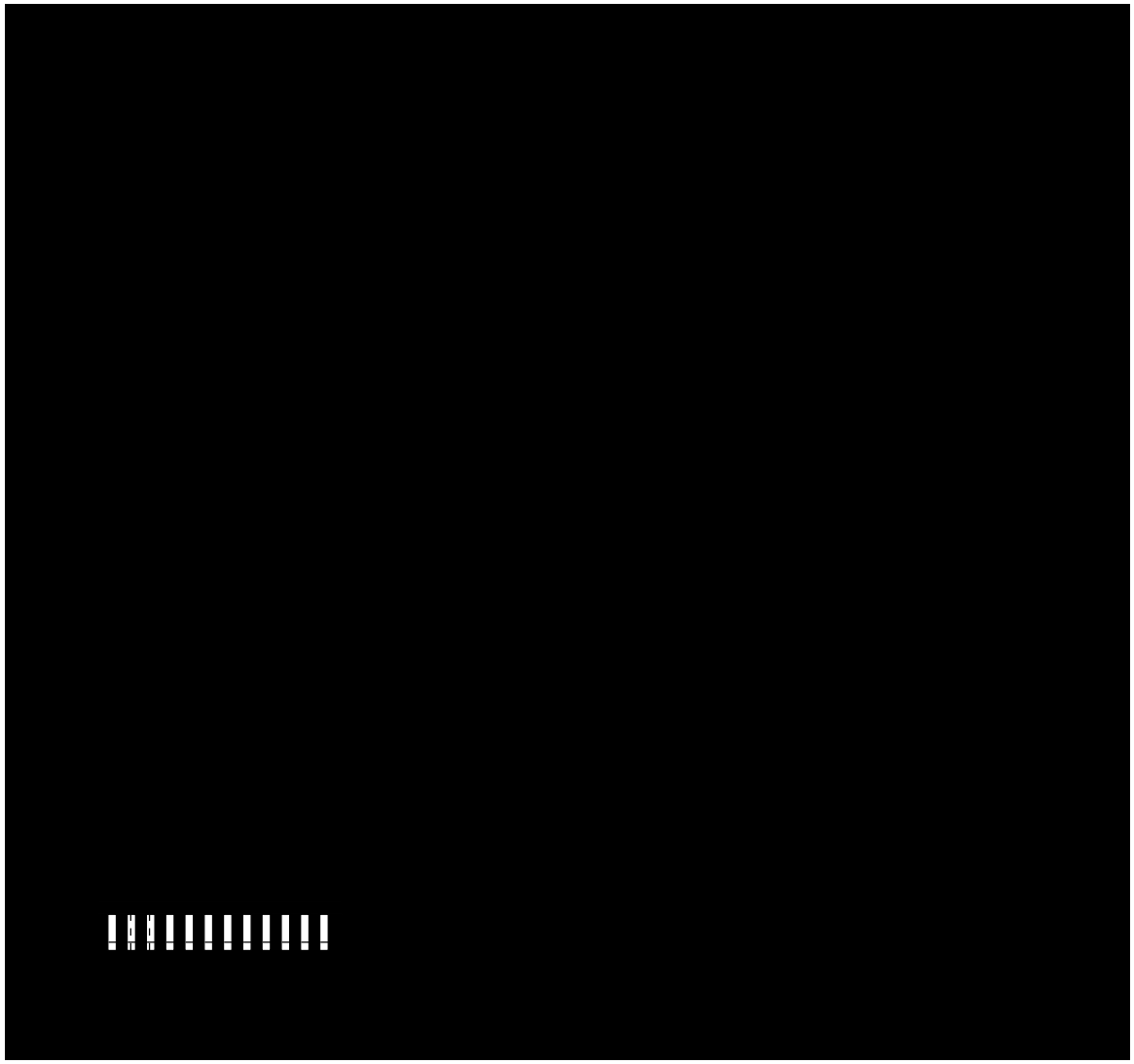
If the die temperature of the FAN5242 exceeds safe limits, the IC shuts itself off.

UVLO

If the input voltages falls below the UVLO threshold, the FAN5242 turns itself off.

Mechanical Dimensions

24 Lead QSOP



Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5242QSC	0°C to 85°C	QSOP-24	Rails
FAN5242QSCX	0°C to 85°C	QSOP-24	Tape and Reel

1/24/02 0.0m 001
Stock#DS30005242