PHK5NQ15T

N-channel TrenchMOS standard level FET

2 August 2013 — Product data sheet

1. General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Low conduction losses due to low on-state resistance

3. Applications

- DC-to-DC convertors switching
- General purpose switching

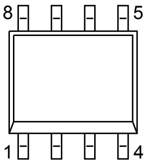
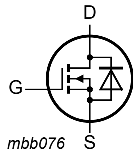
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-	150	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; Fig. 1; Fig. 3		-	-	5	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Fig. 2		-	-	6.25	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 9; Fig. 10		-	56	75	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 5 A; V_{DS} = 75 V; T_j = 25 °C; Fig. 11		-	12	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **SO8 (SOT96-1)**	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHK5NQ15T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PHK5NQ15T	K5NQ15T

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	150	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; R_{GS} = 20 kΩ		-	150	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	T_{sp} = 100 °C; V_{GS} = 10 V; Fig. 1		-	3.23	A
		T_{sp} = 25 °C; V_{GS} = 10 V; Fig. 1; Fig. 3		-	5	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	20	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Fig. 2		-	6.25	W

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
Source-drain diode						
I_S	source current	T_{sp} = 25 °C		-	5	A
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs		-	20	A

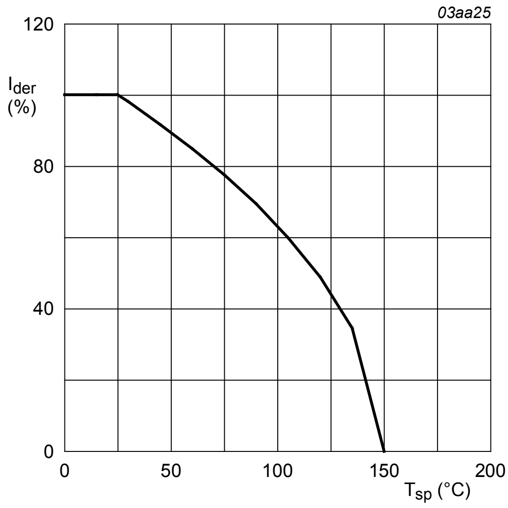


Fig. 1. Normalized continuous drain current as a function of solder point temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

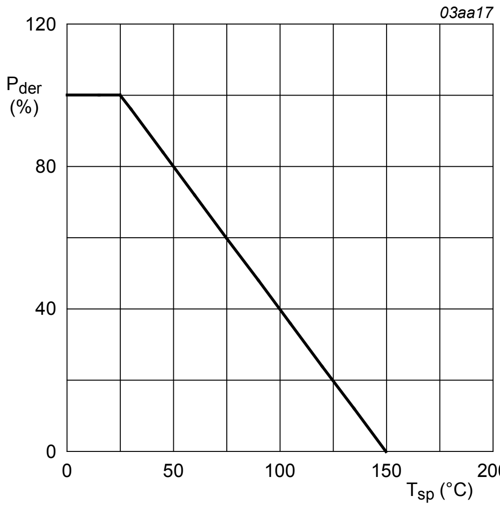


Fig. 2. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

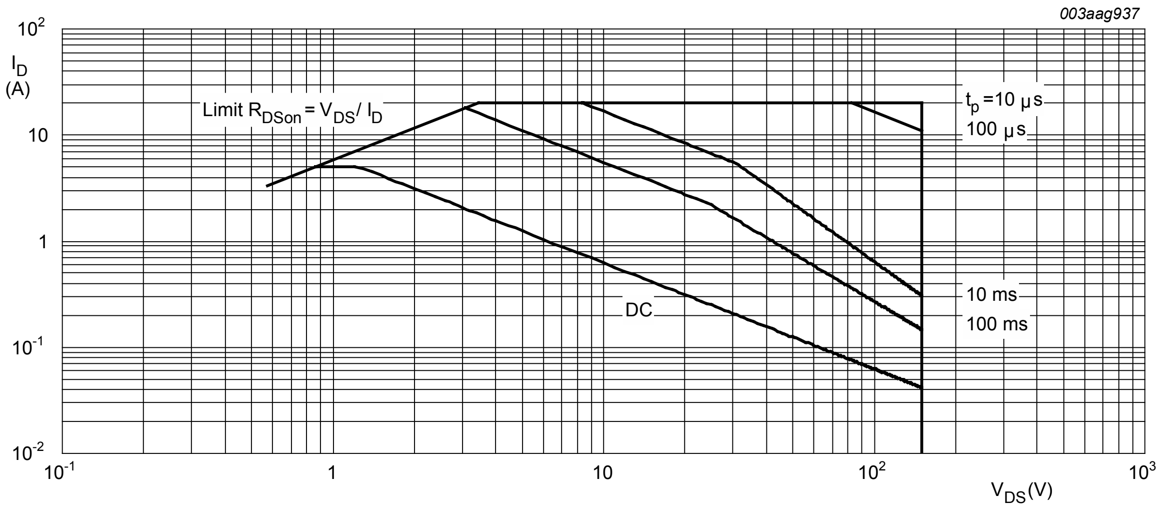


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25°C;\ I_{DM} \text{ is a single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4		-	-	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on printed-circuit board		-	70	-	K/W

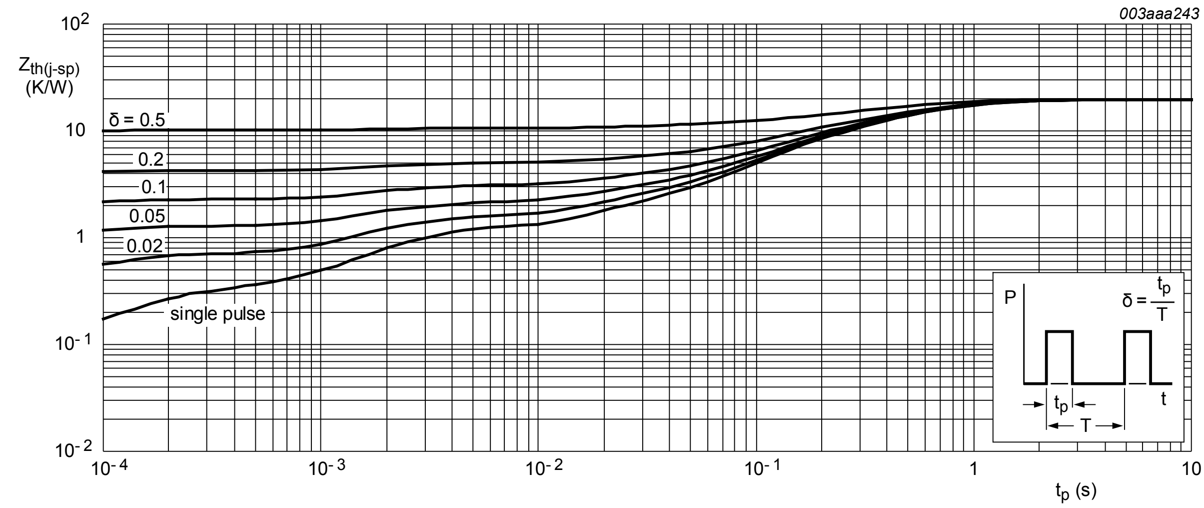


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		134	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		150	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 8		-	-	4.5	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; Fig. 8		1.2	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 8		2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 120 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 120 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 150 °C; Fig. 9; Fig. 10		-	129	173	mΩ
		V_{GS} = 5 V; I_D = 3 A; T_j = 25 °C		-	60	80	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 9; Fig. 10		-	56	75	mΩ
R_G	gate resistance	f = 1 MHz		-	1.9	3.8	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 75 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11		-	29	41	nC
Q_{GS}	gate-source charge			-	3	-	nC
Q_{GD}	gate-drain charge			-	12	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 12		-	1150	1553	pF
C_{oss}	output capacitance			-	187	252	pF
C_{rss}	reverse transfer capacitance			-	61	85	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 75 V; R_L = 15 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C; I_D = 5 A		-	12	-	ns
t_r	rise time			-	12	-	ns
$t_{d(off)}$	turn-off delay time			-	35	-	ns
t_f	fall time			-	18	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 13		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 90 V; T_j = 25 °C		-	87	113	ns
Q_r	recovered charge			-	162	-	nC

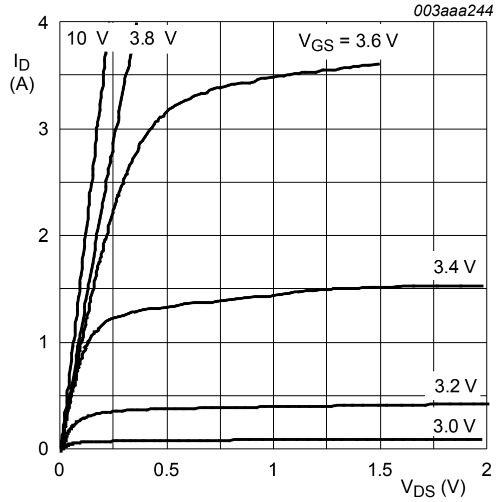


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

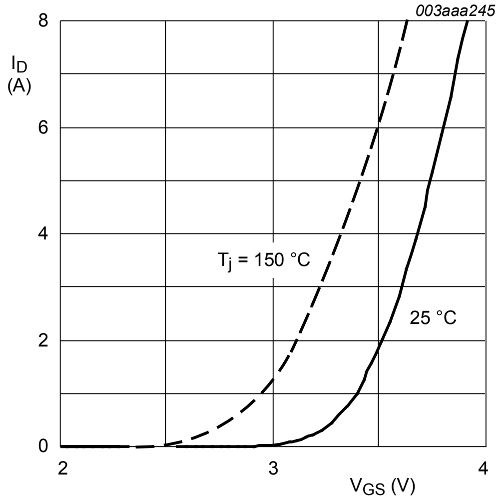


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$T_j = 25°C$ and $150°C; V_{DS} > I_D \times R_{DSon}$

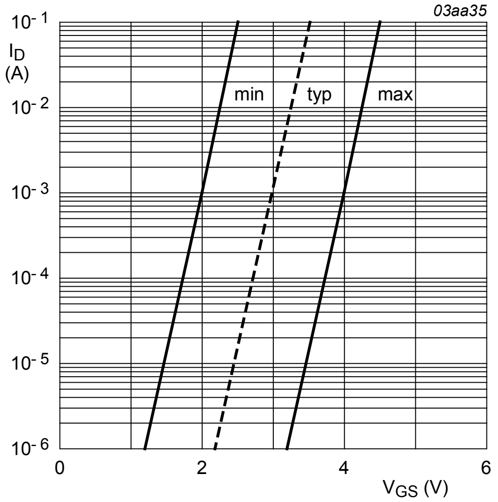


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C; V_{DS} = 5V$

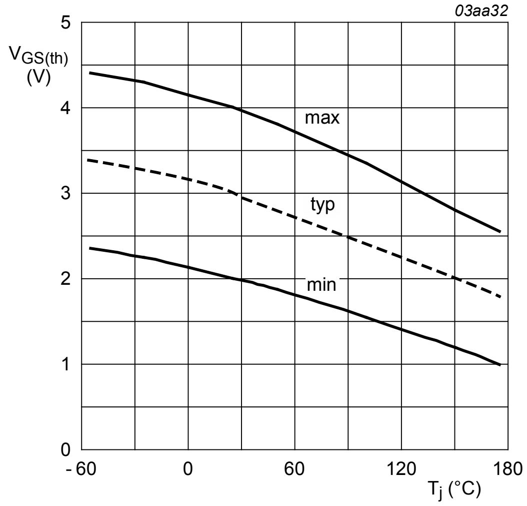


Fig. 8. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

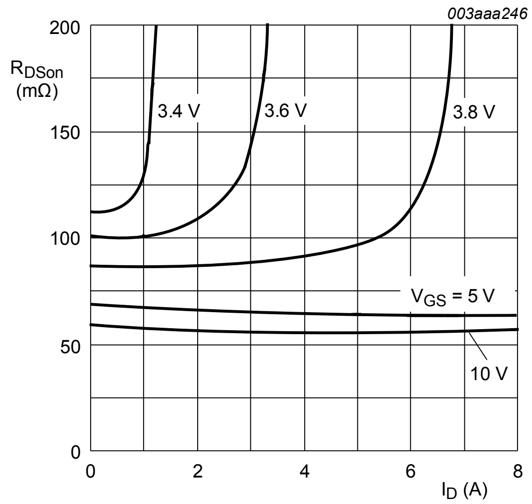


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

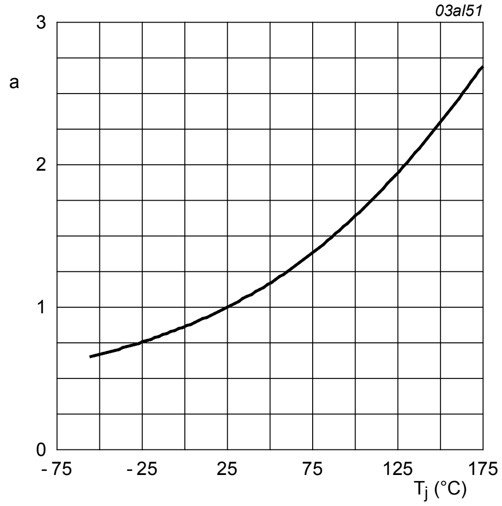


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

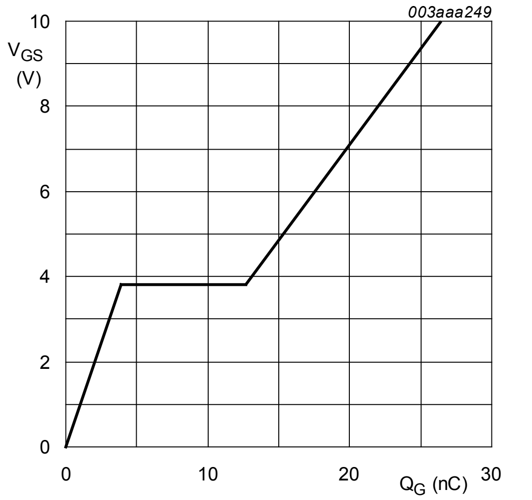


Fig. 11. Gate-source voltage as a function of gate charge; typical values

$I_D = 5A; V_{DD} = 75V$

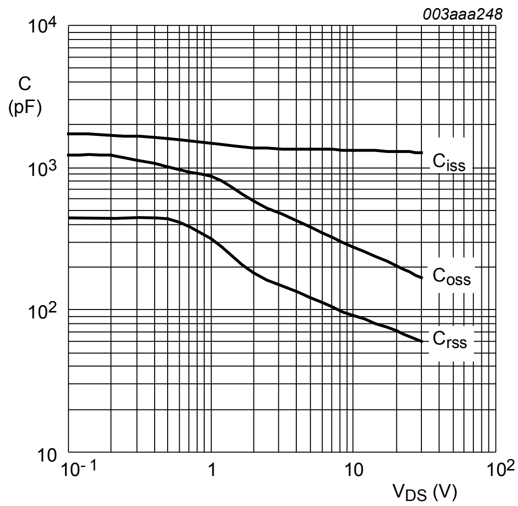


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

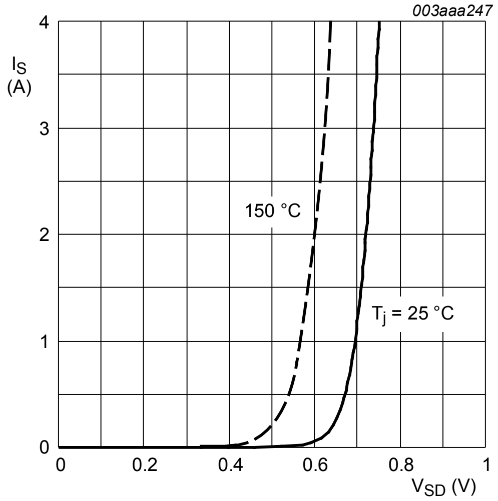
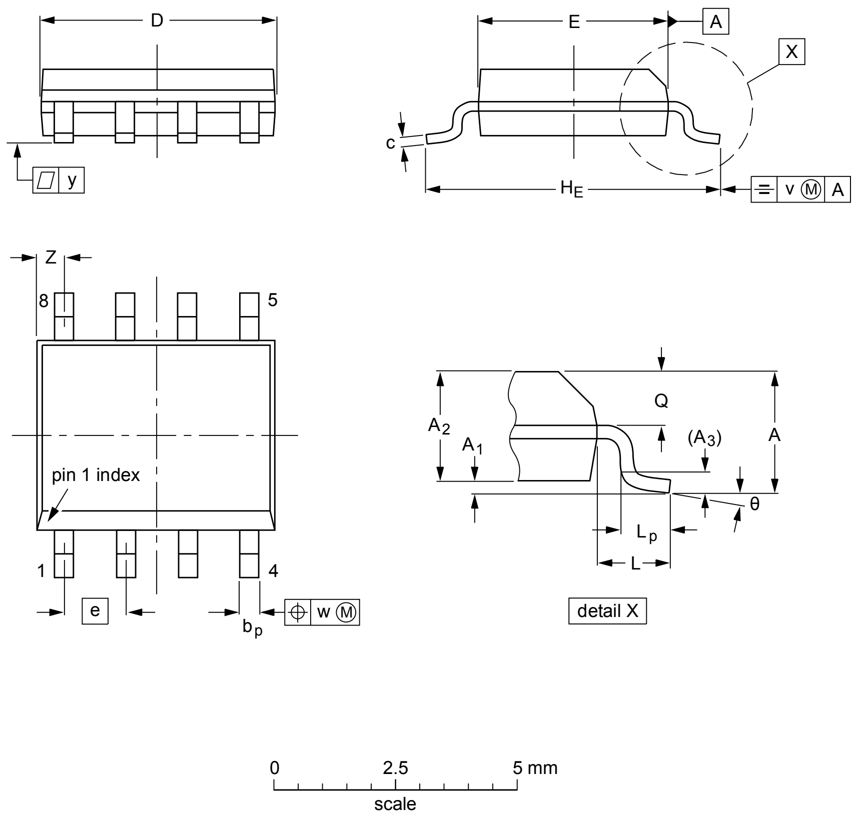


Fig. 13. Source current as a function of source-drain voltage; typical values

$T_j = 25°C$ and $150°C; V_{GS} = 0V$

11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

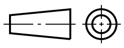
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig. 14. Package outline SO8 (SOT96-1)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

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