THIS SPEC IS OBSOLETE

Spec No: 001-98940

Spec Title: S6E2H1 SERIES 32-BIT ARM(R) CORTEX(R)-M4F, FM4 MICROCONTROLLER

Replaced by: NONE

S6E2H1 Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

Devices in the S6E2H1 Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. These series is based on the ARM Cortex-M4F Processor with on-chip Flash memory and SRAM. The series has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN).

Features

32-bit ARM Cortex-M4F Core

- Processor version: r0p1
- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

- Flash memory

These series are based on two independent on-chip Flash memories.

  - MainFlash memory
    - Up to 512 Kbytes
    - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
    - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
    - Security function for code protection
  - WorkFlash memory
    - 32 Kbytes
    - Read cycle:
    - 6 wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4 wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2 wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0 wait-cycle: the operation frequency up to 40 MHz
    - Security function is shared with code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

  - SRAM0: Up to 32 Kbytes
  - SRAM1: Up to 16 Kbytes
  - SRAM2: Up to 16 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to prepare the dedicated software library to use the scramble function.

Multi-function Serial Interface (Max 8 channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)

- Supports high-speed SPI (ch.4 and ch.6 only)
- Data length 5 to 16-bit

■ LIN
- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can change to 13 to 16-bit length)
- LIN break delimiter generation (can change to 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

■ I^2C
- Standard mode (Max 100 kbps) / High-speed mode (Max 400 kbps) supported
- Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

■ 8 independently configured and operated channels

■ Transfer can be started by software or request from the built-in peripherals

■ Transfer address area: 32-bit (4 Gbytes)

■ Transfer mode: Block transfer/Burst transfer/Demand transfer

■ Transfer data type: bytes/half-word/word

■ Transfer block count: 1 to 16

■ Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels) [12-bit A/D Converter]

■ Successive Approximation type

■ Built-in 3 units

■ Conversion time: 0.5 µs @ 5 V

■ Priority conversion available (priority at 2 levels)

■ Scanning conversion mode

■ Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

DA Converter (Max 2 channels)

■ R-2R type

■ 12-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

■ 16-bit PWM timer

■ 16-bit PPG timer

■ 16-/32-bit reload timer

■ 16-/32-bit PWC timer

■ Event counter mode (external clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

■ Capable of pull-up control per pin

■ Capable of reading pin level directly

■ Built-in the port relocate function

■ Up to 100 high-speed general-purpose I/O ports @ 120 pin Package

■ Some pin is 5 V tolerant I/O.
See 4. Pin Description and 5. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

Minimum resolution: 6.25 ns

■ 16-bit free-run timer × 3ch./unit

■ Input capture × 4ch./unit

■ Output compare × 6ch./unit

■ A/D activation compare × 6ch./unit

■ Waveform generator × 3ch./unit

■ 16-bit PPG timer × 3ch./unit

The following function can be used to achieve the motor control.

■ PWM signal output function

■ DC chopper waveform output function

■ Dead time function

■ Input capture function

■ A/D convertor activate function

■ DTIF (Motor emergency stop) interrupt function

Real-time Clock (RTC)
The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)
The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)
The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter
The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
  - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

Watchdog Timer (2 channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

Hardware watchdog timer is clocked by low-speed internal CR oscillator. Therefore, Hardware watchdog is active in any power saving mode except Stop.

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset
[Clocks]
Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

Clock SuperVisor (CSV)
Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)
This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode
Six low-power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)

- Deep standby stop (selectable from with/without RAM retention)

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register : 32 bytes
- Port circuit

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

Two Power Supplies

- Wide range voltage: VCC = 2.7 V to 5.5 V
- Power supply for VBAT: VBAT = 2.7 V to 5.5 V

Table of Contents

1. Product Lineup

Memory Size

Product name	S6E2H14E0A S6E2H14F0A S6E2H14G0A	S6E2H16E0A S6E2H16F0A S6E2H16G0A
MainFlash memory	256 Kbytes	512 Kbytes
WorkFlash memory	32 Kbytes	32 Kbytes
On-chip SRAM	32 Kbytes	64 Kbytes
SRAM0	16 Kbytes	32 Kbytes
SRAM1	8 Kbytes	16 Kbytes
SRAM2	8 Kbytes	16 Kbytes

Function

Product name		S6E2H14E0A S6E2H16E0A	S6E2H14F0A S6E2H16F0A	S6E2H14G0A S6E2H16G0A
Pin count		80	100	120/121
CPU		Cortex-M4F, MPU, NVIC 128ch.		
	Freq.	160 MHz		
Power supply voltage range		2.7V to 5.5V		
DMAC		8ch.		
DSTC		256ch.		
External Bus Interface		Addr:19-bit (Max), R/W data: 8-bit (Max), CS:5 (Max), SRAM, NOR Flash	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, SDRAM	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, NAND Flash, SDRAM
Multi-function Serial Interface (UART/CSIO/LIN/I²C)		8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)		8ch. (Max)		
MF Timer	A/D activation compare	6ch.	3 units (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC		3ch. (Max)		
Dual Timer		1 unit		
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog Timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		16 pins (Max) + NMI × 1		
I/O Ports		63 pins (Max)	80 pins (Max)	100 pins (Max)
12-bit A/D Converter		16ch. (3 units)	24ch. (3 units)	
12-bit D/A Converter		2 units (Max)		
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz (±2%)		
	Low-speed	100 kHz (Typ)		
Debug Function		SWJ-DP/ETM		
Unique ID		Yes		

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-in CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

Product Name / Package	S6E2H14E0A S6E2H16E0A	S6E2H14F0A S6E2H16F0A	S6E2H14G0A S6E2H16G0A
LQFP: LQH080 (0.5-mm pitch)	○	-	-
LQFP: LQI100 (0.5-mm pitch)	-	○	-
LQFP: LQM120 (0.5-mm pitch)	-	-	○
FBGA: FDI121 (0.5-mm pitch)	-	-	○

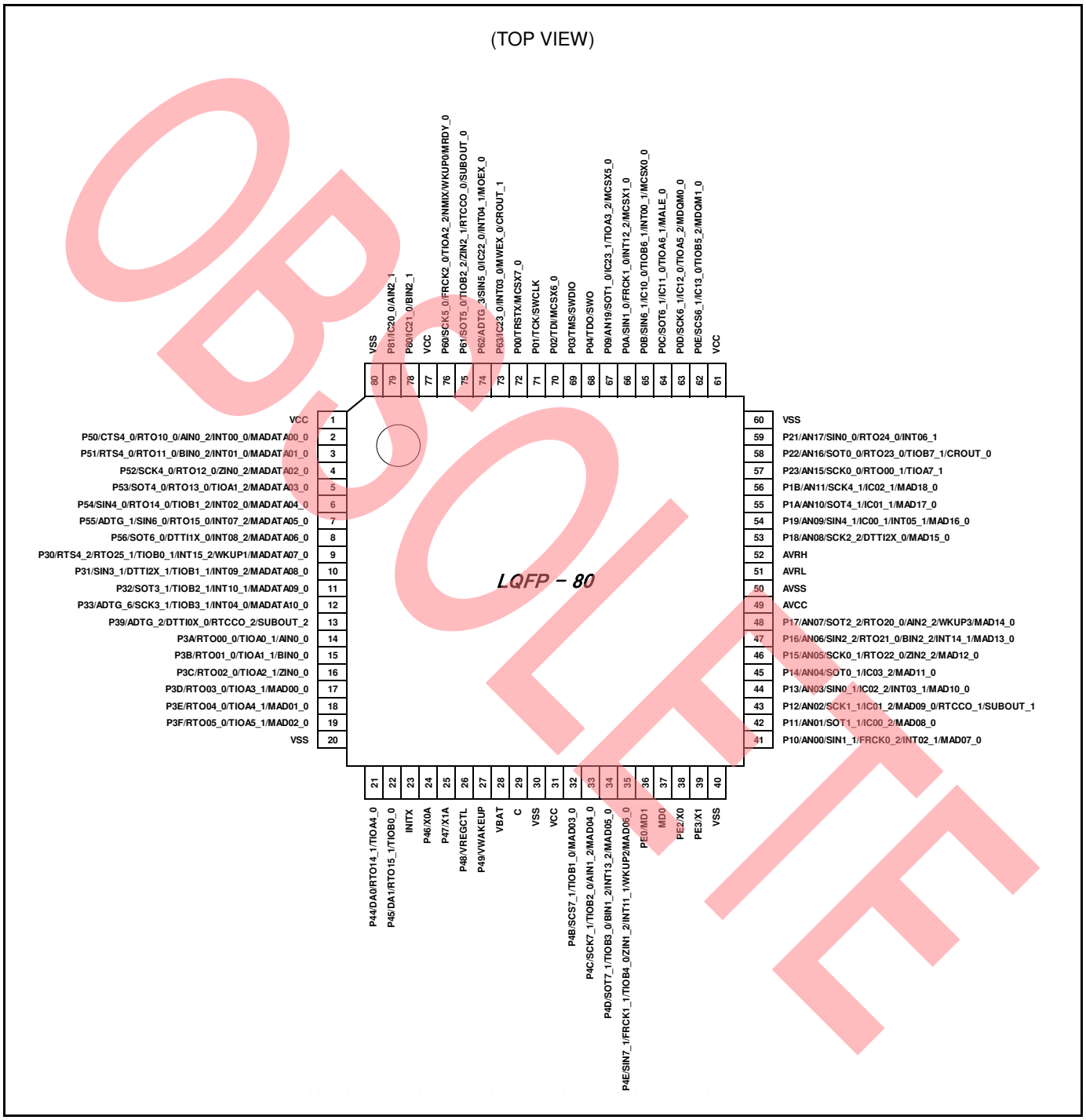
❍: Supported

Note :

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

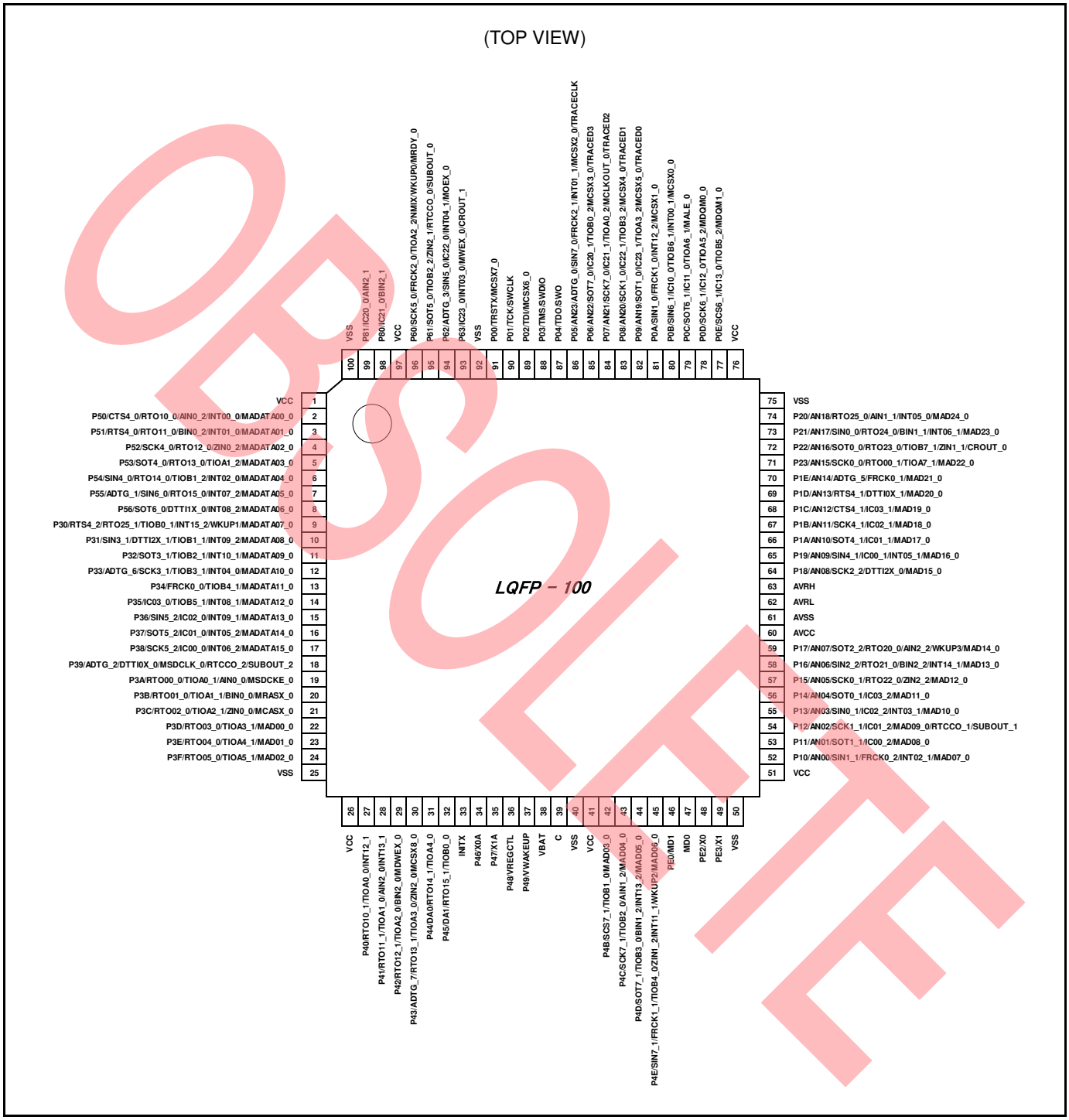
LQH080



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LQI100



Note:

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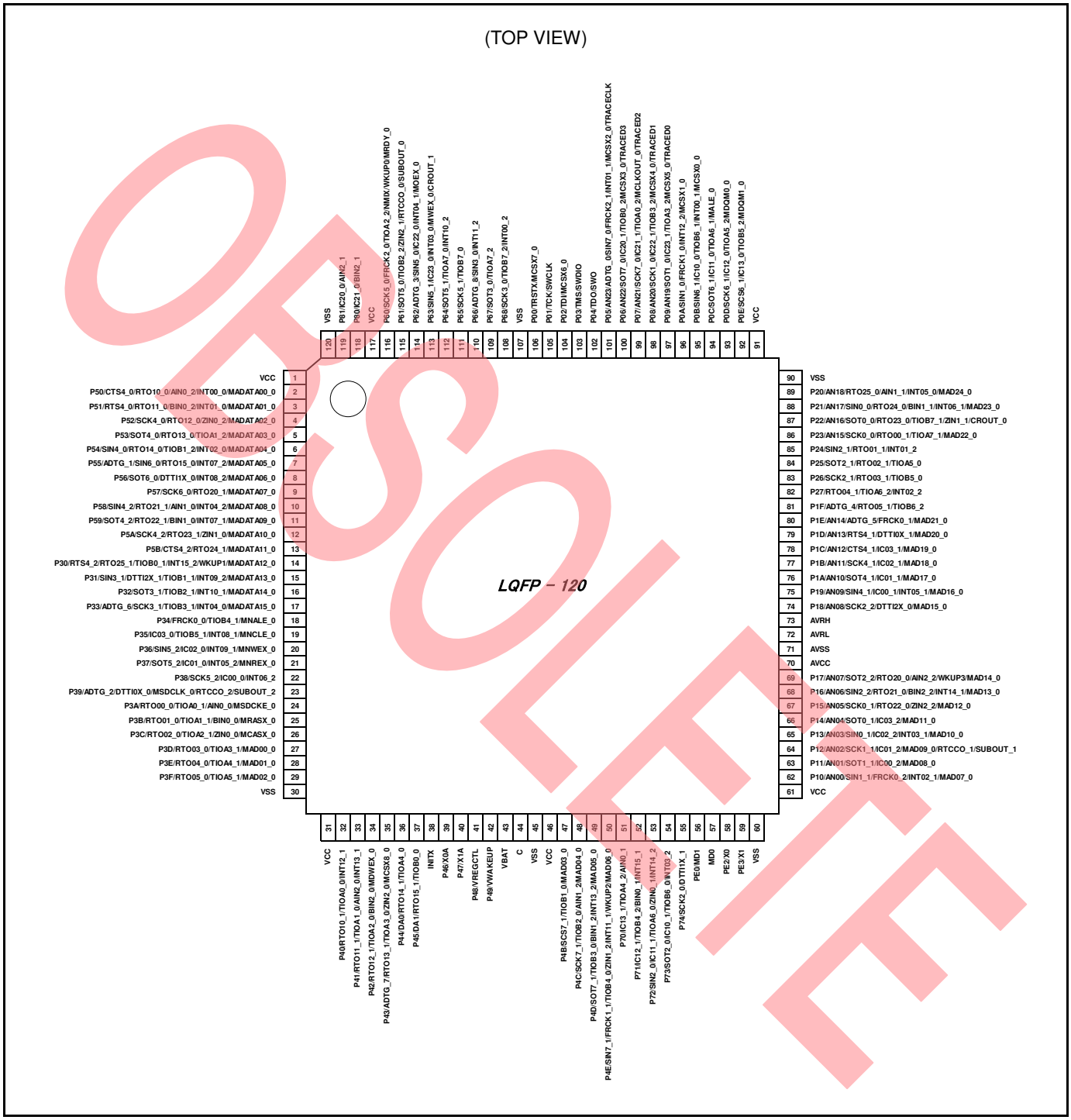
LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

FDI121

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	P81	P80	VCC	TRSTX	VSS	P06	P0A	P0D	VCC	VSS
B	VCC	P60	P61	P63	TCK	TDO	P07	P0B	P0E	P24	P20
C	P50	P51	P62	P64	TDI	TMS	P08	P0C	P25	P22	P21
D	P52	P53	P54	P65	P66	P05	P09	P26	P1E	P1D	P23
E	P30	P55	P56	P57	P67	P68	P27	P1C	P1B	P1A	P19
F	P34	P33	P32	P31	P58	P59	P1F	P18	P17	P16	AVRH
G	P35	P36	P37	P38	P5A	P5B	P72	P15	P14	P13	AVRL
H	P39	P3A	P3B	P3C	P43	P70	P71	P73	P12	P11	AVSS
J	P3D	P3E	P41	P45	P42	P4B	P4C	P4D	P74	P10	AVCC
K	VCC	P3F	P44	X1A	P48	P49	VCC	P4E	MD0	VSS	VCC
L	VSS	P40	INITX	X0A	VBAT	C	VSS	MD1	X0	X1	VSS

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. Pin Description

List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50	E	K
				CTS4_0		
				AIN0_2		
				RTO10_0 (PPG10_0)		
				INT00_0		
				MADATA00_0		
3	3	3	C2	P51	E	K
				RTS4_0		
				BIN0_2		
				RTO11_0 (PPG10_0)		
				INT01_0		
				MADATA01_0		
4	4	4	D1	P52	E	I
				SCK4_0 (SCL4_0)		
				ZIN0_2		
				RTO12_0 (PPG12_0)		
				MADATA02_0		
5	5	5	D2	P53	E	I
				TIOA1_2		
				SOT4_0 (SDA4_0)		
				RTO13_0 (PPG12_0)		
				MADATA03_0		
6	6	6	D3	P54	E	K
				TIOB1_2		
				SIN4_0		
				RTO14_0 (PPG14_0)		
				INT02_0		
				MADATA04_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
7	7	7	E2	P55 ADTG_1 SIN6_0 RTO15_0 (PPG14_0) INT07_2 MADATA05_0	E	K
8	8	8	E3	P56 SOT6_0 (SDA6_0) DTTI1X_0 INT08_2 MADATA06_0	E	K
9	-	-	E4	P57 SCK6_0 (SCL6_0) MADATA07_0 RTO20_1	E	I
10	-	-	F5	P58 SIN4_2 AIN1_0 INT04_2 MADATA08_0 RTO21_1	E	K
11	-	-	F6	P59 SOT4_2 (SDA4_2) BIN1_0 INT07_1 MADATA09_0 RTO22_1	E	K
12	-	-	G5	P5A SCK4_2 (SCL4_2) ZIN1_0 MADATA10_0 RTO23_1	E	I
13	-	-	G6	P5B CTS4_2 MADATA11_0 RTO24_1	E	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
14	9	9	E1	P30	E	Q
				TIOB0_1		
				RTS4_2		
				INT15_2		
				WKUP1		
-			-	MADATA07_0		
14	-	-	E1	MADATA12_0		
	9	9		RTO25_1		
15	10	10	F4	P31	I	K
				TIOB1_1		
				SIN3_1		
				INT09_2		
-			-	MADATA08_0		
15	-	-	F4	MADATA13_0		
	10	10		DTTI2X_1		
16	11	11	F3	P32	N	K
				TIOB2_1		
				SOT3_1 (SDA3_1)		
				INT10_1		
-			-	MADATA09_0		
16	-	-	F3	MADATA14_0		
17	12	12	F2	P33	N	K
				ADTG_6		
				TIOB3_1		
				SCK3_1 (SCL3_1)		
				INT04_0		
-			-	MADATA10_0		
17	-	-	F2	MADATA15_0		
18	13	-	F1	P34	E	I
				TIOB4_1		
				FRCK0_0		
-			-	MADATA11_0		
18	-	-	F1	MNALE_0		
19	14	-	G1	P35	E	K
				TIOB5_1		
				IC03_0		
				INT08_1		
-			-	MADATA12_0		
19	-	-	G1	MNCLE_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
20	15	-	G2	P36	E	K
				SIN5_2		
				IC02_0		
				INT09_1		
-			-	MADATA13_0		
20	-	-	G2	MNWEX_0		
21	16	-	G3	P37	E	K
				SOT5_2 (SDA5_2)		
				IC01_0		
				INT05_2		
-			-	MADATA14_0		
21	-	-	G3	MNREX_0		
22	17	-	G4	P38	E	K
				SCK5_2 (SCL5_2)		
				IC00_0		
				INT06_2		
-			-	MADATA15_0		
23	18	13	H1	P39	L	I
				ADTG_2		
				DTTI0X_0		
				RTCCO_2		
				SUBOUT_2		
		-		MSDCLK_0		
24	19	14	H2	P3A	G	I
				TIOA0_1		
				AIN0_0		
				RTO00_0 (PPG00_0)		
		-		MSDCKE_0		
25	20	15	H3	P3B	G	I
				TIOA1_1		
				BIN0_0		
				RTO01_0 (PPG00_0)		
		-		MRASX_0		
26	21	16	H4	P3C	G	I
				TIOA2_1		
				ZIN0_0		
				RTO02_0 (PPG02_0)		
		-		MCASX_0		
27	22	17	J1	P3D	G	I
				TIOA3_1		
				RTO03_0 (PPG02_0)		
				MAD00_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
39	34	24	L4	P46 X0A	P	S
40	35	25	K4	P47 X1A	Q	T
41	36	26	K5	P48 VREGCTL	O	U
42	37	27	K6	P49 VWAKEUP	O	U
43	38	28	L5	VBAT	-	-
44	39	29	L6	C	-	-
45	40	30	L7	VSS	-	-
46	41	31	K7	VCC	-	-
47	42	32	J6	P4B TIOB1_0 SCS7_1 MAD03_0	E	I
48	43	33	J7	P4C TIOB2_0 SCK7_1 (SCL7_1) AIN1_2 MAD04_0	N	I
49	44	34	J8	P4D TIOB3_0 SOT7_1 (SDA7_1) BIN1_2 INT13_2 MAD05_0	N	K
50	45	35	K8	P4E TIOB4_0 SIN7_1 ZIN1_2 FRCK1_1 INT11_1 WKUP2 MAD06_0	I	Q
51	-	-	H6	P70 TIOA4_2 AIN0_1 IC13_1	E	I
52	-	-	H7	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
53	-	-	G7	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	H8	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	J9	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	L8	PE0 MD1	C	E
57	47	37	K9	MD0	J	D
58	48	38	L9	PE2 X0	A	A
59	49	39	L10	PE3 X1	A	B
60	50	40	L11	VSS	-	-
61	51	-	K11	VCC	-	-
62	52	41	J10	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0	F	M
63	53	42	H10	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0	F	L
64	54	43	H9	P12 AN02 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1 MAD09_0	F	L

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
65	55	44	G10	P13 AN03 SIN0_1 IC02_2 INT03_1 MAD10_0	F	M
66	56	45	G9	P14 AN04 SOT0_1 (SDA0_1) IC03_2 MAD11_0	F	L
67	57	46	G8	P15 AN05 SCK0_1 (SCL0_1) MAD12_0 ZIN2_2 RTO22_0	F	L
68	58	47	F10	P16 AN06 SIN2_2 INT14_1 MAD13_0 BIN2_2 RTO21_0	F	M
69	59	48	F9	P17 AN07 SOT2_2 (SDA2_2) WKUP3 MAD14_0 AIN2_2 RTO20_0	F	P
70	60	49	J11	AVCC	-	-
71	61	50	H11	AVSS	-	-
72	62	51	G11	AVRL	-	-
73	63	52	F11	AVRH	-	-
74	64	53	F8	P18 AN08 SCK2_2 (SCL2_2) MAD15_0 DTTI2X_0	F	L

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
75	65	54	E11	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	E10	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	E9	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	E8	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	D10	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L
80	70	-	D9	P1E AN14 ADTG_5 FRCK0_1 MAD21_0	F	L
81	-	-	F7	P1F ADTG_4 TIOB6_2 RTO05_1 (PPG04_1)	E	I
82	-	-	E7	P27 TIOA6_2 RTO04_1 (PPG04_1) INT02_2	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
83	-	-	D8	P26 TIOB5_0 SCK2_1 (SCL2_1) RTO03_1 (PPG02_1)	E	I
84	-	-	C9	P25 TIOA5_0 SOT2_1 (SDA2_1) RTO02_1 (PPG02_1)	E	I
85	-	-	B10	P24 SIN2_1 RTO01_1 (PPG00_1) INT01_2	E	K
86	71	57	D11	P23 AN15 TIOA7_1 SCK0_0 (SCL0_0) RTO00_1 (PPG00_1)	F	L
		-		MAD22_0		
87	72	58	C10	P22 CROUT_0 AN16 TIOB7_1 SOT0_0 (SDA0_0)	F	L
		-		ZIN1_1		
		58		RTO23_0		
88	73	59	C11	P21 AN17 SIN0_0	F	M
		-		BIN1_1		
		59		INT06_1		
		-		MAD23_0		
		59		RTO24_0		
89	74	-	B11	P20 AN18 AIN1_1 INT05_0 MAD24_0 RTO25_0	F	M
90	75	60	A11	VSS	-	-

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
91	76	61	A10	VCC	-	-
92	77	62	B9	P0E	L	I
				TIOB5_2		
				SCS6_1		
				IC13_0		
				MDQM1_0		
93	78	63	A9	P0D	L	I
				TIOA5_2		
				SCK6_1 (SCL6_1)		
				IC12_0		
				MDQM0_0		
94	79	64	C8	P0C	L	I
				TIOA6_1		
				SOT6_1 (SDA6_1)		
				IC11_0		
				MALE_0		
95	80	65	B8	P0B	L	K
				TIOB6_1		
				SIN6_1		
				IC10_0		
				INT00_1		
				MCSX0_0		
96	81	66	A8	P0A	L	K
				SIN1_0		
				FRCK1_0		
				INT12_2		
				MCSX1_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
97	82	67 - 67	D7	P09 AN19 TRACED0 TIOA3_2 SOT1_0 (SDA1_0) MCSX5_0 IC23_1	M	N
98	83	-	C7	P08 AN20 TRACED1 TIOB3_2 SCK1_0 (SCL1_0) MCSX4_0 IC22_1	F	N
99	84	-	B7	P07 AN21 TRACED2 TIOA0_2 SCK7_0 (SCL7_0) MCLKOUT_0 IC21_1	M	N
100	85	-	A7	P06 AN22 TRACED3 TIOB0_2 SOT7_0 (SDA7_0) MCSX3_0 IC20_1	F	N
101	86	-	D6	P05 AN23 ADTG_0 TRACECLK SIN7_0 INT01_1 MCSX2_0 FRCK2_1	F	O
102	87	68	B6	P04 TDO SWO	E	G
103	88	69	C6	P03 TMS SWDIO	E	G

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
104	89	70	C5	P02 TDI MCSX6_0	E	H
105	90	71	B5	P01 TCK SWCLK	E	G
106	91	72	A5	P00 TRSTX MCSX7_0	E	H
107	92	-	A6	VSS	-	-
108	-	-	E6	P68 TIOB7_2 SCK3_0 (SCL3_0) INT00_2	E	K
109	-	-	E5	P67 TIOA7_2 SOT3_0 (SDA3_0)	E	I
110	-	-	D5	P66 ADTG_8 SIN3_0 INT11_2	E	K
111	-	-	D4	P65 TIOB7_0 SCK5_1 (SCL5_1)	E	I
112	-	-	C4	P64 TIOA7_0 SOT5_1 (SDA5_1) INT10_2	E	K
113	93 - 93	73 - 73	B4	P63 CROUT_1 SIN5_1 INT03_0 MWEX_0 IC23_0	E	K
114	94	74	C3	P62 ADTG_3 SIN5_0 INT04_1 MOEX_0 IC22_0	I	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
115	95	75	B3	P61 TIOB2_2 SOT5_0 (SDA5_0) RTCCO_0 SUBOUT_0 ZIN2_1	E	I
116	96	76	B2	P60 TIOA2_2 SCK5_0 (SCL5_0) NMIX WKUP0 MRDY_0 FRCK2_0	I	F
117	97	77	A4	VCC	-	-
118	98	78	A3	P80 BIN2_1 IC21_0	E *1	I
119	99	79	A2	P81 AIN2_1 IC20_0	E *1	I
120	100	80	A1	VSS	-	-
-	-	-	K10	VSS	-	-

*1 without pullup control register

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
ADC	ADTG_0	A/D converter external trigger input pin	101	86	-	D6
	ADTG_1		7	7	7	E2
	ADTG_2		23	18	13	H1
	ADTG_3		114	94	74	C3
	ADTG_4		81	-	-	F7
	ADTG_5		80	70	-	D9
	ADTG_6		17	12	12	F2
	ADTG_7		35	30	-	H5
	ADTG_8		110	-	-	D5
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	41	J10
	AN01		63	53	42	H10
	AN02		64	54	43	H9
	AN03		65	55	44	G10
	AN04		66	56	45	G9
	AN05		67	57	46	G8
	AN06		68	58	47	F10
	AN07		69	59	48	F9
	AN08		74	64	53	F8
	AN09		75	65	54	E11
	AN10		76	66	55	E10
	AN11		77	67	56	E9
	AN12		78	68	-	E8
	AN13		79	69	-	D10
	AN14		80	70	-	D9
	AN15		86	71	57	D11
	AN16		87	72	58	C10
	AN17		88	73	59	C11
	AN18		89	74	-	B11
	AN19		97	82	67	D7
	AN20		98	83	-	C7
	AN21		99	84	-	B7
	AN22		100	85	-	A7
	AN23		101	86	-	D6
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-	L2
	TIOA0_1		24	19	14	H2
	TIOA0_2		99	84	-	B7
	TIOB0_0	Base timer ch.0 TIOB pin	37	32	22	J4
	TIOB0_1		14	9	9	E1
	TIOB0_2		100	85	-	A7

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-	J3
	TIOA1_1		25	20	15	H3
	TIOA1_2		5	5	5	D2
	TIOB1_0	Base timer ch.1 TIOB pin	47	42	32	J6
	TIOB1_1		15	10	10	F4
	TIOB1_2		6	6	6	D3
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-	J5
	TIOA2_1		26	21	16	H4
	TIOA2_2		116	96	76	B2
	TIOB2_0	Base timer ch.2 TIOB pin	48	43	33	J7
	TIOB2_1		16	11	11	F3
	TIOB2_2		115	95	75	B3
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-	H5
	TIOA3_1		27	22	17	J1
	TIOA3_2		97	82	67	D7
	TIOB3_0	Base timer ch.3 TIOB pin	49	44	34	J8
	TIOB3_1		17	12	12	F2
	TIOB3_2		98	83	-	C7
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21	K3
	TIOA4_1		28	23	18	J2
	TIOA4_2		51	-	-	H6
	TIOB4_0	Base timer ch.4 TIOB pin	50	45	35	K8
	TIOB4_1		18	13	-	F1
	TIOB4_2		52	-	-	H7
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	84	-	-	C9
	TIOA5_1		29	24	19	K2
	TIOA5_2		93	78	63	A9
	TIOB5_0	Base timer ch.5 TIOB pin	83	-	-	D8
	TIOB5_1		19	14	-	G1
	TIOB5_2		92	77	62	B9
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	G7
	TIOA6_1		94	79	64	C8
	TIOA6_2		82	-	-	E7
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	H8
	TIOB6_1		95	80	65	B8
	TIOB6_2		81	-	-	F7
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	C4
	TIOA7_1		86	71	57	D11
	TIOA7_2		109	-	-	E5
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	D4
	TIOB7_1		87	72	58	C10
	TIOB7_2		108	-	-	E6

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Debugger	SWCLK	Serial wire debug interface clock input pin	105	90	71	B5
	SWDIO	Serial wire debug interface data input / output pin	103	88	69	C6
	SWO	Serial wire viewer output pin	102	87	68	B6
	TCK	JTAG test clock input pin	105	90	71	B5
	TDI	JTAG test data input pin	104	89	70	C5
	TDO	JTAG debug data output pin	102	87	68	B6
	TMS	JTAG test mode state input/output pin	103	88	69	C6
	TRACECLK	Trace CLK output pin of ETM	101	86	-	D6
	TRACED0	Trace data output pin of ETM	97	82	-	D7
	TRACED1		98	83	-	C7
	TRACED2		99	84	-	B7
	TRACED3		100	85	-	A7
	TRSTX	JTAG test reset Input pin	106	91	72	A5
External Bus	MAD00_0	External bus interface address bus	27	22	17	J1
	MAD01_0		28	23	18	J2
	MAD02_0		29	24	19	K2
	MAD03_0		47	42	32	J6
	MAD04_0		48	43	33	J7
	MAD05_0		49	44	34	J8
	MAD06_0		50	45	35	K8
	MAD07_0		62	52	41	J10
	MAD08_0		63	53	42	H10
	MAD09_0		64	54	43	H9
	MAD10_0		65	55	44	G10
	MAD11_0		66	56	45	G9
	MAD12_0		67	57	46	G8
	MAD13_0		68	58	47	F10
	MAD14_0		69	59	48	F9
	MAD15_0		74	64	53	F8
	MAD16_0		75	65	54	E11
	MAD17_0		76	66	55	E10
	MAD18_0		77	67	56	E9
	MAD19_0		78	68	-	E8
	MAD20_0		79	69	-	D10
	MAD21_0		80	70	-	D9
	MAD22_0		86	71	-	D11
	MAD23_0		88	73	-	C11
	MAD24_0		89	74	-	B11

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Bus	MCSX0_0	External bus interface chip select output pin	95	80	65	B8
	MCSX1_0		96	81	66	A8
	MCSX2_0		101	86	-	D6
	MCSX3_0		100	85	-	A7
	MCSX4_0		98	83	-	C7
	MCSX5_0		97	82	67	D7
	MCSX6_0		104	89	70	C5
	MCSX7_0		106	91	72	A5
	MCSX8_0		35	30	-	H5
	MADATA00_0	External bus interface data bus (Address / data multiplex bus)	2	2	2	C1
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	D1
	MADATA03_0		5	5	5	D2
	MADATA04_0		6	6	6	D3
	MADATA05_0		7	7	7	E2
	MADATA06_0		8	8	8	E3
	MADATA07_0		9	9	9	E4
	MADATA08_0		10	10	10	F5
	MADATA09_0		11	11	11	F6
	MADATA10_0		12	12	12	G5
	MADATA11_0		13	13	-	G6
	MADATA12_0		14	14	-	E1
	MADATA13_0		15	15	-	F4
	MADATA14_0		16	16	-	F3
	MADATA15_0		17	17	-	F2
	MDQM0_0	External bus interface byte mask signal output pin	93	78	63	A9
	MDQM1_0		92	77	62	B9
	MALE_0	External bus interface Address Latch enable output signal for multiplex	94	79	64	C8
	MRDY_0	External bus interface external RDY input signal	116	96	76	B2
	MCLKOUT_0	External bus interface external clock output pin	99	84	-	B7
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	18	-	-	F1
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	19	-	-	G1
	MNREX_0	External bus interface read enable signal to control NAND Flash	21	-	-	G3
	MNWEX_0	External bus interface write enable signal to control NAND Flash	20	-	-	G2
	MOEX_0	External bus interface read enable signal for SRAM	114	94	74	C3
	MWEX_0	External bus interface write enable signal for SRAM	113	93	73	B4

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Bus	MSDCLK_0	SDRAM interface SDRAM clock output pin	23	18	-	H1
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	24	19	-	H2
	MRASX_0	SDRAM interface SDRAM row address strobe pin	25	20	-	H3
	MCASX_0	SDRAM interface SDRAM column address strobe pin	26	21	-	H4
	MSDWEX_0	SDRAM interface SDRAM write enable pin	34	29	-	J5
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	C1
	INT00_1		95	80	65	B8
	INT00_2		108	-	-	E6
	INT01_0	External interrupt request 01 input pin	3	3	3	C2
	INT01_1		101	86	-	D6
	INT01_2		85	-	-	B10
	INT02_0	External interrupt request 02 input pin	6	6	6	D3
	INT02_1		62	52	41	J10
	INT02_2		82	-	-	E7
	INT03_0	External interrupt request 03 input pin	113	93	73	B4
	INT03_1		65	55	44	G10
	INT03_2		54	-	-	H8
	INT04_0	External interrupt request 04 input pin	17	12	12	F2
	INT04_1		114	94	74	C3
	INT04_2		10	-	-	F5
	INT05_0	External interrupt request 05 input pin	89	74	-	B11
	INT05_1		75	65	54	E11
	INT05_2		21	16	-	G3
	INT06_1	External interrupt request 06 input pin	88	73	59	C11
	INT06_2		22	17	-	G4
	INT07_1	External interrupt request 07 input pin	11	-	-	F6
	INT07_2		7	7	7	E2
	INT08_1	External interrupt request 08 input pin	19	14	-	G1
	INT08_2		8	8	8	E3
	INT09_1	External interrupt request 09 input pin	20	15	-	G2
	INT09_2		15	10	10	F4
	INT10_1	External interrupt request 10 input pin	16	11	11	F3
	INT10_2		112	-	-	C4
	INT11_1	External interrupt request 11 input pin	50	45	35	K8
	INT11_2		110	-	-	D5
	INT12_1	External interrupt request 12 input pin	32	27	-	L2
	INT12_2		96	81	66	A8
	INT13_1	External interrupt request 13 input pin	33	28	-	J3
	INT13_2		49	44	34	J8
	INT14_1	External interrupt request 14 input pin	68	58	47	F10
	INT14_2		53	-	-	G7
	INT15_1	External interrupt request 15 input pin	52	-	-	H7
	INT15_2		14	9	9	E1

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Interrupt	NMIX	Non-Maskable Interrupt input pin	116	96	76	B2
GPIO	P00	General-purpose I/O port 0	106	91	72	A5
	P01		105	90	71	B5
	P02		104	89	70	C5
	P03		103	88	69	C6
	P04		102	87	68	B6
	P05		101	86	-	D6
	P06		100	85	-	A7
	P07		99	84	-	B7
	P08		98	83	-	C7
	P09		97	82	67	D7
	P0A		96	81	66	A8
	P0B		95	80	65	B8
	P0C		94	79	64	C8
	P0D		93	78	63	A9
	P0E		92	77	62	B9
	P10	General-purpose I/O port 1	62	52	41	J10
	P11		63	53	42	H10
	P12		64	54	43	H9
	P13		65	55	44	G10
	P14		66	56	45	G9
	P15		67	57	46	G8
	P16		68	58	47	F10
	P17		69	59	48	F9
	P18		74	64	53	F8
	P19		75	65	54	E11
	P1A		76	66	55	E10
	P1B		77	67	56	E9
	P1C		78	68	-	E8
	P1D		79	69	-	D10
	P1E		80	70	-	D9
	P1F		81	-	-	F7
	P20	General-purpose I/O port 2	89	74	-	B11
	P21		88	73	59	C11
	P22		87	72	58	C10
	P23		86	71	57	D11
	P24		85	-	-	B10
	P25		84	-	-	C9
	P26		83	-	-	D8
	P27		82	-	-	E7

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
GPIO	P30	General-purpose I/O port 3	14	9	9	E1
	P31		15	10	10	F4
	P32		16	11	11	F3
	P33		17	12	12	F2
	P34		18	13	-	F1
	P35		19	14	-	G1
	P36		20	15	-	G2
	P37		21	16	-	G3
	P38		22	17	-	G4
	P39		23	18	13	H1
	P3A		24	19	14	H2
	P3B		25	20	15	H3
	P3C		26	21	16	H4
	P3D		27	22	17	J1
	P3E		28	23	18	J2
	P3F		29	24	19	K2
	P40	General-purpose I/O port 4	32	27	-	L2
	P41		33	28	-	J3
	P42		34	29	-	J5
	P43		35	30	-	H5
	P44		36	31	21	K3
	P45		37	32	22	J4
	P46		39	34	24	L4
	P47		40	35	25	K4
	P48		41	36	26	K5
	P49		42	37	27	K6
	P4B		47	42	32	J6
	P4C		48	43	33	J7
	P4D		49	44	34	J8
	P4E		50	45	35	K8
	P50	General-purpose I/O port 5	2	2	2	C1
	P51		3	3	3	C2
	P52		4	4	4	D1
	P53		5	5	5	D2
	P54		6	6	6	D3
	P55		7	7	7	E2
	P56		8	8	8	E3
	P57		9	-	-	E4
	P58		10	-	-	F5
	P59		11	-	-	F6
	P5A		12	-	-	G5
	P5B		13	-	-	G6

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
GPIO	P60	General-purpose I/O port 6	116	96	76	B2
	P61		115	95	75	B3
	P62		114	94	74	C3
	P63		113	93	73	B4
	P64		112	-	-	C4
	P65		111	-	-	D4
	P66		110	-	-	D5
	P67		109	-	-	E5
	P68		108	-	-	E6
	P70	General-purpose I/O port 7	51	-	-	H6
	P71		52	-	-	H7
	P72		53	-	-	G7
	P73		54	-	-	H8
	P74		55	-	-	J9
	P80	General-purpose I/O port 8	118	98	78	A3
	P81		119	99	79	A2
	PE0	General-purpose I/O port E	56	46	36	L8
	PE2		58	48	38	L9
	PE3		59	49	39	L10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	59	C11
	SIN0_1		65	55	44	G10
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I2C (operation mode 4).	87	72	58	C10
	SOT0_1 (SDA0_1)		66	56	45	G9
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I2C (operation mode 4).	86	71	57	D11
	SCK0_1 (SCL0_1)		67	57	46	G8
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	96	81	66	A8
	SIN1_1		62	52	41	J10
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I2C (operation mode 4).	97	82	67	D7
	SOT1_1 (SDA1_1)		63	53	42	H10
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I2C (operation mode 4).	98	83	-	C7
	SCK1_1 (SCL1_1)		64	54	43	H9

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	53	-	-	G7
	SIN2_1		85	-	-	B10
	SIN2_2		68	58	47	F10
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I2C (operation mode 4).	54	-	-	H8
	SOT2_1 (SDA2_1)		84	-	-	C9
	SOT2_2 (SDA2_2)		69	59	48	F9
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I2C (operation mode 4).	55	-	-	J9
	SCK2_1 (SCL2_1)		83	-	-	D8
	SCK2_2 (SCL2_2)		74	64	53	F8
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-	D5
	SIN3_1		15	10	10	F4
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I2C (operation mode 4).	109	-	-	E5
	SOT3_1 (SDA3_1)		16	11	11	F3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I2C (operation mode 4).	108	-	-	E6
	SCK3_1 (SCL3_1)		17	12	12	F2

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	6	6	6	D3
	SIN4_1		75	65	54	E11
	SIN4_2		10	-	-	F5
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I2C (operation mode 4).	5	5	5	D2
	SOT4_1 (SDA4_1)		76	66	55	E10
	SOT4_2 (SDA4_2)		11	-	-	F6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I2C (operation mode 4).	4	4	4	D1
	SCK4_1 (SCL4_1)		77	67	56	E9
	SCK4_2 (SCL4_2)		12	-	-	G5
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	2	2	2	C1
	CTS4_1		78	68	-	E8
	CTS4_2		13	-	-	G6
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	3	3	3	C2
	RTS4_1		79	69	-	D10
	RTS4_2		14	9	9	E1
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	114	94	74	C3
	SIN5_1		113	-	-	B4
	SIN5_2		20	15	-	G2
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I2C (operation mode 4).	115	95	75	B3
	SOT5_1 (SDA5_1)		112	-	-	C4
	SOT5_2 (SDA5_2)		21	16	-	G3
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation modes 2) and as SCL5 when it is used in an I2C (operation mode 4).	116	96	76	B2
	SCK5_1 (SCL5_1)		111	-	-	D4
	SCK5_2 (SCL5_2)		22	17	-	G4

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	7	7	7	E2
	SIN6_1		95	80	65	B8
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I2C (operation mode 4).	8	8	8	E3
	SOT6_1 (SDA6_1)		94	79	64	C8
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I2C (operation mode 4).	9	-	-	E4
	SCK6_1 (SCL6_1)		93	78	63	A9
	SCS6_1	Multi-function serial interface ch.6 serial chip select pin	92	77	62	B9
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	101	86	-	D6
	SIN7_1		50	45	35	K8
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I2C (operation mode 4).	100	85	-	A7
	SOT7_1 (SDA7_1)		49	44	34	J8
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I2C (operation mode 4).	99	84	-	B7
	SCK7_1 (SCL7_1)		48	43	33	J7
	SCS7_1	Multi-function serial interface ch.7 serial chip select pin	47	42	32	J6

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	23	18	13	H1
	DTTI0X_1		79	69	-	D10
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	18	13	-	F1
	FRCK0_1		80	70	-	D9
	FRCK0_2		62	52	41	J10
	IC00_0	16-bit input capture ch.0 input pin of Multi-function timer 0. ICxx describes channel number.	22	17	-	G4
	IC00_1		75	65	54	E11
	IC00_2		63	53	42	H10
	IC01_0		21	16	-	G3
	IC01_1		76	66	55	E10
	IC01_2		64	54	43	H9
	IC02_0		20	15	-	G2
	IC02_1		77	67	56	E9
	IC02_2		65	55	44	G10
	IC03_0		19	14	-	G1
	IC03_1		78	68	-	E8
	IC03_2		66	56	45	G9
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	24	19	14	H2
	RTO00_1 (PPG00_1)		86	71	57	D11
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	25	20	15	H3
	RTO01_1 (PPG00_1)		85	-	-	B10
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	26	21	16	H4
	RTO02_1 (PPG02_1)		84	-	-	C9
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	27	22	17	J1
	RTO03_1 (PPG02_1)		83	-	-	D8
	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	28	23	18	J2
	RTO04_1 (PPG04_1)		82	-	-	E7
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	29	24	19	K2
	RTO05_1 (PPG04_1)		81	-	-	F7

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi- function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	8	8	8	E3
	DTTI1X_1		55	-	-	J9
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	96	81	66	A8
	FRCK1_1		50	45	35	K8
	IC10_0	16-bit input capture ch.1 input pin of Multi-function timer 1. ICxx describes channel number.	95	80	65	B8
	IC10_1		54	-	-	H8
	IC11_0		94	79	64	C8
	IC11_1		53	-	-	G7
	IC12_0		93	78	63	A9
	IC12_1		52	-	-	H7
	IC13_0		92	77	62	B9
	IC13_1		51	-	-	H6
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	2	2	2	C1
	RTO10_1 (PPG10_1)		32	27	-	L2
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	3	3	3	C2
	RTO11_1 (PPG10_1)		33	28	-	J3
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	4	4	4	D1
	RTO12_1 (PPG12_1)		34	29	-	J5
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	5	5	5	D2
	RTO13_1 (PPG12_1)		35	30	-	H5
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	6	6	6	D3
	RTO14_1 (PPG14_1)		36	31	21	K3
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	7	7	7	E2
	RTO15_1 (PPG14_1)		37	32	22	J4

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi- function Timer 2	DTTI2X_0	Input signal controlling wave form generator outputs RTO20 to RTO25 of Multi-function timer 2.	74	64	53	F8
	DTTI2X_1		15	10	10	F4
	FRCK2_0	16-bit free-run timer ch.2 external clock input pin	116	96	76	B2
	FRCK2_1		101	86	-	D6
	IC20_0	16-bit input capture ch.2 input pin of Multi-function timer 2. ICxx describes channel number.	119	99	79	A2
	IC20_1		100	85	-	A7
	IC21_0		118	98	78	A3
	IC21_1		99	84	-	B7
	IC22_0		114	94	74	C3
	IC22_1		98	83	-	C7
	IC23_0		113	93	73	B4
	IC23_1		97	82	67	D7
	RTO20_0 (PPG20_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG10 when it is used in PPG2 output modes.	69	59	48	F9
	RTO20_1 (PPG20_1)		9	-	-	E4
	RTO21_0 (PPG20_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	68	58	47	F10
	RTO21_1 (PPG20_1)		10	-	-	F5
	RTO22_0 (PPG22_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	67	57	46	G8
	RTO22_1 (PPG22_1)		11	-	-	F6
	RTO23_0 (PPG22_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	87	72	58	C10
	RTO23_1 (PPG22_1)		12	-	-	G5
	RTO24_0 (PPG24_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	88	73	59	C11
	RTO24_1 (PPG24_1)		13	-	-	G6
	RTO25_0 (PPG24_0)	Wave form generator output pin of Multi-function timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	89	74	-	B11
	RTO25_1 (PPG24_1)		14	9	9	E1
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	24	19	14	H2
	AIN0_1		51	-	-	H6
	AIN0_2		2	2	2	C1
	BIN0_0	QPRC ch.0 BIN input pin	25	20	15	H3
	BIN0_1		52	-	-	H7
	BIN0_2		3	3	3	C2
	ZIN0_0	QPRC ch.0 ZIN input pin	26	21	16	H4
	ZIN0_1		53	-	-	G7
	ZIN0_2		4	4	4	D1

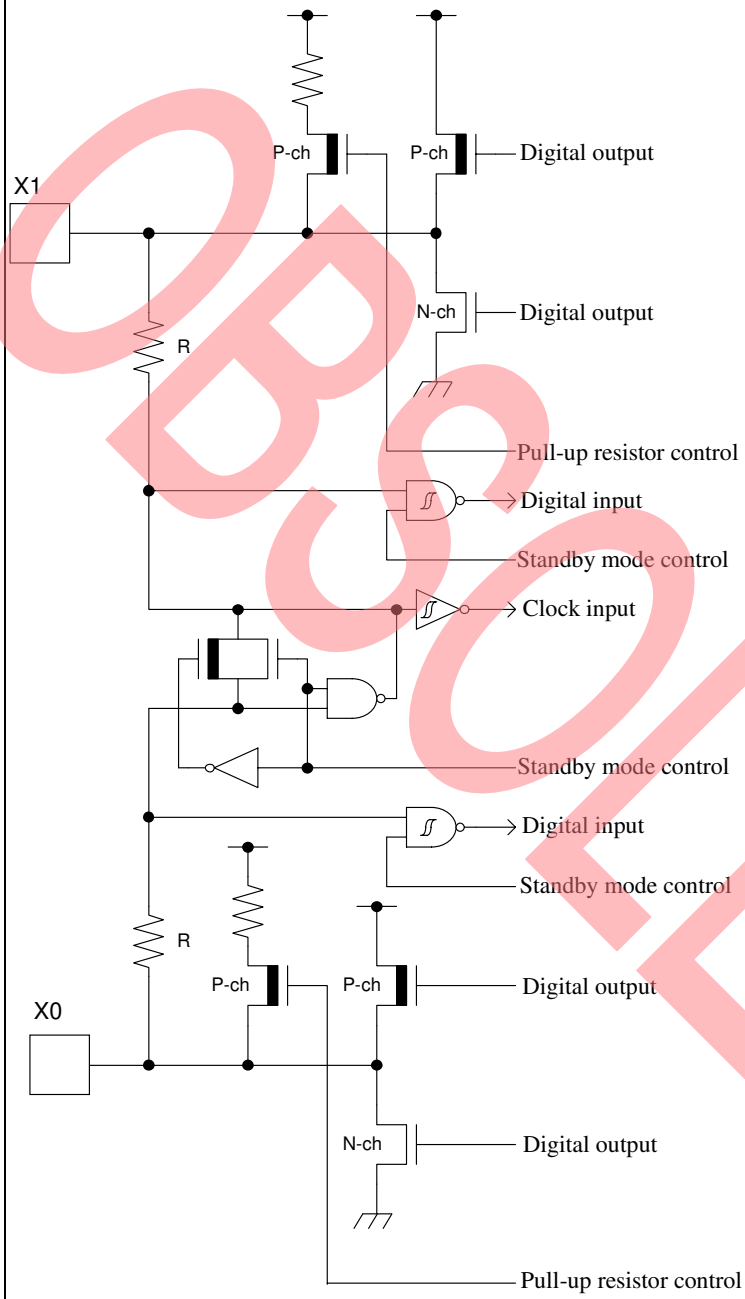
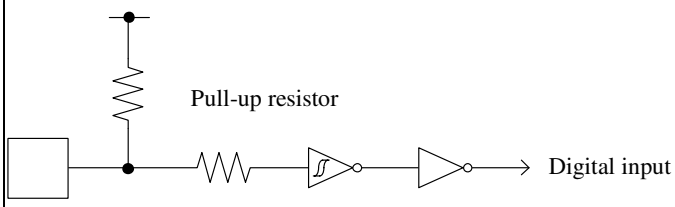
Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	10	-	-	F5
	AIN1_1		89	74	-	B11
	AIN1_2		48	43	33	J7
	BIN1_0	QPRC ch.1 BIN input pin	11	-	-	F6
	BIN1_1		88	73	-	C11
	BIN1_2		49	44	34	J8
	ZIN1_0	QPRC ch.1 ZIN input pin	12	-	-	G5
	ZIN1_1		87	72	-	C10
	ZIN1_2		50	45	35	K8
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	33	28	-	J3
	AIN2_1		119	99	79	A2
	AIN2_2		69	59	48	F9
	BIN2_0	QPRC ch.2 BIN input pin	34	29	-	J5
	BIN2_1		118	98	78	A3
	BIN2_2		68	58	47	F10
	ZIN2_0	QPRC ch.2 ZIN input pin	35	30	-	H5
	ZIN2_1		115	95	75	B3
	ZIN2_2		67	57	46	G8
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	115	95	75	B3
	RTCCO_1		64	54	43	H9
	RTCCO_2		23	18	13	H1
	SUBOUT_0	Sub clock output pin	115	95	75	B3
	SUBOUT_1		64	54	43	H9
	SUBOUT_2		23	18	13	H1
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	116	96	76	B2
	WKUP1	Deep standby mode return signal input pin 1	14	9	9	E1
	WKUP2	Deep standby mode return signal input pin 2	50	45	35	K8
	WKUP3	Deep standby mode return signal input pin 3	69	59	48	F9
DAC	DA0	D/A converter ch.0 analog output pin	36	31	21	K3
	DA1	D/A converter ch.1 analog output pin	37	32	22	J4
VBAT	VREGCTL	On-board regulator control pin	41	36	26	K5
	VWAKEUP	The return signal input pin from a hibernation state	42	37	27	K6

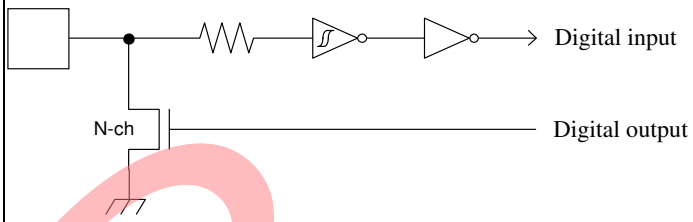
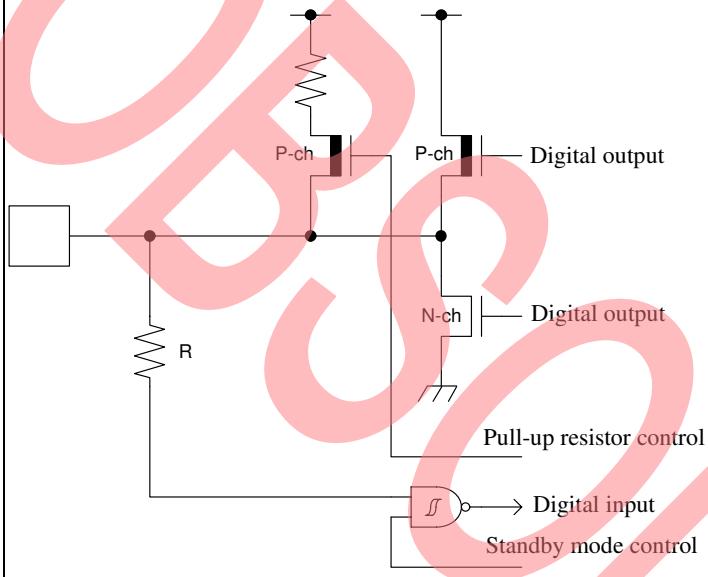
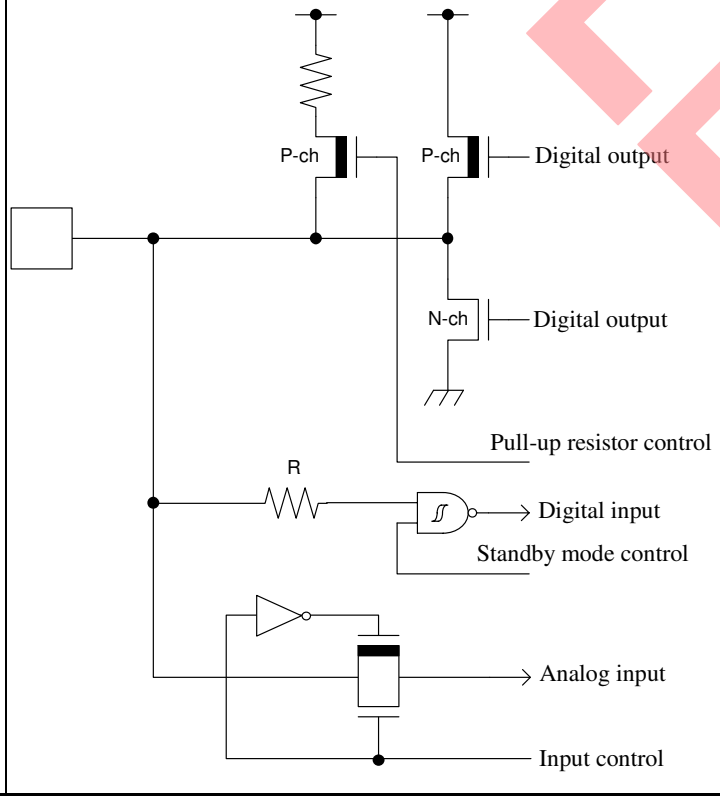
Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Reset	INITX	External Reset Input pin. A reset is valid when INITX=L.	38	33	23	L3
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1=L must be input.	56	46	36	L8
	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to Flash memory, MD0=H must be input.	57	47	37	K9
Power	VCC	Power supply Pin	1	1	1	B1
			31	26	-	K1
			46	41	31	K7
			61	51	-	K11
			91	76	61	A10
			117	97	77	A4
GND	VSS	GND Pin	107	92	-	A6
			30	25	20	L1
			45	40	30	L7
			60	50	40	L11
			90	75	60	A11
			120	100	80	A1
			-	-	-	K10
Clock	X0	Main clock (oscillation) input pin	58	48	38	L9
	X1	Main clock (oscillation) I/O pin	59	49	39	L10
	X0A	Sub clock (oscillation) input pin	39	34	24	L4
	X1A	Sub clock (oscillation) I/O pin	40	35	25	K4
	CROUT_0	Built-in high-speed CR-osc clock output port	87	72	58	C10
	CROUT_1		113	93	73	B4
ADC Power	AVCC	A/D converter and D/A converter analog power supply pin	70	60	49	J11
	AVRL	A/D converter analog reference voltage input pin	72	62	51	G11
	AVRH	A/D converter analog reference voltage input pin	73	63	52	F11
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	43	38	28	L5
ADC GND	AVSS	A/D converter and D/A converter GND pin	71	61	50	H11
C pin	C	Power supply stabilization capacity pin	44	39	29	L6

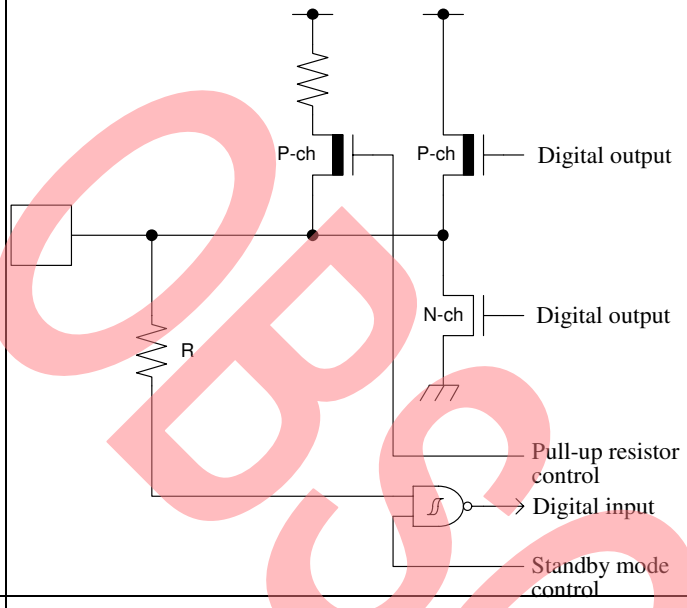
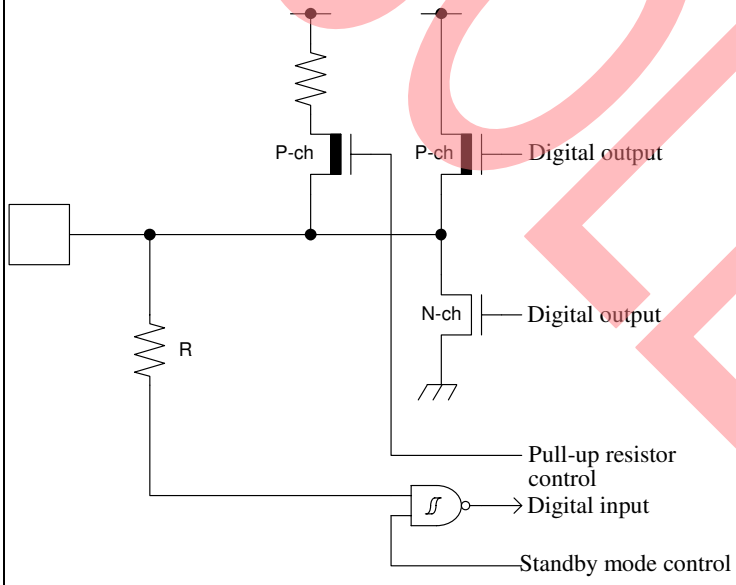
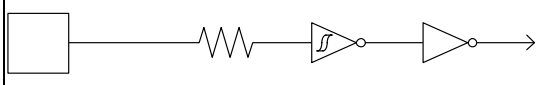
Notes:

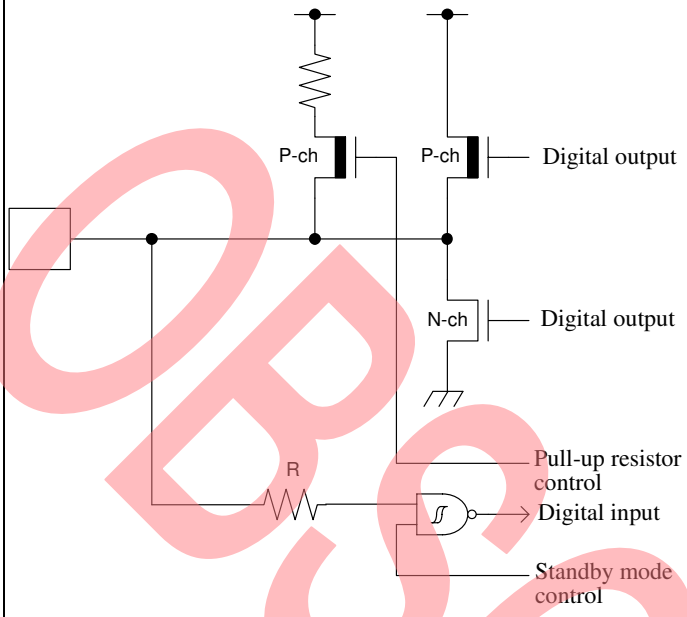
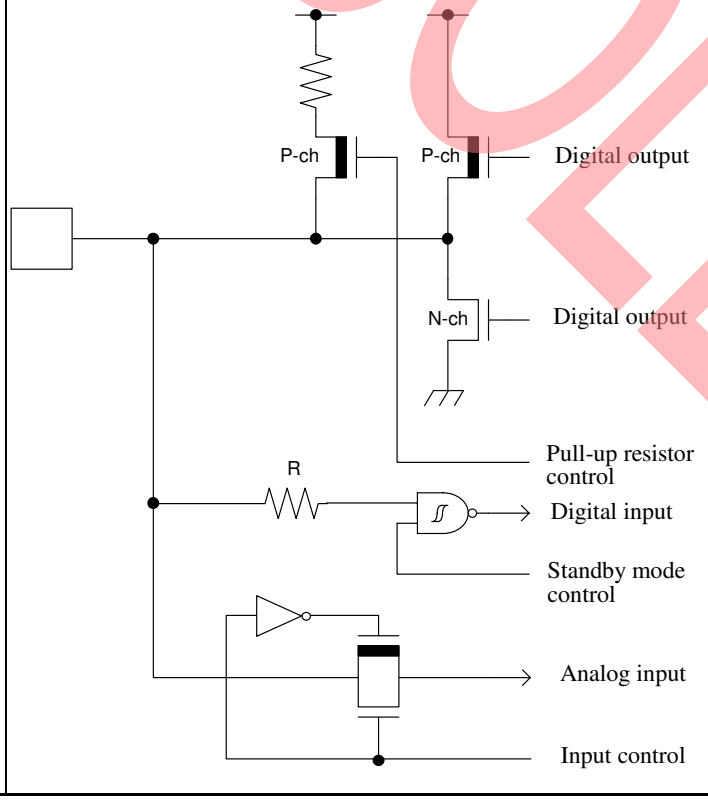
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

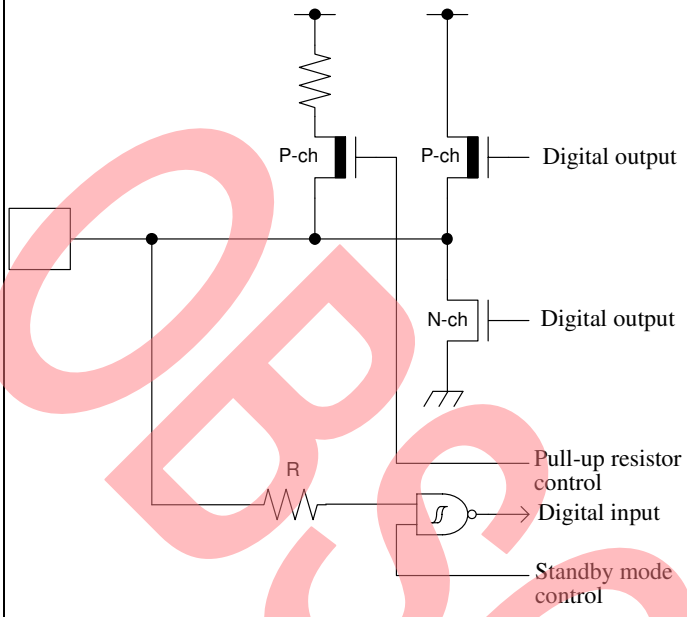
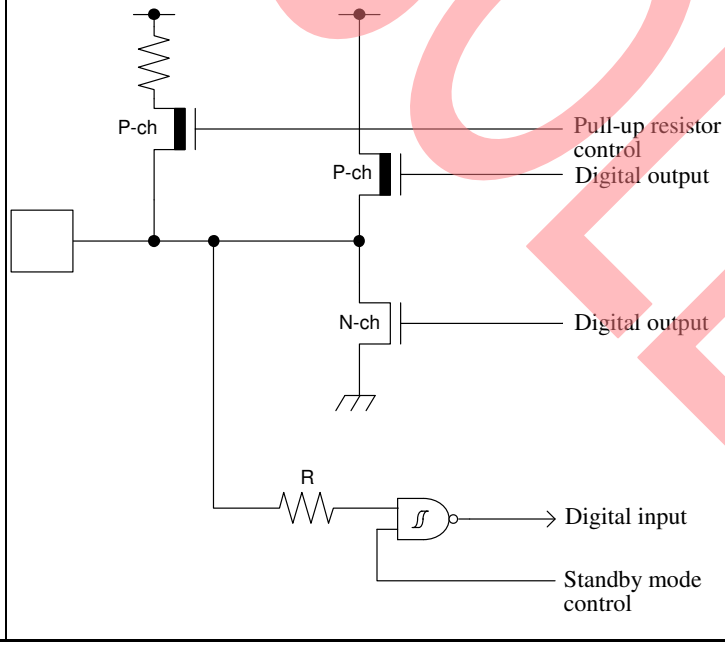
5. I/O Circuit Type

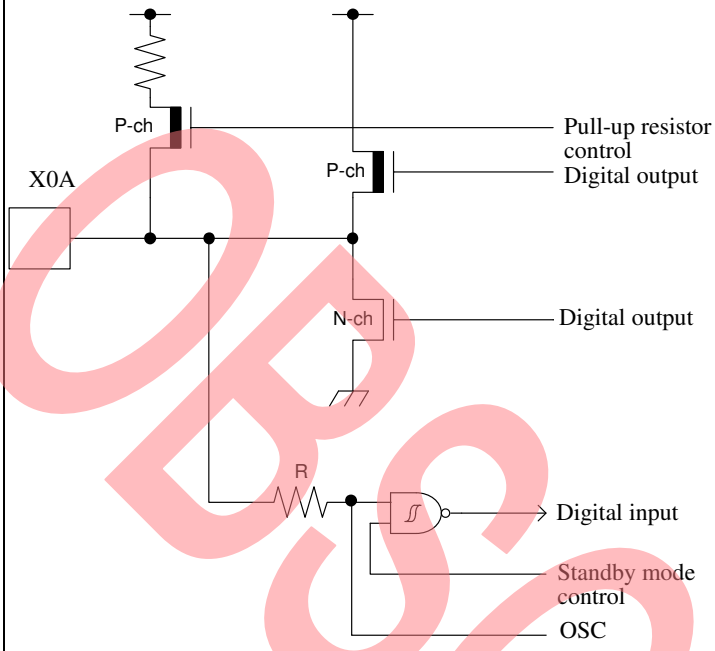
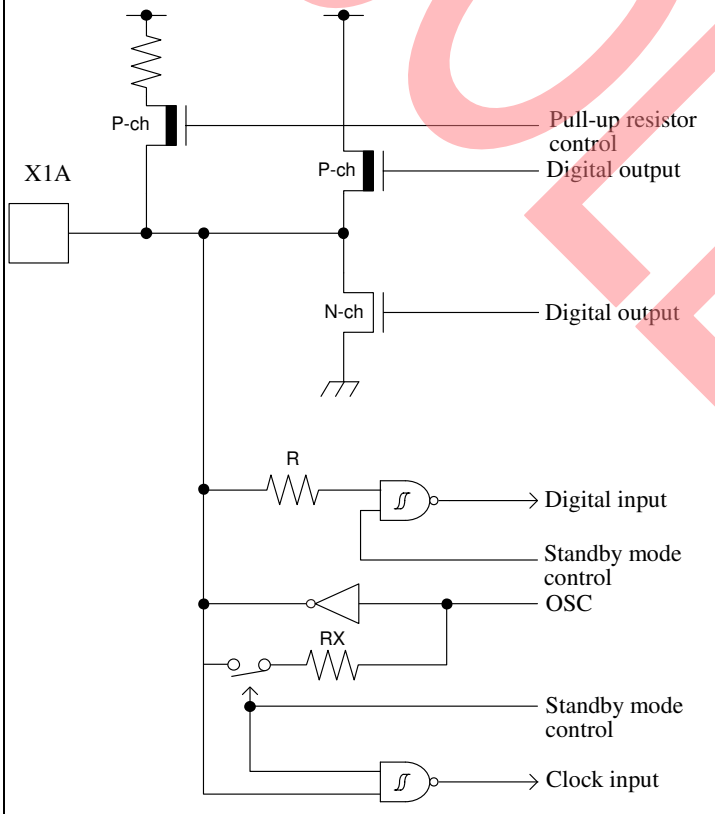
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1 MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

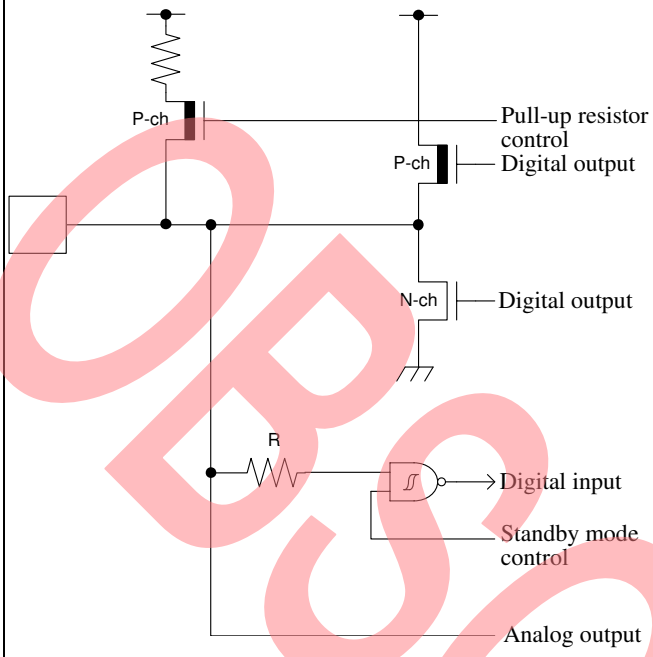
Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
E		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
I		– CMOS level output – CMOS level hysteresis input – 5V tolerant – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – Available to control of PZR registers.
J		CMOS level hysteresis input

Type	Circuit	Remarks
L		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -8 mA, I_{OL} = 8 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
M		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -8 mA, I_{OL} = 8 mA

Type	Circuit	Remarks
N		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) – I_{OL} = 20 mA (Fast Mode Plus) – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
O		– CMOS level output – CMOS level hysteresis input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

Type	Circuit	Remarks
P		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual
Q		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor : Approximately 10 MΩ – With Standby mode control – When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA – For I/O setting, refer to VBAT Domain in the Peripheral Manual

Type	Circuit	Remarks
R		– CMOS level output – CMOS level hysteresis input – Analog output – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -12 mA, I_{OL} = 12 mA (4.5 V to 5.5 V) – I_{OH} = -8 mA, I_{OL} = 8 mA (2.7 V to 4.5 V)

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Code: DS00-00004-3E

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (FBGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

Power Supply Pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

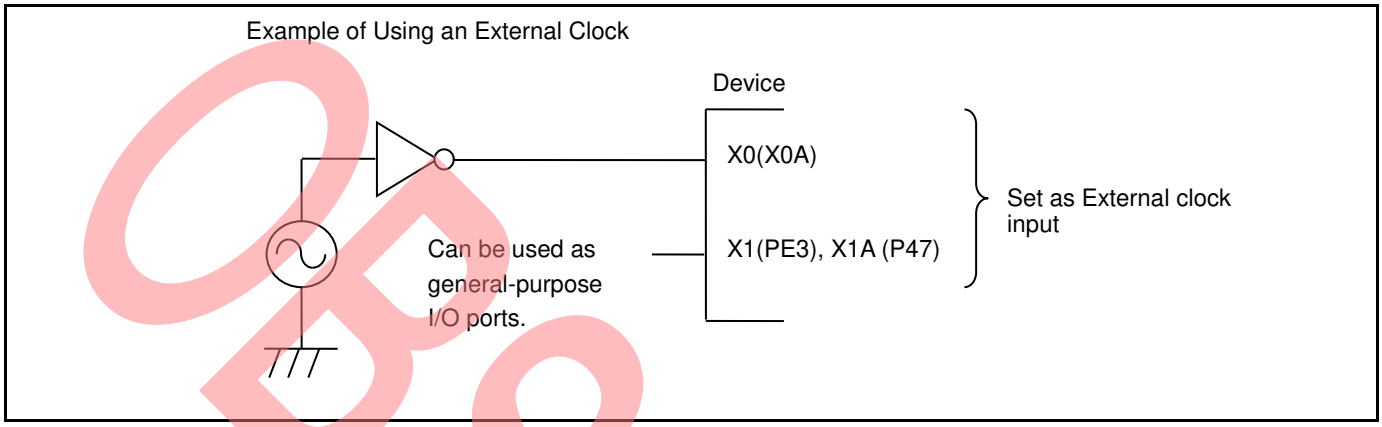
Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm × 1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

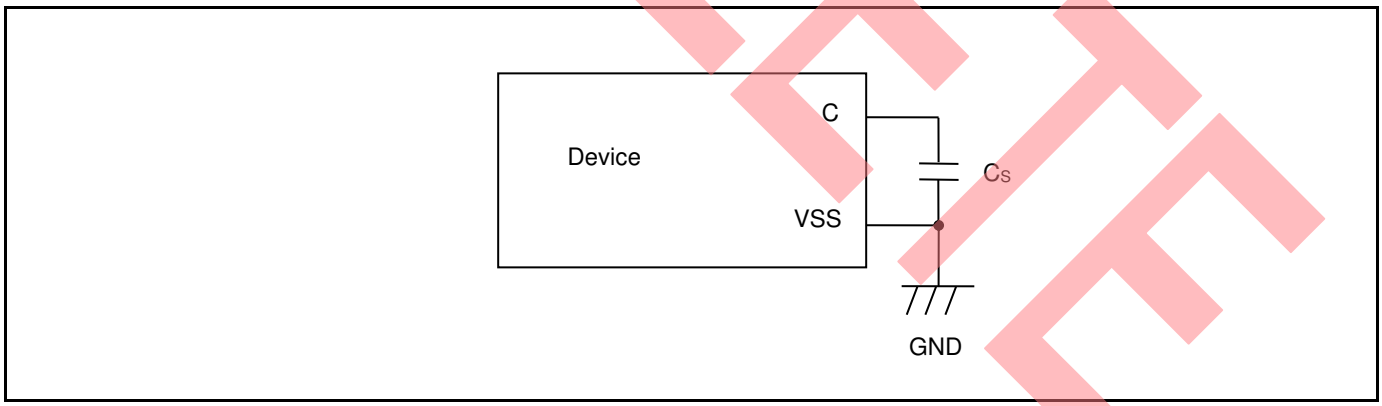


Handling when Using Multi-function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on:	VBAT → VCC
	VCC → AVCC → AVRH
Turning off:	VCC → VBAT
	AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

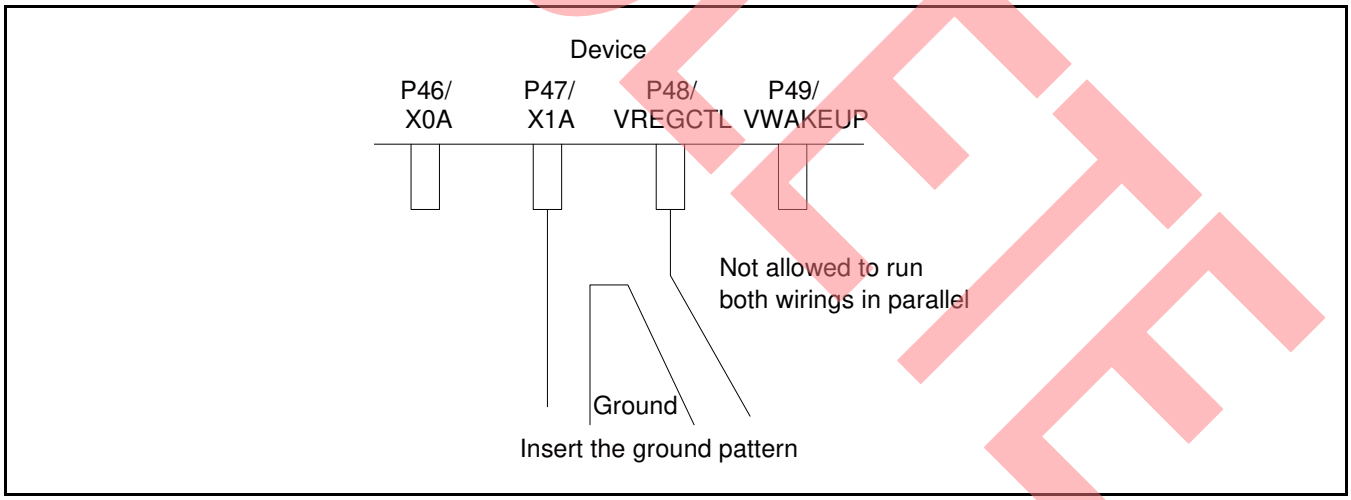
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Adjoining Wiring on Circuit Board

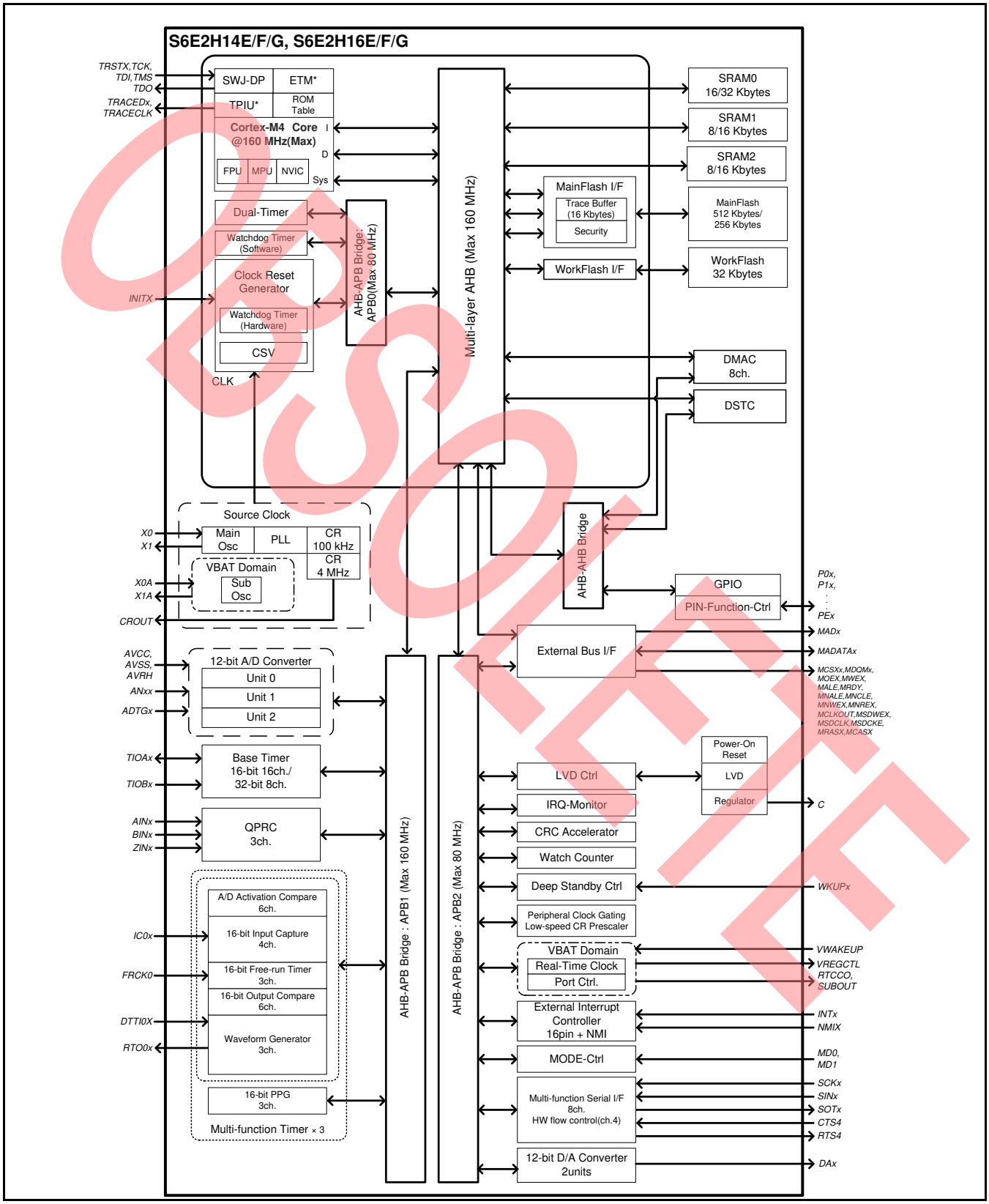
If wiring of the crystal oscillation circuit X1A adjoins and also runs in parallel with the wiring of P48/VREGCTL, there is a possibility that the oscillation erroneously counts because X1A has noise with the change of P48/VREGCTL. Keep as much distance as possible between both wirings and insert the ground pattern between them in order to avoid this possibility.



Handling when Using Debug Pins

When debug pins(TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

8. Block Diagram



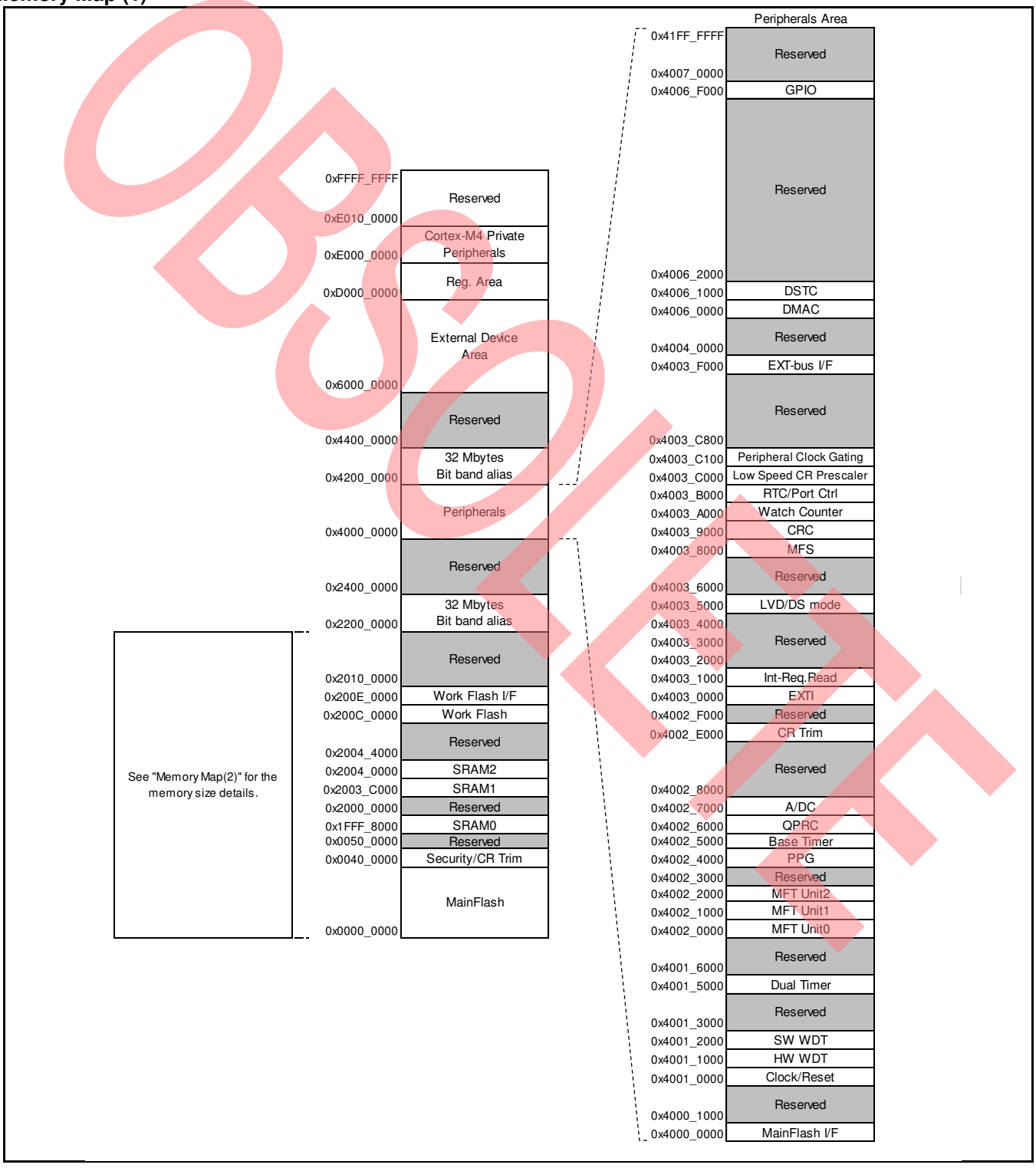
*: For the S6E2H14E0A and S6E2H16E0A, ETM is not available.

9. Memory Size

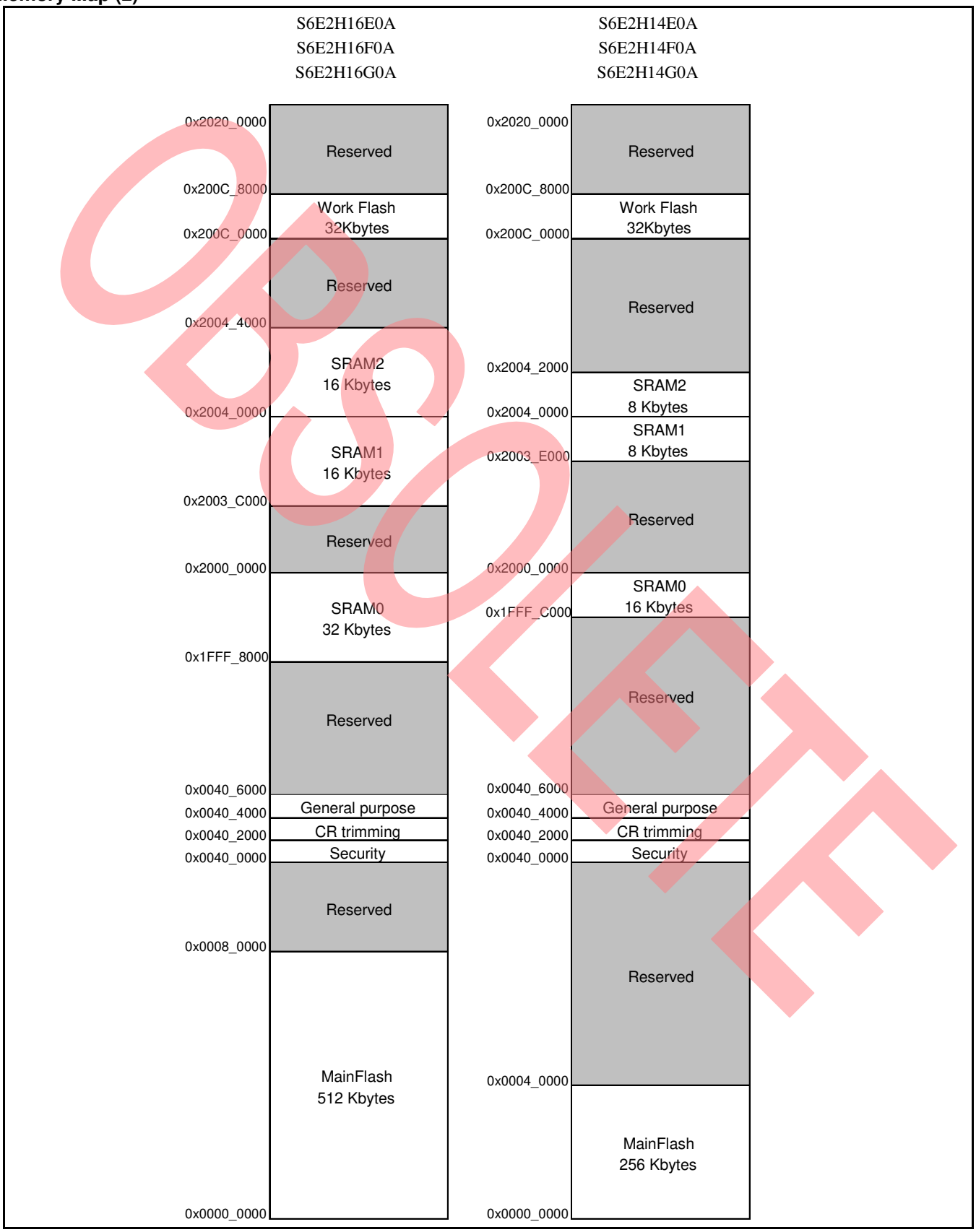
See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_2FFF		Multi-function timer unit2
0x4002_3000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_EFFF		Reserved
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■ INITX=0
This is the period when the INITX pin is the L level.

■ INITX=1
This is the period when the INITX pin is the H level.

■ SPL=0
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

■ SPL=1
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

■ Input enabled
Indicates that the input function can be used.

■ Internal input fixed at 0
This is the status that the input function cannot be used. Internal input is fixed at L.

■ Hi-Z
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■ Setting disabled
Indicates that the setting is disabled.

■ Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■ Analog input is enabled
Indicates that the analog input is enabled.

■ Trace output
Indicates that the trace function can be used.

■ GPIO selected
In Deep standby mode, pins switch to the general-purpose I/O port.

■ Setting prohibition
Prohibition of a setting by specification limitation.

List of Pin Status

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0 / or Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0					
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									Maintain previous state
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*2	*3	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected									
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixedat 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, Stop mode, Deep standby RTC mode, and Deep standby Stop mode.

*2: Maintain previous state at timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	VBAT Power-on reset	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Sode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected / GPIO selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*: When The SOSCNTL bit in the WTOSCCNT Register is 0, Sub crystal oscillator output pin is maintain previous state.
When The SOSCNTL bit in the WTOSCCNT Register is 1, Oscillation is stopped at Stop mode and Deep standby Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1,*3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1,*4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1,*4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *5	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *6	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current *7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *5	I_{OH}	-	- 10	mA	4 mA type
			20	mA	8 mA type
			- 20	mA	12 mA type
H level average output current *6	I_{OHAV}	-	- 4	mA	4 mA type
			8	mA	8 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: V_{BAT} must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*4	5.5	V	
Power supply voltage (VBAT)		V_{BAT}	-	2.7	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC}=V_{CC}
Analog reference voltage		AVRH	-	*3	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *1
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	- 40	*2	°C	

*1: See "●C pin" in "■Handling Devices" for the connection of the smoothing capacitor.

*2: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is shown below.

T_A (Max) = T_J (Max) - Pd(Max) × θja
Pd: Power dissipation (W)
θja: Package thermal resistance (°C/W)

Pd (Max) = V_{CC} × I_{CC} (Max) + Σ (I_{OL}×V_{OL}) + Σ ((V_{CC}-V_{OH}) × (- I_{OH}))
I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*3 :The minimum value of Analog reference voltage depends on the value of compare clock cycle (Tcck). See 12.5 12-bit A/D Converter for the details.

*4: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

Package thermal resistance and maximum permissible power for each package are shown below.

The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			T_A=+85°C	T_A=+105°C
LQH080 (0.5-mm pitch)	Single-layered both sides	82	488	244
	4 layers	56	714	357
LQI100 (0.5-mm pitch)	Single-layered both sides	59	678	339
	4 layers	39	1026	513
LQM120 (0.5-mm pitch)	Single-layered both sides	71	563	282
	4 layers	50	800	400
FDI121 (0.5-mm pitch)	Single-layered both sides	63	635	317
	4 layers	37	1081	540

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
   Any use of semiconductor devices will be under their recommended operating condition.
   Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
   No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator
$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

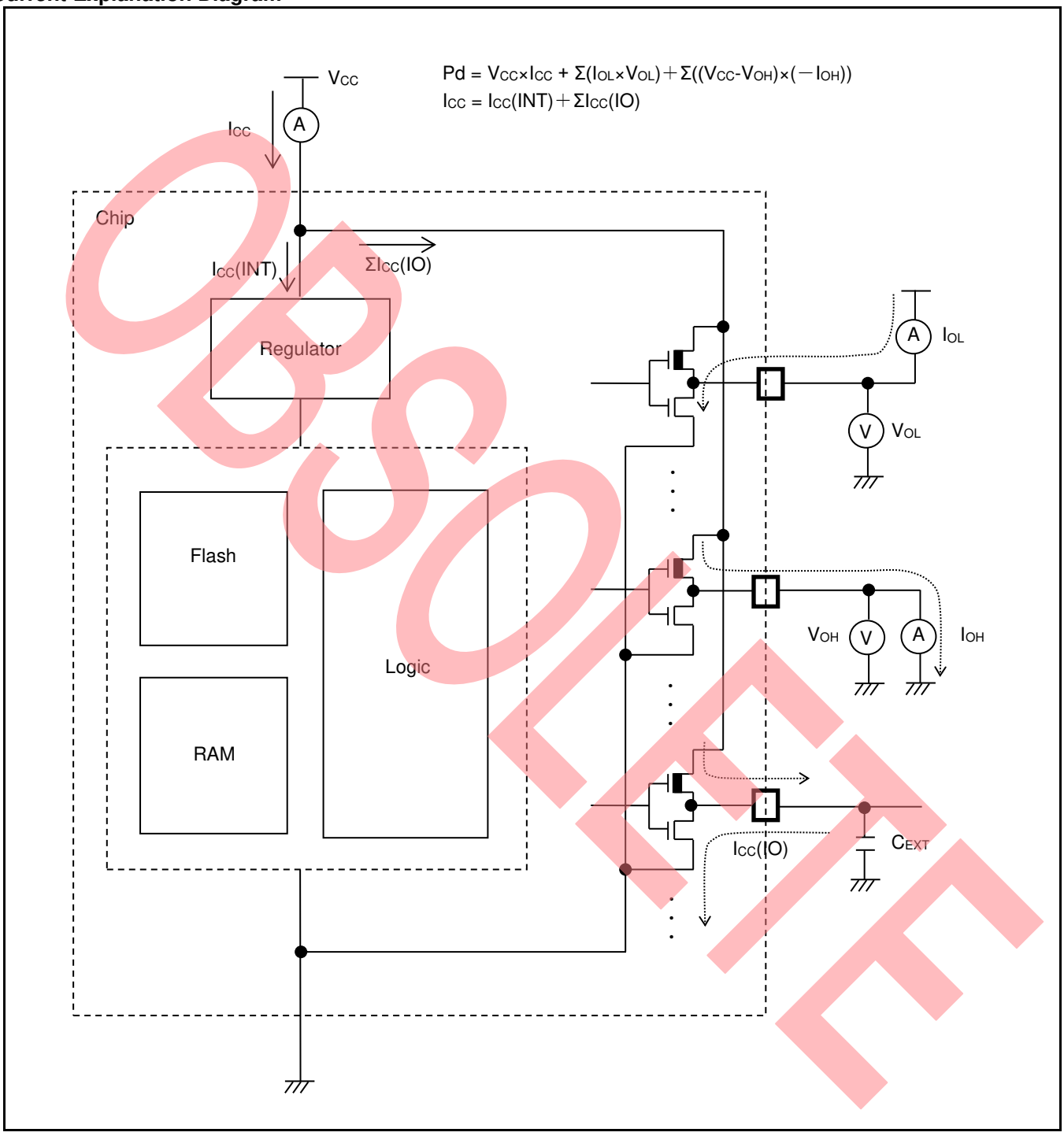
Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	T_J = +125°C	16.8 mA
		T_J = +105°C	8.6 mA
		T_J = +85°C	5.8 mA

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation(PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5, *6 *9	160 MHz	51	71	mA	*3 When all peripheral clocks are ON
					144 MHz	47	67		
					120 MHz	39	59		
					100 MHz	33	53		
					80 MHz	27	47		
					60 MHz	20	40		
					40 MHz	14	34		
					20 MHz	7.6	28		
					8 MHz	3.9	24		
					4 MHz	2.7	23		
					160 MHz	30	51	mA	*3 When all peripheral clocks are OFF
					144 MHz	28	48		
					120 MHz	23	43		
					100 MHz	20	40		
					80 MHz	16	36		
					60 MHz	12	32		
					40 MHz	8.7	29		
					20 MHz	5.0	25		
					8 MHz	2.8	23		
					4 MHz	2.1	22		

Table 12-2 Typical and Maximum Current Consumption in Normal Operation(PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*7	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*8 *9	160 MHz	56	76	mA	*3 When all peripheral clocks are ON
					144 MHz	51	71		
					120 MHz	43	63		
					100 MHz	37	57		
					80 MHz	30	50		
					60 MHz	23	43		
					40 MHz	16	36		
					20 MHz	8.5	29		
					8 MHz	4.3	25		
					4 MHz	2.9	23		
					160 MHz	30	51	mA	*3 When all peripheral clocks are OFF
					144 MHz	28	48		
					120 MHz	24	44		
					100 MHz	20	41		
					80 MHz	17	37		
					60 MHz	13	33		
					40 MHz	9.2	30		
					20 MHz	5.3	26		
					8 MHz	3.0	23		
					4 MHz	2.2	23		

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory
*7: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK
*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)
*9: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-3 Typical and Maximum Current Consumption in Normal Operation(PLL), Code with Data Accessing Running from Flash Memory (Flash 0 wait-cycle Mode and Read Access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5 *6	72 MHz	38	58	mA	*3 When all peripheral clocks are ON
					60 MHz	33	53		
					48 MHz	28	48		
					36 MHz	22	42		
					24 MHz	16	36		
					12 MHz	9.5	30		
					8 MHz	6.9	27		
					4 MHz	4.2	25		
					72 MHz	29	49	mA	*3 When all peripheral clocks are OFF
					60 MHz	26	46		
					48 MHz	22	42		
					36 MHz	18	38		
					24 MHz	13	33		
					12 MHz	7.8	28		
					8 MHz	5.8	26		
					4 MHz	3.7	24		

*1: T_A=+25°C, V_{CC}=3.3 V
*2: T_J=+125°C, V_{CC}=5.5 V
*3: When all ports are fixed.
*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK
*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)
*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-4 Typical and Maximum Current Consumption in Normal Operation(Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 wait-cycle Mode and Read Access 0 wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (main oscillation)	*5*6	4 MHz	4.0	24	mA	*3 When all peripheral clocks are ON
						3.2	24	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in high-speed CR)	*5	4 MHz	3.2	24	mA	*3 When all peripheral clocks are ON
						2.7	23	mA	*3 When all peripheral clocks are OFF
			Normal operation (sub oscillation)	*5	32 kHz	0.34	21	mA	*3 When all peripheral clocks are ON
						0.30	21	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in low-speed CR)	*5	100 kHz	0.36	21	mA	*3 When all peripheral clocks are ON
						0.33	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, VC_C=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *6 (PLL)	160 MHz	35	55	mA	*3 When all peripheral clocks are ON
				144 MHz	32	52		
				120 MHz	27	47		
				100 MHz	23	43		
				80 MHz	18	39		
				60 MHz	14	34		
				40 MHz	9.9	30		
				20 MHz	5.5	26		
				8 MHz	3.1	23		
				4 MHz	2.3	23		
				160 MHz	14	35	mA	*3 When all peripheral clocks are OFF
				144 MHz	13	33		
				120 MHz	11	31		
				100 MHz	9.5	30		
				80 MHz	7.8	28		
				60 MHz	6.3	27		
				40 MHz	4.6	25		
				20 MHz	2.9	23		
				8 MHz	2.2	23		
				4 MHz	2.0	22		

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *6 (PLL)	72 MHz	23	43	mA	*3 When all peripheral clocks are ON
				60 MHz	19	39		
				48 MHz	16	36		
				36 MHz	12	32		
				24 MHz	8.5	29		
				12 MHz	5.1	25		
				8 MHz	3.9	24		
				4 MHz	2.7	23		
				72 MHz	8.8	29	mA	*3 When all peripheral clocks are OFF
				60 MHz	7.6	28		
				48 MHz	6.3	27		
				36 MHz	5.1	25		
				24 MHz	3.9	24		
				12 MHz	2.7	23		
				8 MHz	2.3	23		
				4 MHz	1.9	22		

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation(Other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *5 (main oscillation)	4MHz	2.1	22	mA	*3 When all peripheral clocks are ON
					1.3	22	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in high-speed CR)	4 MHz	1.3	22	mA	*3 When all peripheral clocks are ON
					0.8	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.28	21	mA	*3 When all peripheral clocks are ON
					0.27	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.29	21	mA	*3 When all peripheral clocks are ON
					0.28	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.21	0.94	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode *5 (main oscillation)	4 MHz	1.4	2.1	mA	*3, *4 T_A=+25°C
					-	8.8	mA	*3, *4 T_A=+85°C
					-	11	mA	*3, *4 T_A=+105°C
			Timer mode (built-in high-speed CR)	4 MHz	0.49	1.2	mA	*3, *4 T_A=+25°C
					-	7.9	mA	*3, *4 T_A=+85°C
					-	11	mA	*3, *4 T_A=+105°C
			Timer mode (sub oscillation)	32 kHz	0.23	0.96	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.24	0.97	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (sub oscillation)	32 kHz	0.21	0.94	mA	*3, *4 T_A=+25°C
					-	7.6	mA	*3, *4 T_A=+85°C
					-	10	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When using the crystal oscillator of 4 M Hz (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

*1: V_{CC}=3.3 V

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is OFF)	-	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby Stop mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep standby RTC mode *6 (When RAM is OFF)	32 kHz	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby RTC mode *6 (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop	-	0.015	0.14	µA	*3, *4, *5 T_A=+25°C
					-	4.0	µA	*3, *4, *5 T_A=+85°C
					-	9.4	µA	*3, *4, *5 T_A=+105°C
			RTC operation *6		1.3	2.4	µA	*3, *4 T_A=+25°C
					-	6.2	µA	*3, *4 T_A=+85°C
					-	12	µA	*3, *4 T_A=+105°C

*2: V_{CC}=5.5 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
Main flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	13.4	15.9	mA	
Work flash memory write/erase current	$I_{CCWFLASH}$		At Write/Erase	-	11.5	13.6	mA	*1

1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

Table 12-11 Peripheral Current Dissipation

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			40	80	160		
HCLK	GPIO	All ports	0.16	0.32	0.62	mA	T_A=+25°C, V_{CC}=3.3 V
	DMAC	-	0.68	1.35	2.63		
	DSTC	-	0.93	1.88	3.65		
	External bus I/F	-	0.17	0.34	0.71		
PCLK1	Base timer	4 ch.	0.18	0.37	0.73	mA	T_A=+25°C, V_{CC}=3.3 V
	Multi-functional timer/PPG	1 unit / 4 ch.	0.61	1.22	2.43		
	Quadrature position/Revolution counter	1 unit	0.04	0.07	0.14		
	A/DC	1 unit	0.22	0.44	0.88		
PCLK2	Muli-function serial	1 ch.	0.30	0.60	-	mA	T_A=+25°C, V_{CC}=3.3 V

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 4 mA $V_{CC} < 4.5$ V, I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 8 mA $V_{CC} < 4.5$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 12 mA $V_{CC} < 4.5$ V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OH} = - 4 mA $V_{CC} < 4.5$ V, I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OH} = 4 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OH} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OH} = 3 mA					
			$V_{CC} \leq 5.5$ V, I_{OH} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

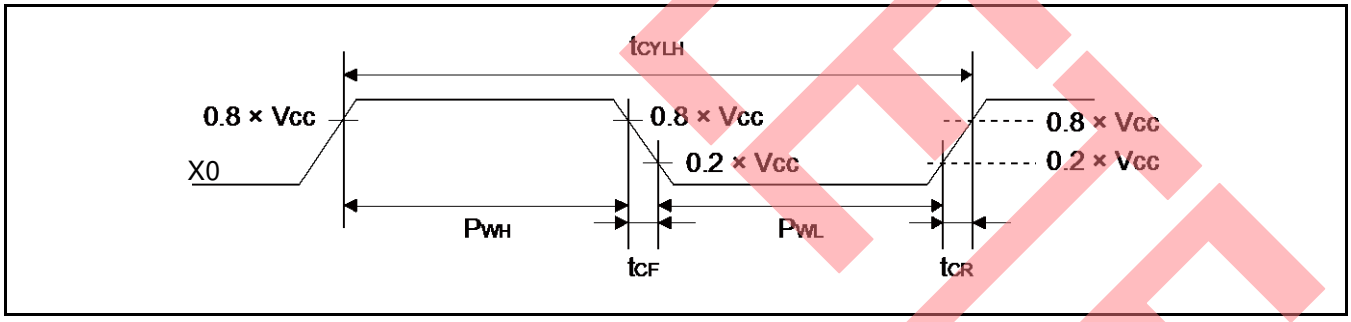
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CC}	-	-	-	160	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	80	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	160	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	80	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	6.25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	12.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	6.25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	12.5	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part(MN709-00001).

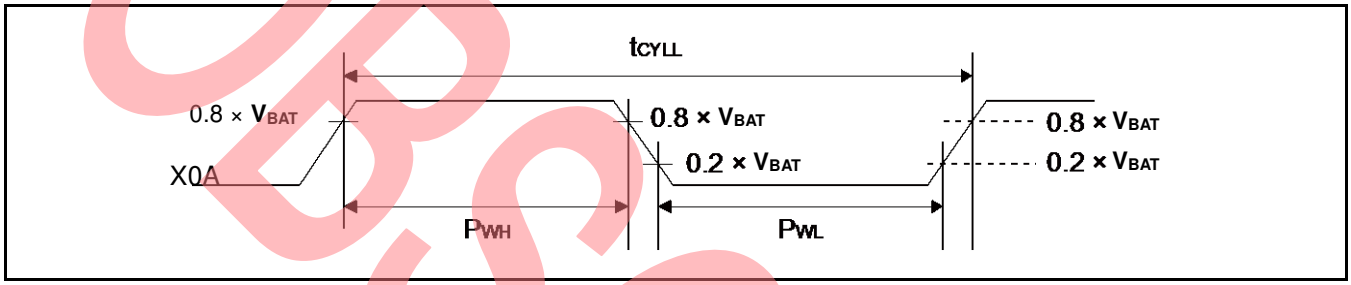
*2: For about each APB bus which each peripheral is connected to, see 8. Block Diagram in this data sheet.



12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = -20°C to + 105°C	3.92	4	4.08	MHz	When trimming*1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
Clock frequency	f_{CRH}	T_J = - 40°C to + 125°C	2.9	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.
This period is able to use high-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	80	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	320	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part(MN709-00001).

12.4.5 Operating Conditions of Main PLL (In the Case of Using Built-in High-speed CR Clock for Input Clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	75	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	320	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part(MN709-00001).

Note:

- *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency and temperature has been trimmed.*

12.4.6 Reset Input Characteristics

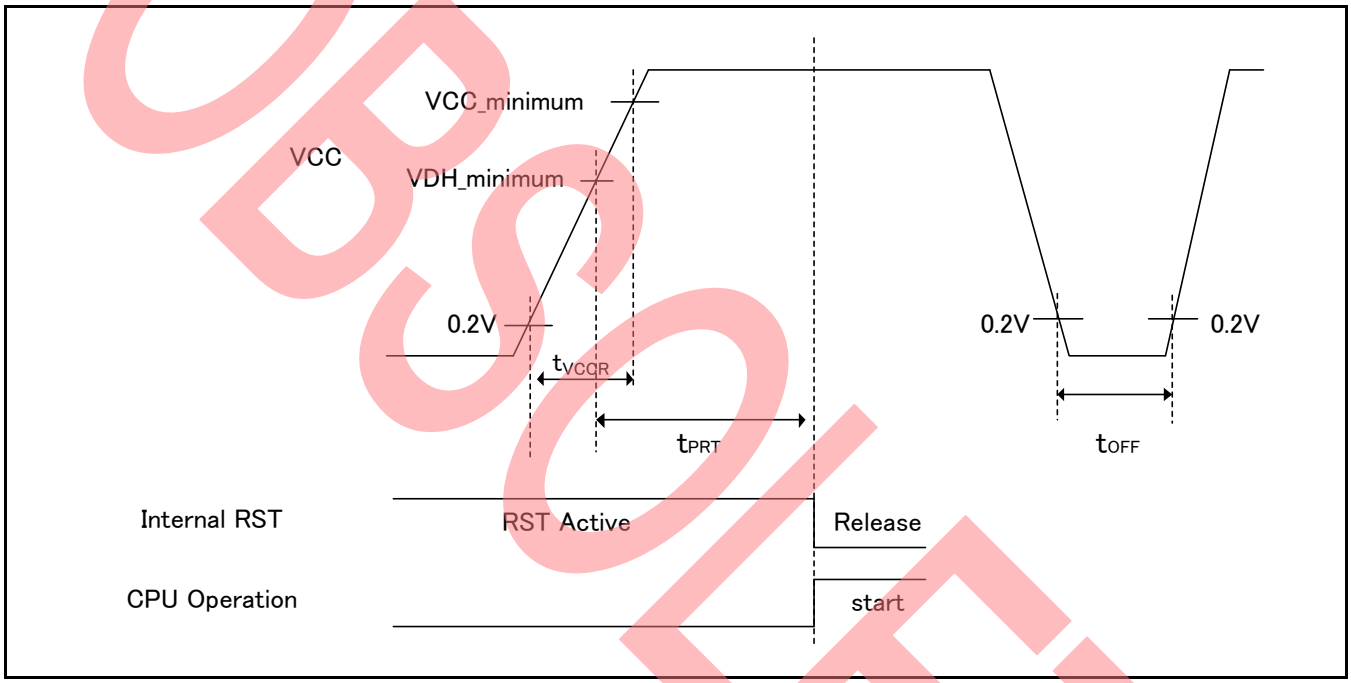
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		0.33	0.60	ms	



Glossary

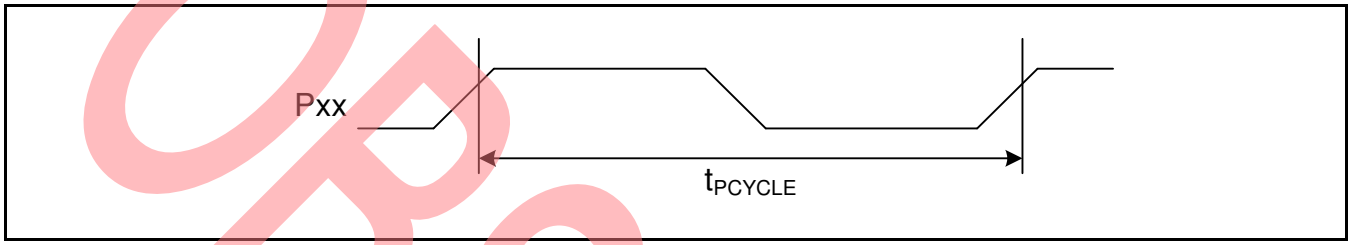
- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum detection voltage of Low-Voltage detection reset. See 8. Low-Voltage Detection Characteristics.

12.4.8 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.



12.4.9 External Bus Timing

External Bus Clock Output Characteristics

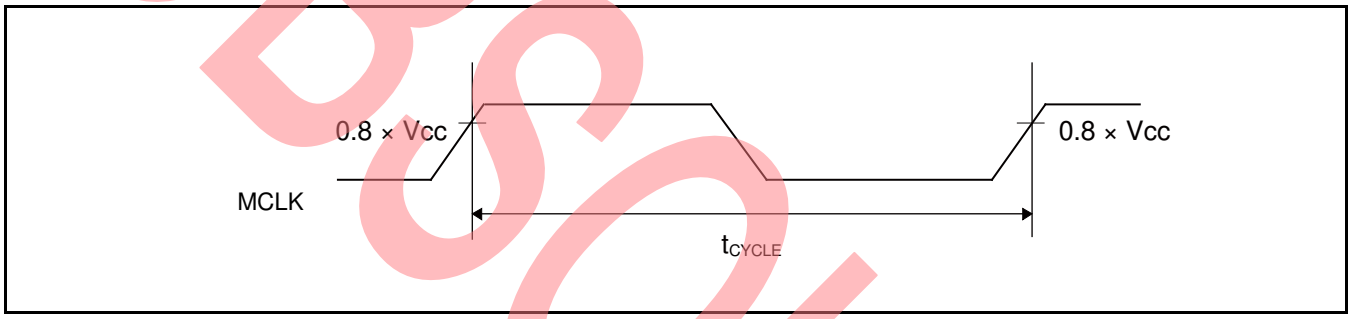
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part(MN709-00001).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

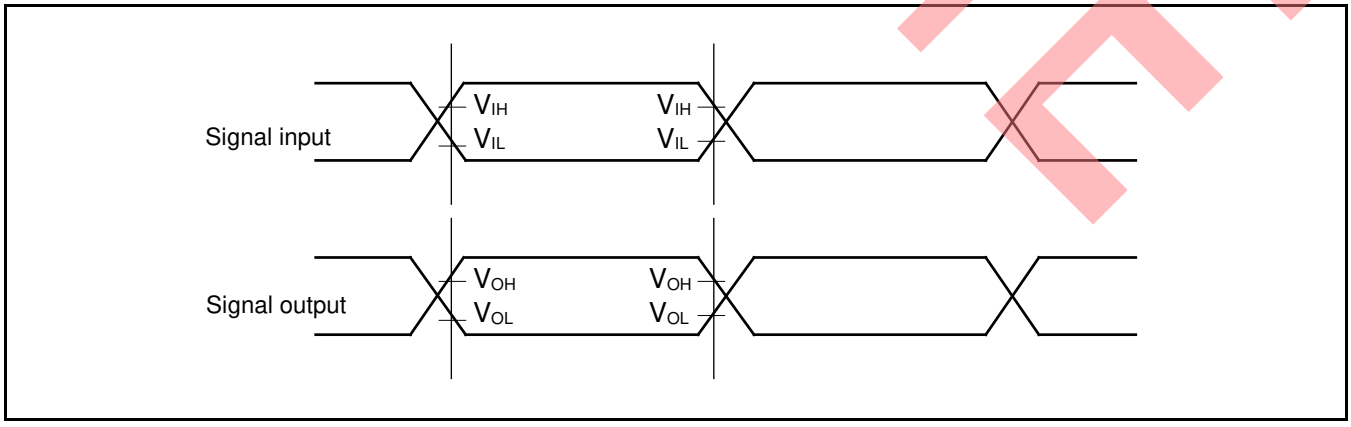
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



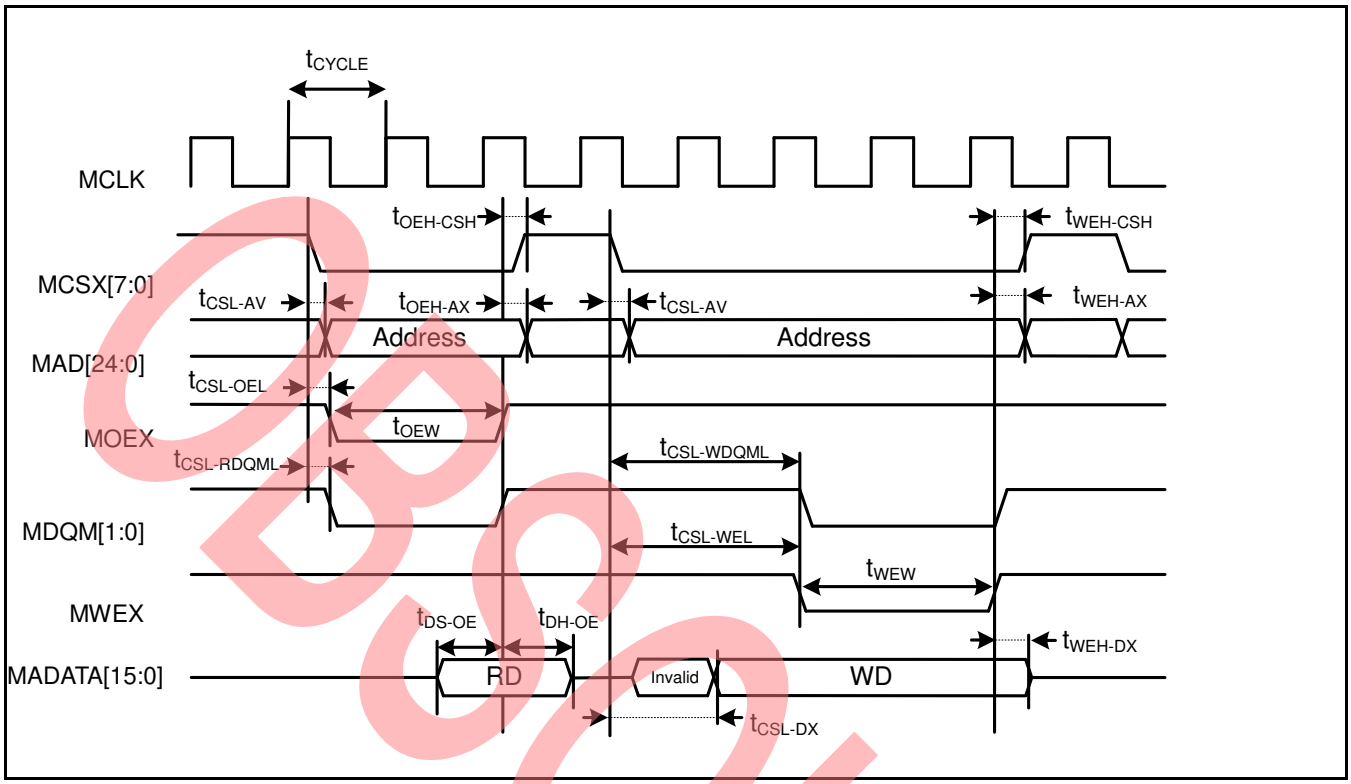
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MOEX Mininum pulse width	t_{OEW}	MOEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MCSX↓→Address output delay time	t_{CSL-AV}	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 4.5$ V	-9	+9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MOEX↑→Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→ MOEX↓ delay time	$t_{CSL-OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MOEX↑→ MCSX↑ time	$t_{OEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
Data set up→MOEX↑ time	t_{DS-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MOEX↑→ Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX Mininum pulse width	t_{WEW}	MWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MWEX↑→Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MWEX↓ delay time	$t_{CSL-WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX↑→MCSX↑ delay time	$t_{WEH-CSH}$		$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MCSX↓→MDQM↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 4.5$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 4.5$ V	MCLK×n-12	MCLK×n+12	
MWEX↓→ Data output time	t_{CSL-DX}	MCSX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 4.5$ V	MCLK-12	MCLK+12	
MWEX↑→ Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*


tCYCLE
MCLK
tOEH-CSH
tWEH-CSH
MCSX[7:0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MAD[24:0]
tCSL-OEL
tOEW
MOEX
tCSL-RDQML
tCSL-WDQML
MDQM[1:0]
tCSL-WEL
tWEW
MWEX
tDS-OE
tDH-OE
tWEH-DX
MADATA[15:0]
RD
Invalid
WD
tCSL-DX

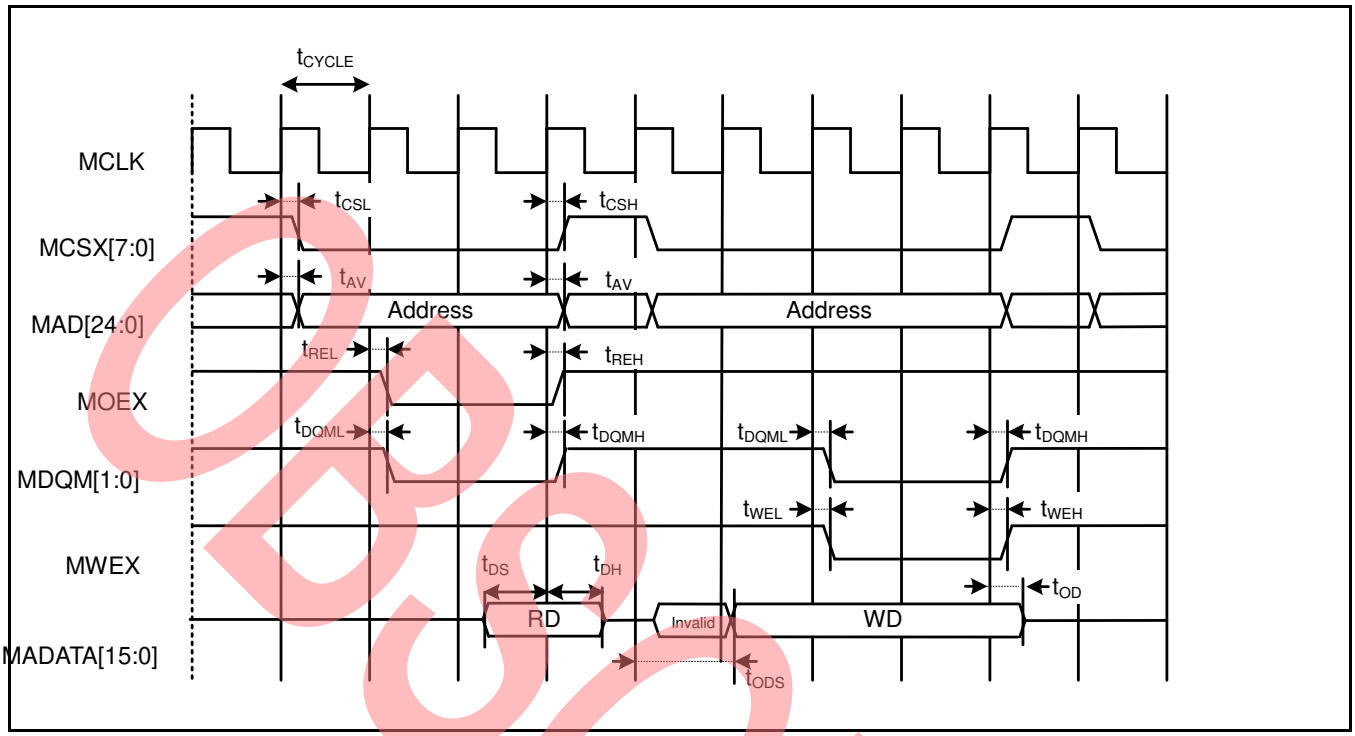
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{CSH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{REH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
Data set up →MCLK↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	19	-	ns
			$V_{CC} < 4.5$ V	37		
MCLK↑→ Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{WEH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
	t_{DQMH}		$V_{CC} \geq 4.5$ V	1	9	ns
			$V_{CC} < 4.5$ V		12	
MCLK↑→ Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 4.5$ V		MCLK+24	
MCLK↑→ Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	18	ns
			$V_{CC} < 4.5$ V		24	

Note:

- *When the external load capacitance C_L = 30 pF*


tCYCLE
MCLK
tCSL
tCSH
MCSX[7:0]
tAV
tAV
Address
Address
MAD[24:0]
tREL
tREH
MOEX
tDQML
tDQMH
tDQML
tDQMH
MDQM[1:0]
tWEL
tWEH
MWEX
tDS
tDH
tOD
RD
Invalid
WD
MADATA[15:0]
tODS

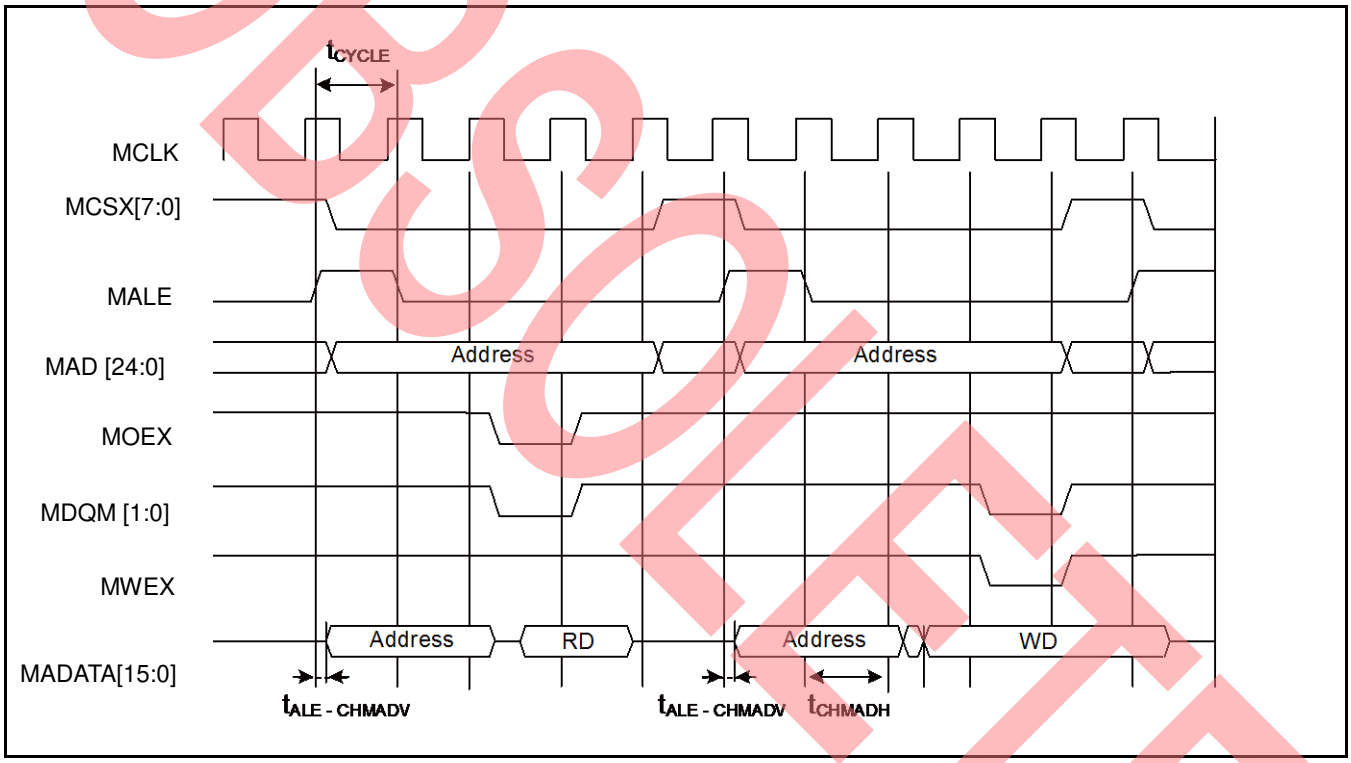
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*



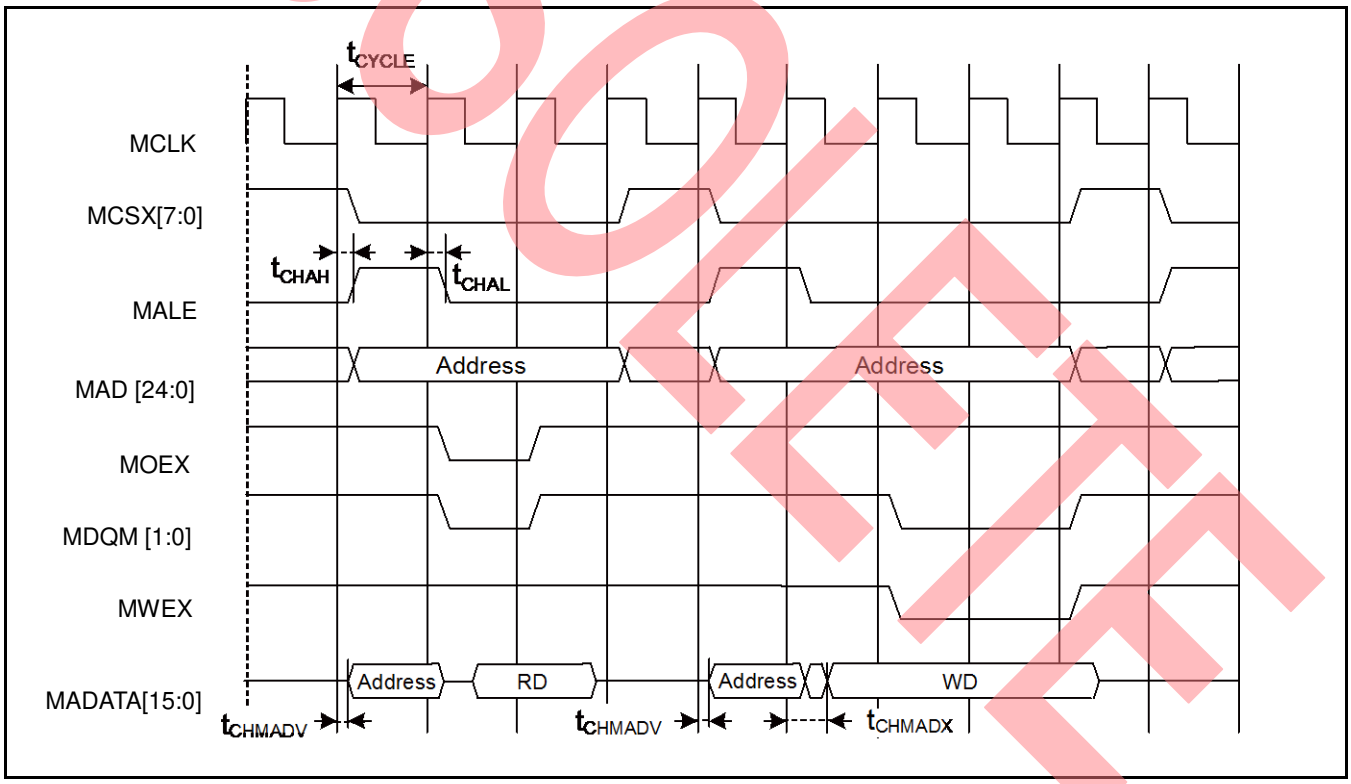
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
	t_{CHAH}		$V_{CC} \geq 4.5$ V	1	9	ns	
			$V_{CC} < 4.5$ V		12	ns	
MCLK↑→ Multiplexed address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				
MCLK↑→ Multiplexed data output time	t_{CHMADX}		$V_{CC} \geq 4.5$ V	1	t_{OD}	ns	
			$V_{CC} < 4.5$ V				

Note:

- *When the external load capacitance C_L = 30 pF*



NAND Flash Mode

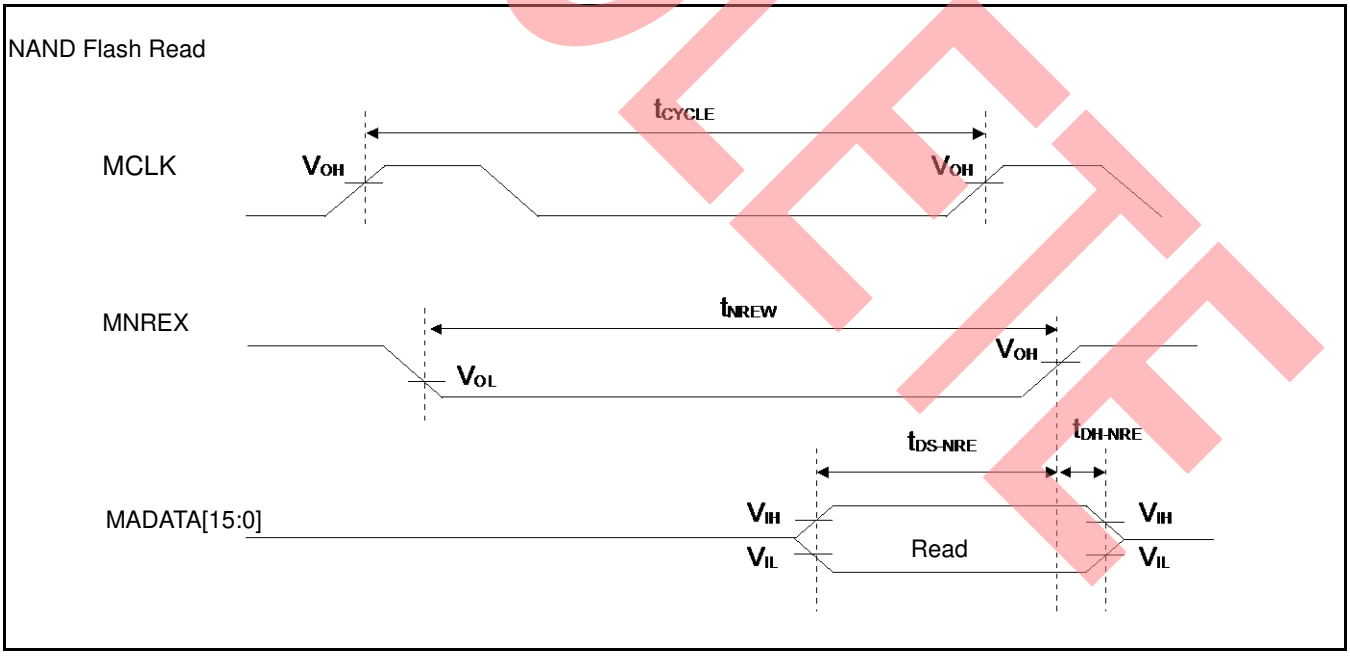
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data set up →MNREX↑ time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE↑→ MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→ MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→ MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→ MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX↓→ Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX↑→ Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

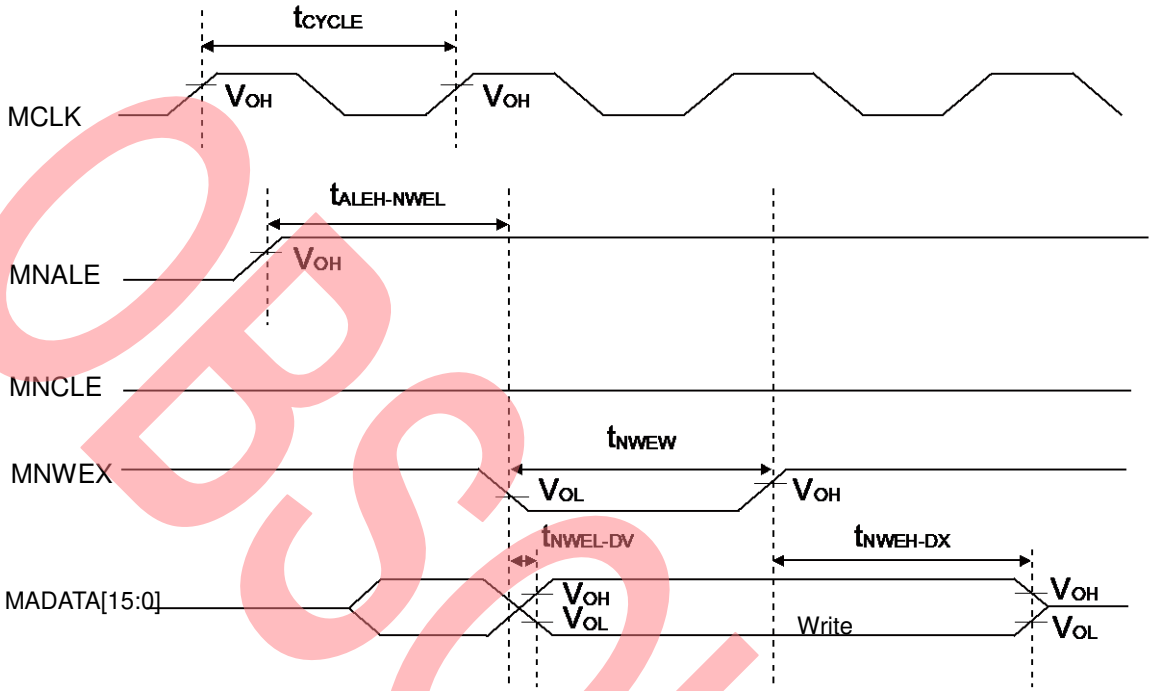
Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

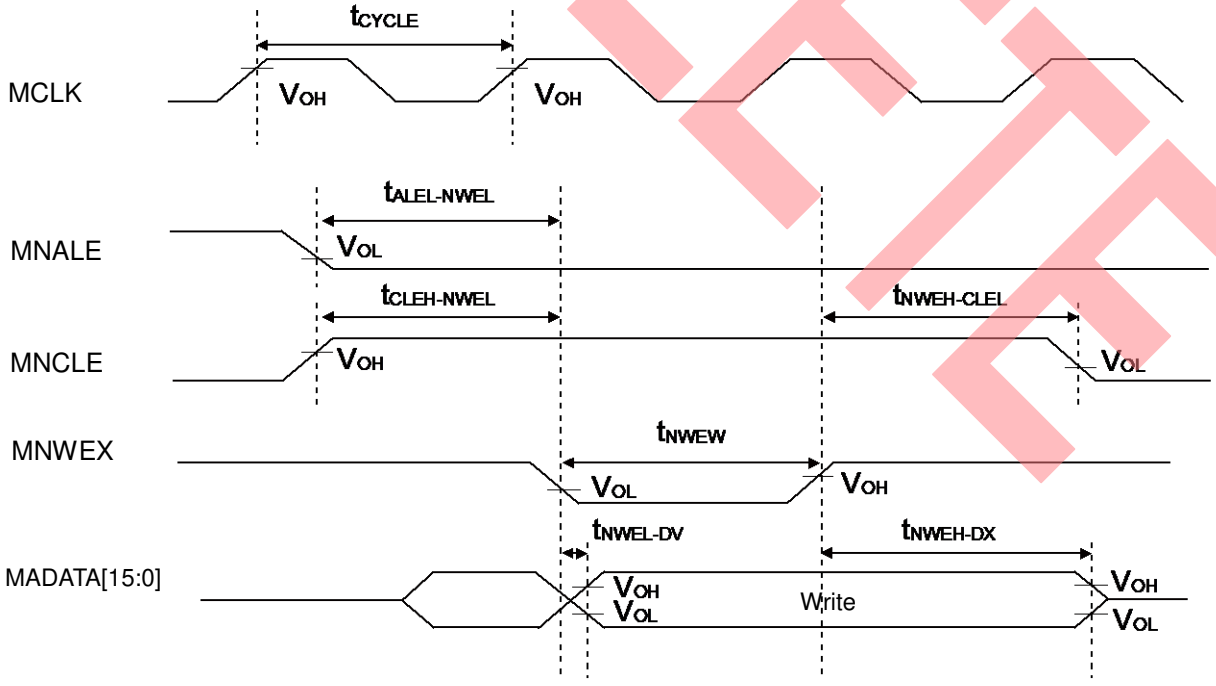
NAND Flash Read



NAND Flash Address Write



NAND Flash Command Write

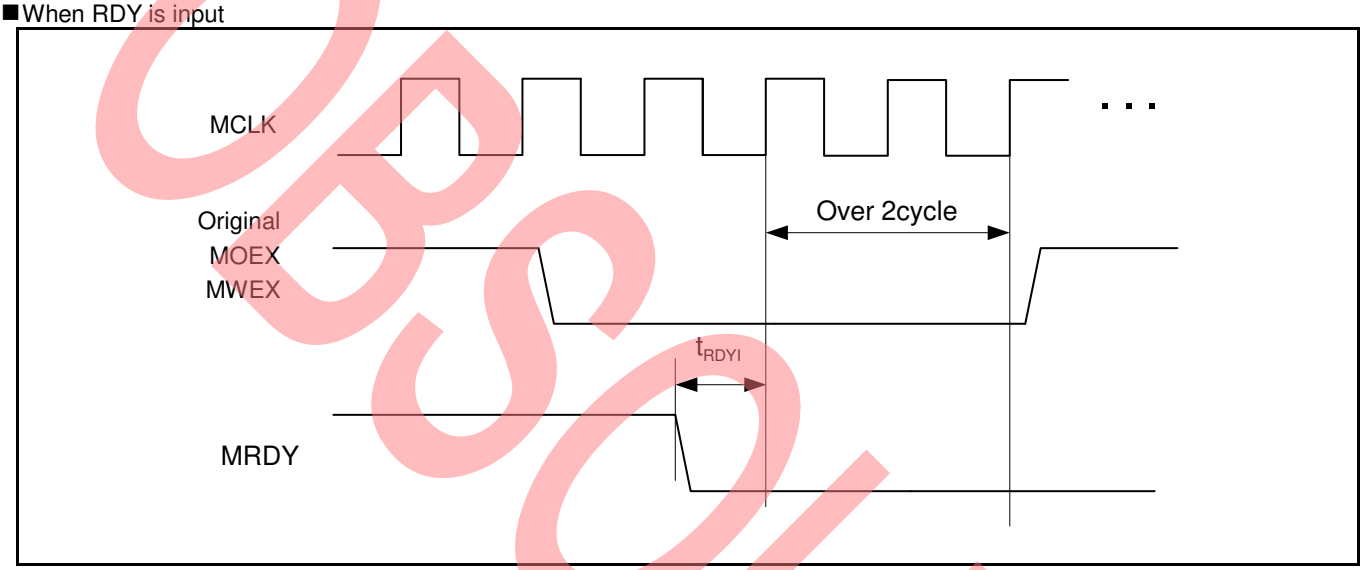


External Ready Input Timing

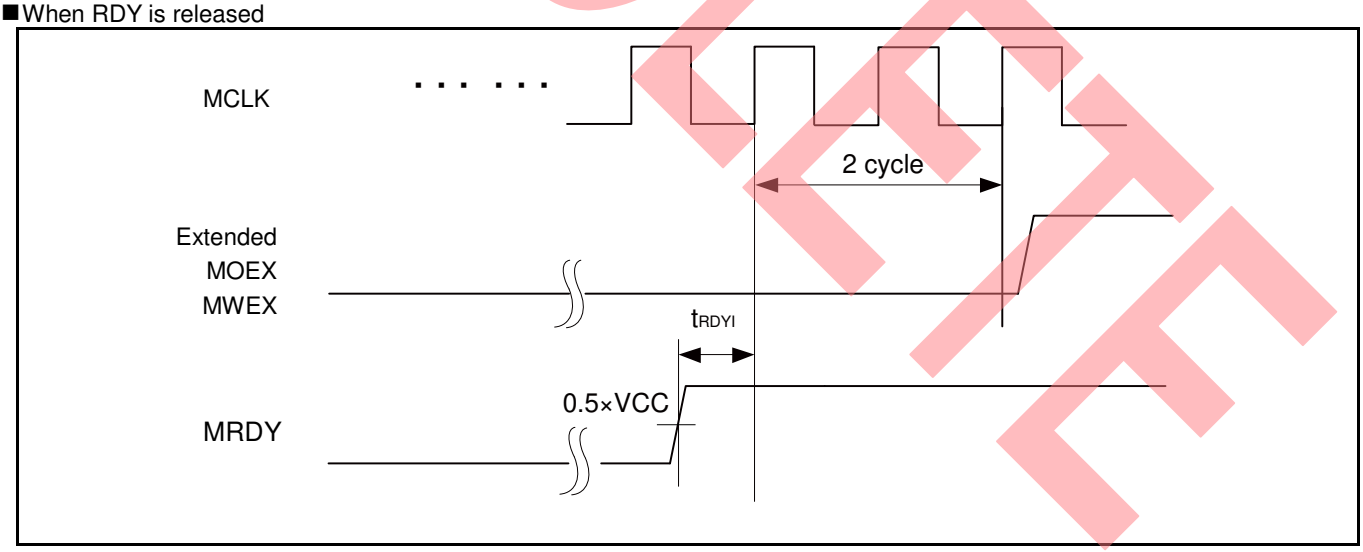
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

■When RDY is input



■When RDY is released



SDRAM Mode

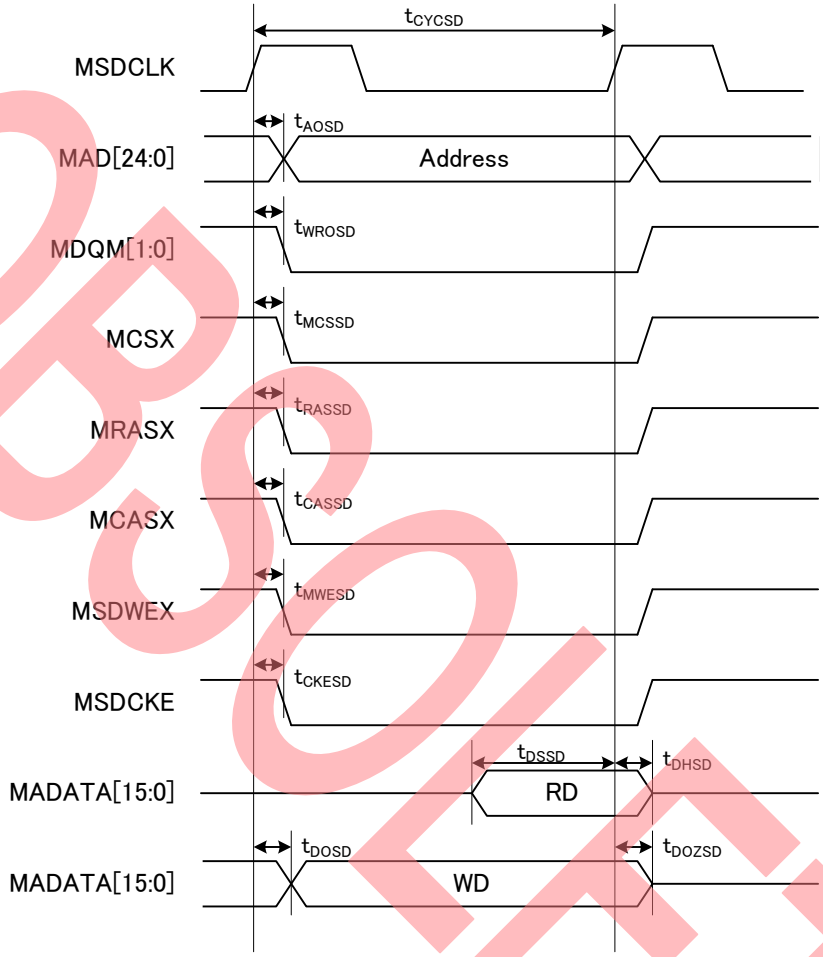
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Output frequency	t_{CYCSD}	MSDCLK	-	32	MHz
Address delay time	t_{AOSD}	MSDCLK, MAD[15:0]	2	12	ns
MSDCLK↑→Data output delay time	t_{DOSD}	MSDCLK, MADATA[31:0]	2	12	ns
MSDCLK↑→Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[31:0]	2	20	ns
MDQM[1:0] delay time	t_{WROSD}	MSDCLK, MDQM[1:0]	1	12	ns
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	2	12	ns
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	2	12	ns
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	2	12	ns
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	2	12	ns
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	2	12	ns
Data set up time	t_{DSSD}	MSDCLK, MADATA[31:0]	23	-	ns
Data hold time	t_{DHSD}	MSDCLK, MADATA[31:0]	0	-	ns

Note:

- *When the external load capacitance C_L = 30 pF*

SDRAM Access

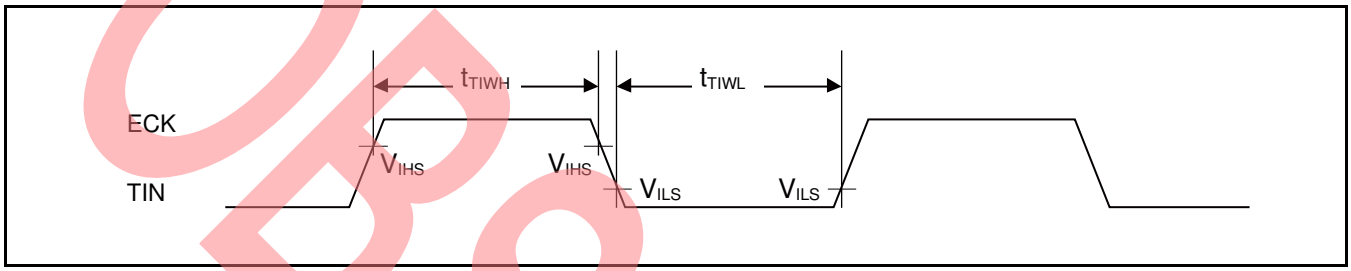


12.4.10 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

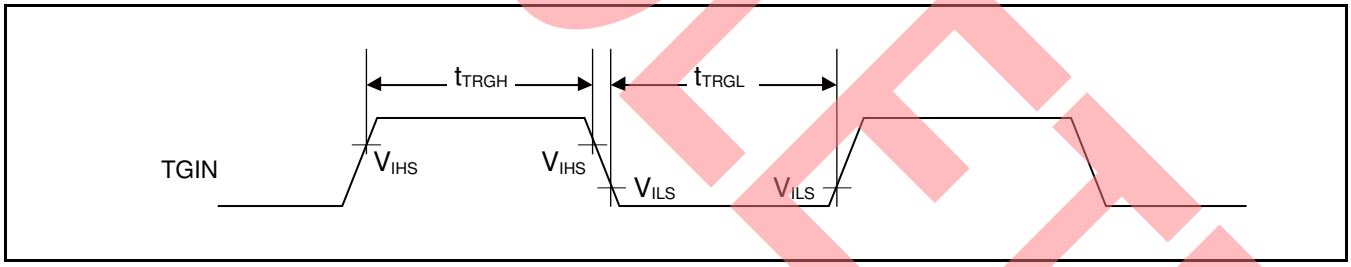
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see 8. Block Diagram in this data sheet.

12.4.11 CSIO Timing

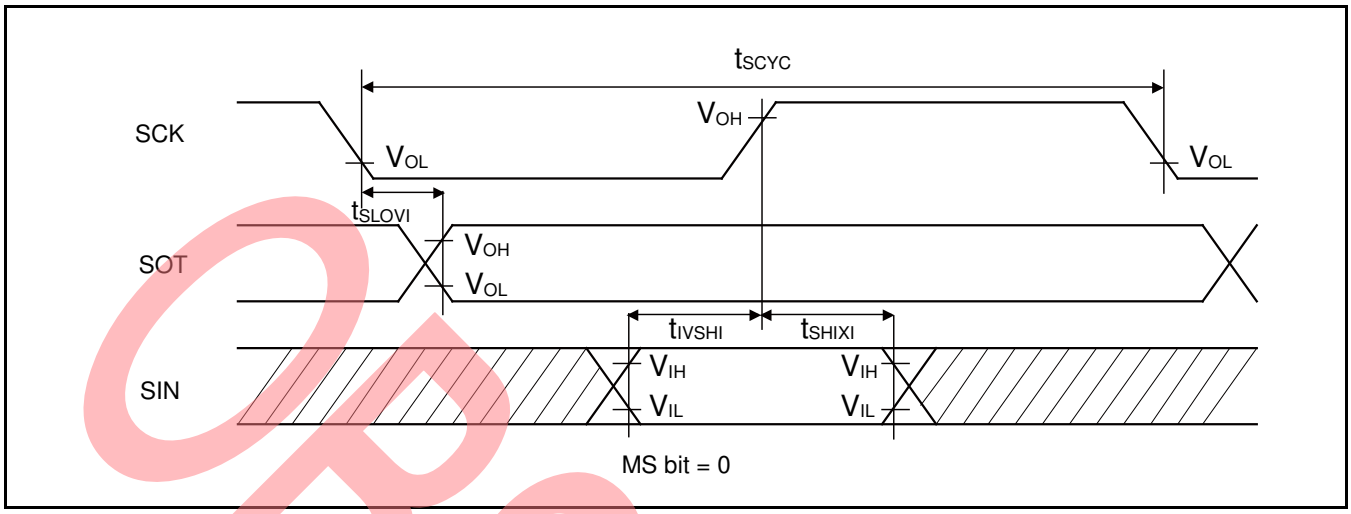
Synchronous Serial (SPI = 0, SCINV = 0)

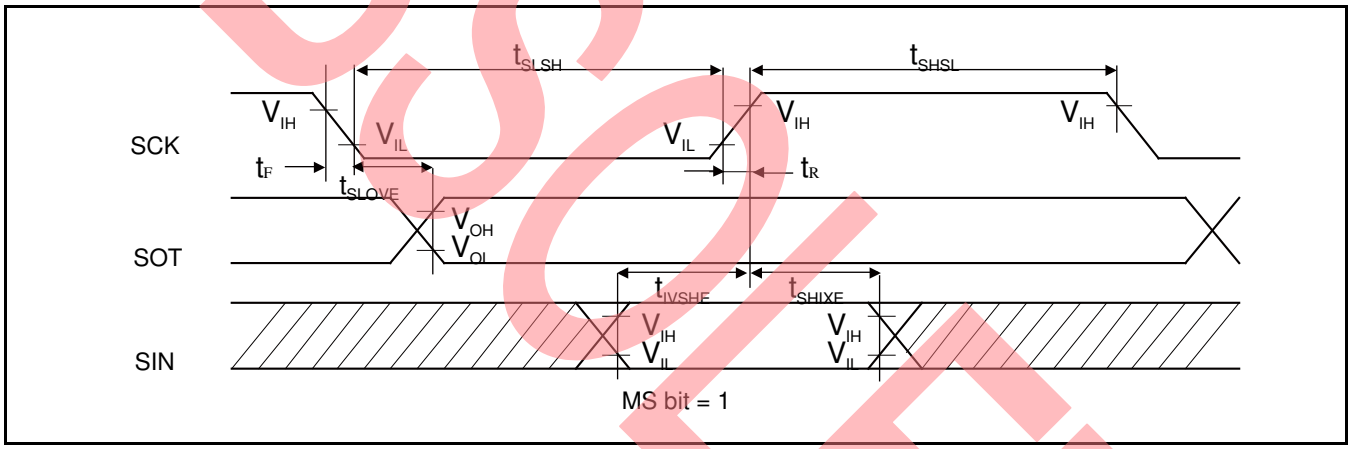
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIH
VIH
tF
tR
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

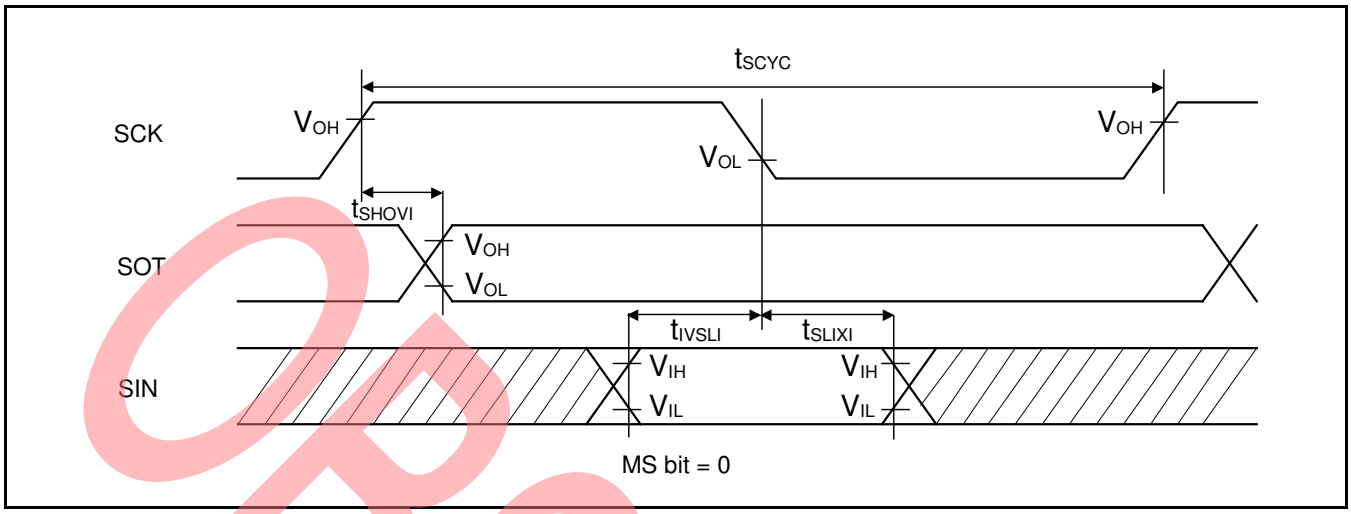
Synchronous Serial (SPI = 0, SCINV = 1)

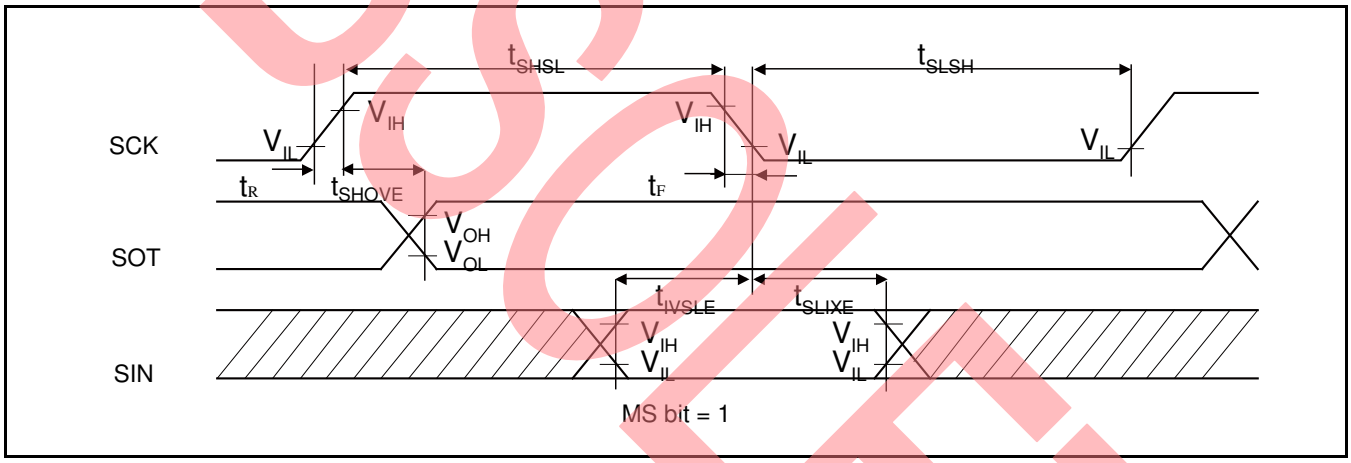
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2tC_{YCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*


tSCYC
SCK
VOH
VOL
VOH
tSHOVI
SOT
VOH
VOL
tIVSLI
tSLIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSHSL
tSLSH
SCK
VIL
VIH
VIH
VIL
VIL
tR
tSHOVE
tF
SOT
VOH
VOL
tIVSLE
tSLIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

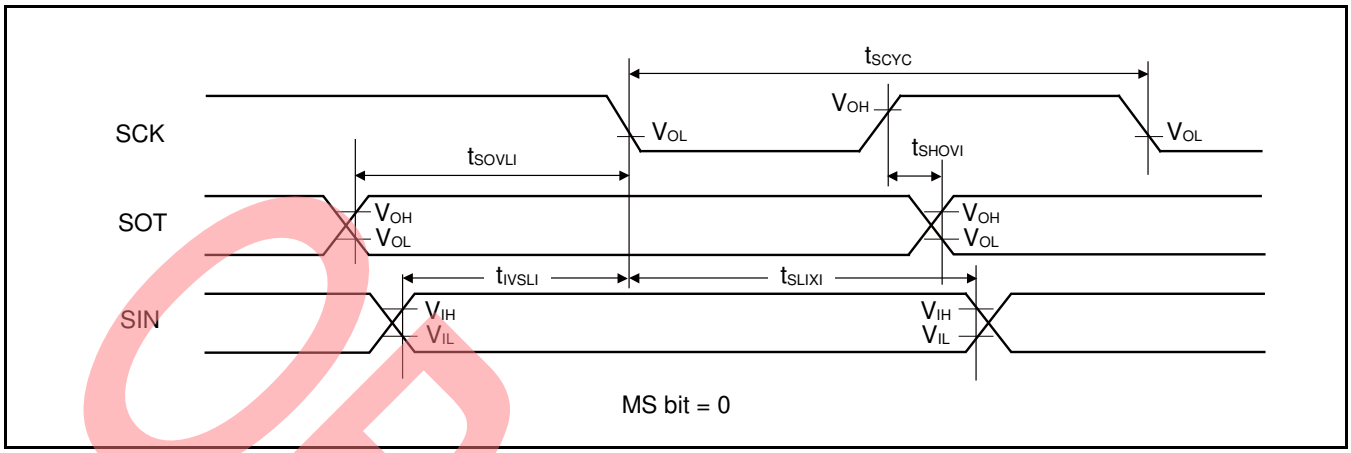
Synchronous Serial (SPI = 1, SCINV = 0)

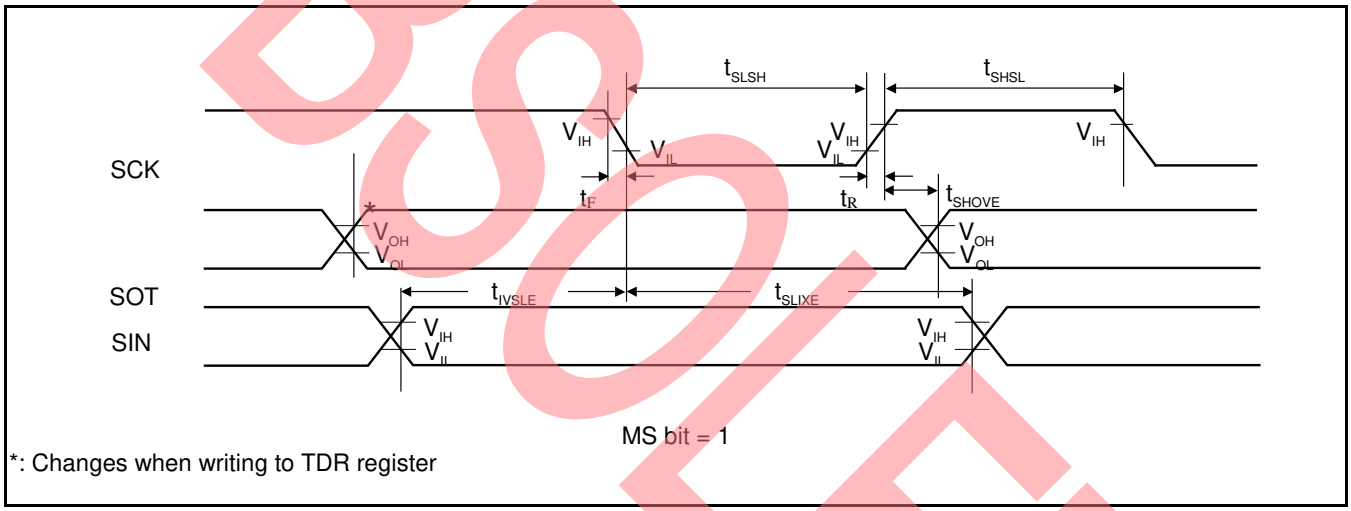
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*





*: Changes when writing to TDR register

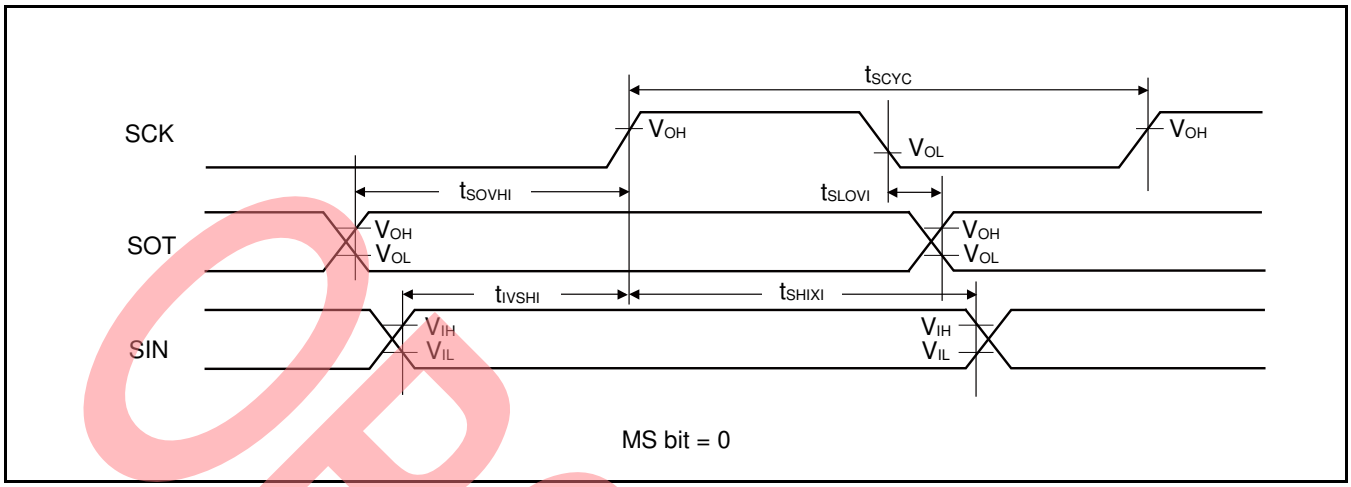
Synchronous Serial (SPI = 1, SCINV = 1)

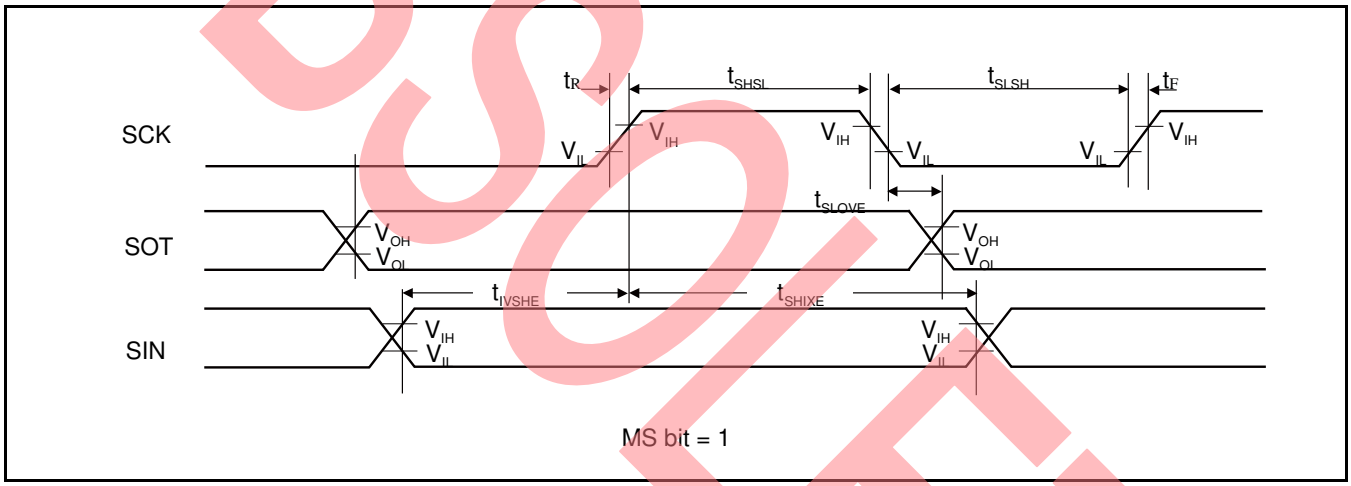
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2tC_{YCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*


tSCYC
SCK
VOH
VOL
VOH
tSOVHI
tSLOVI
SOT
VOH
VOL
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tR
tSHSL
tSLSH
tF
SCK
VIL
VIH
VIH
VIL
VIL
VIH
tSLOVE
SOT
VOH
VOL
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3tC_{YCP}+30	-	ns
SCS↓→SUT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SUT delay time	t_{DEE}		0	-	0	-	ns

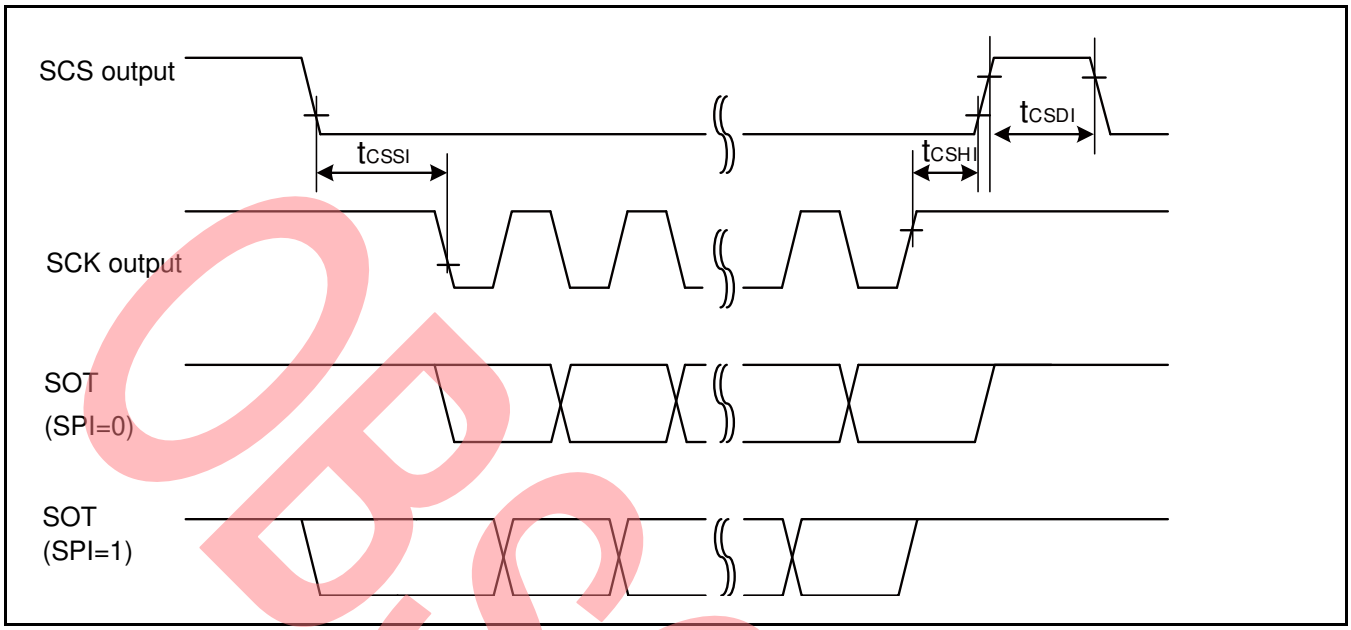
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

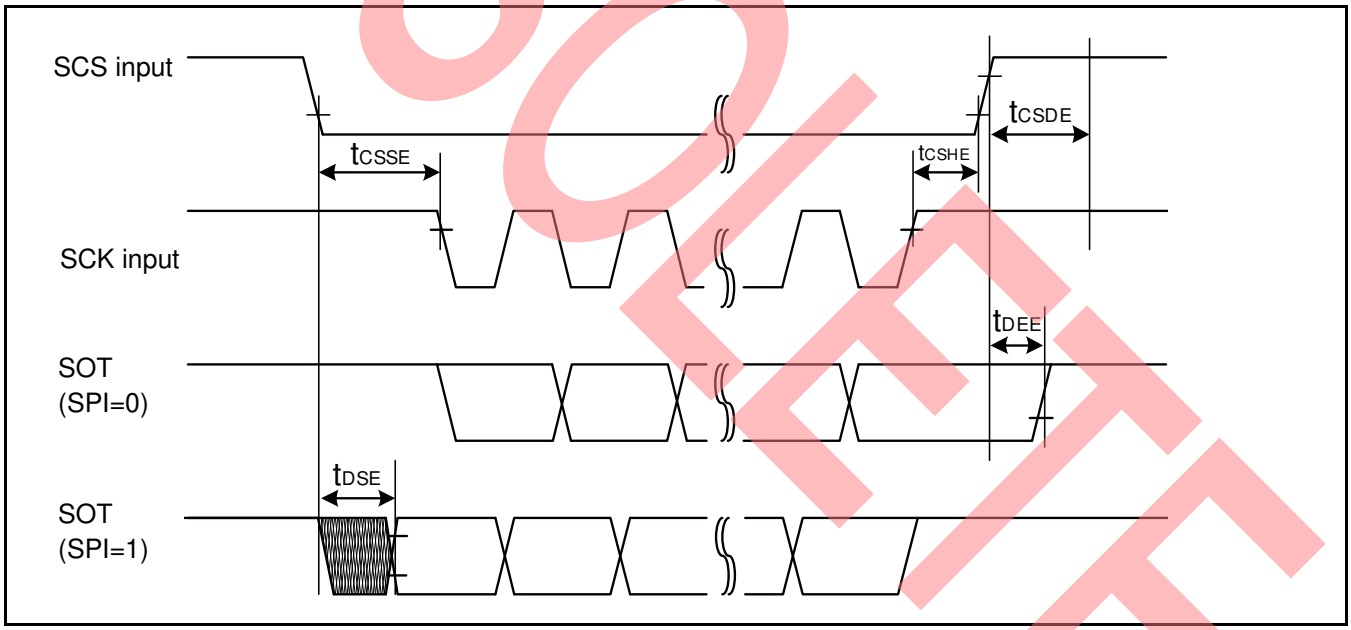
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5tC_{YCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

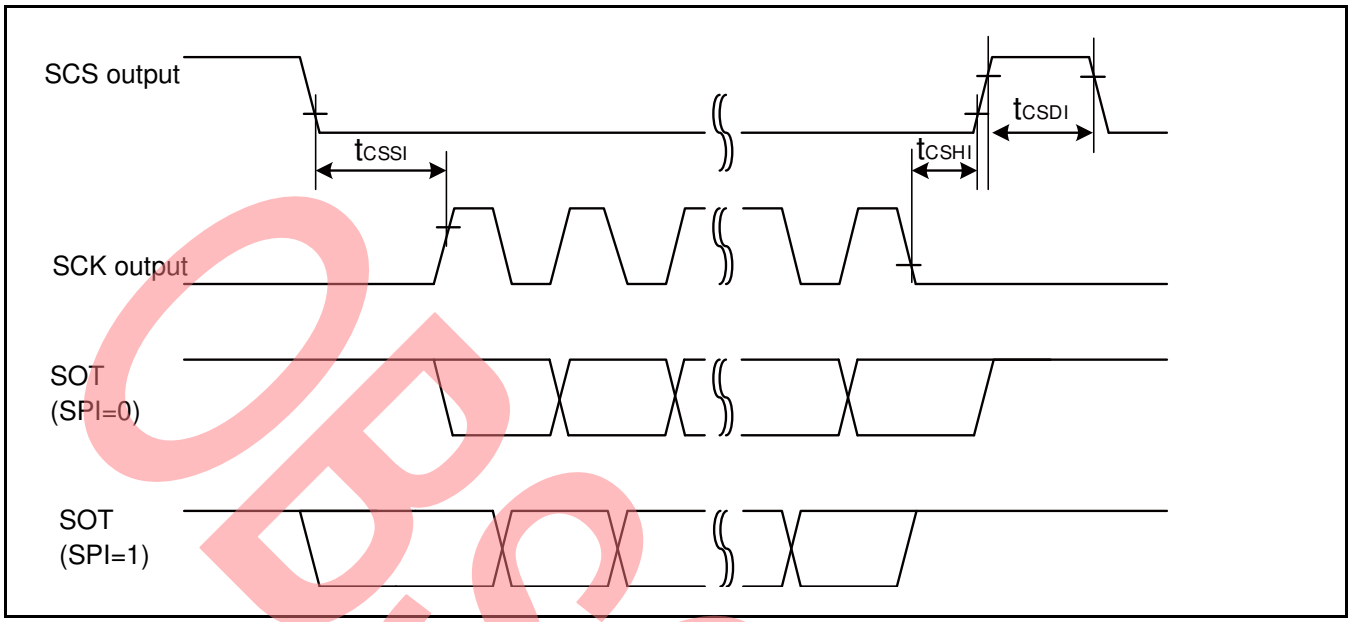
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

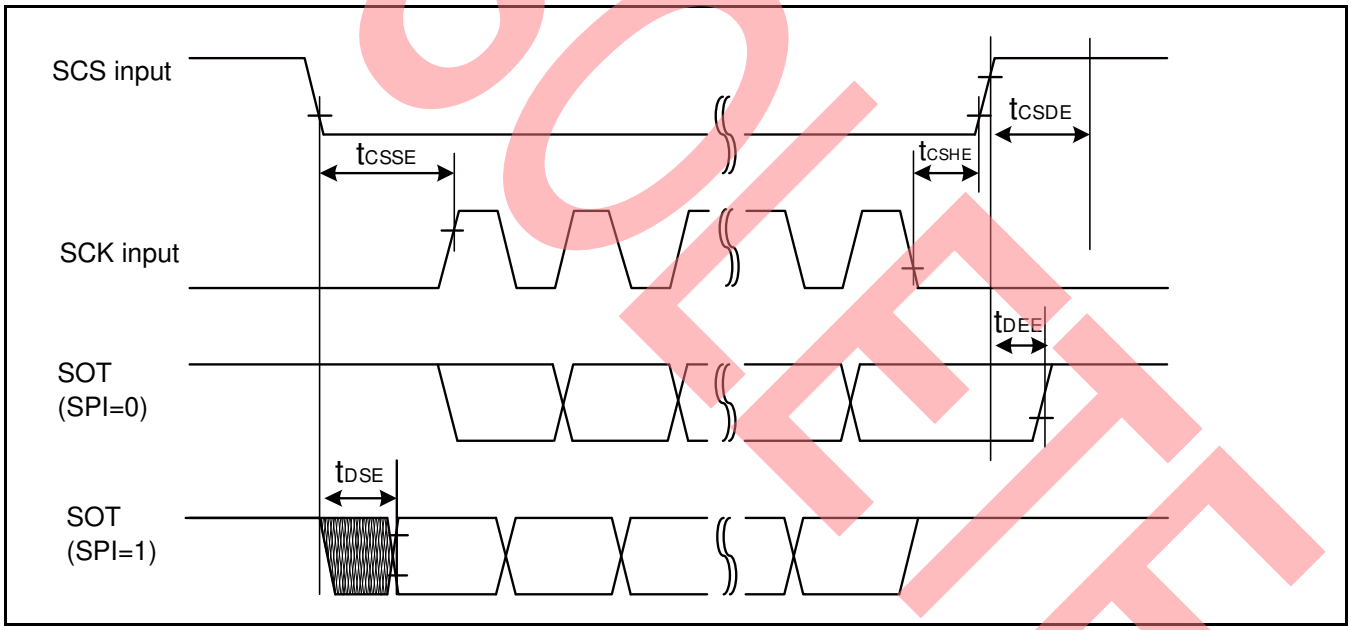
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

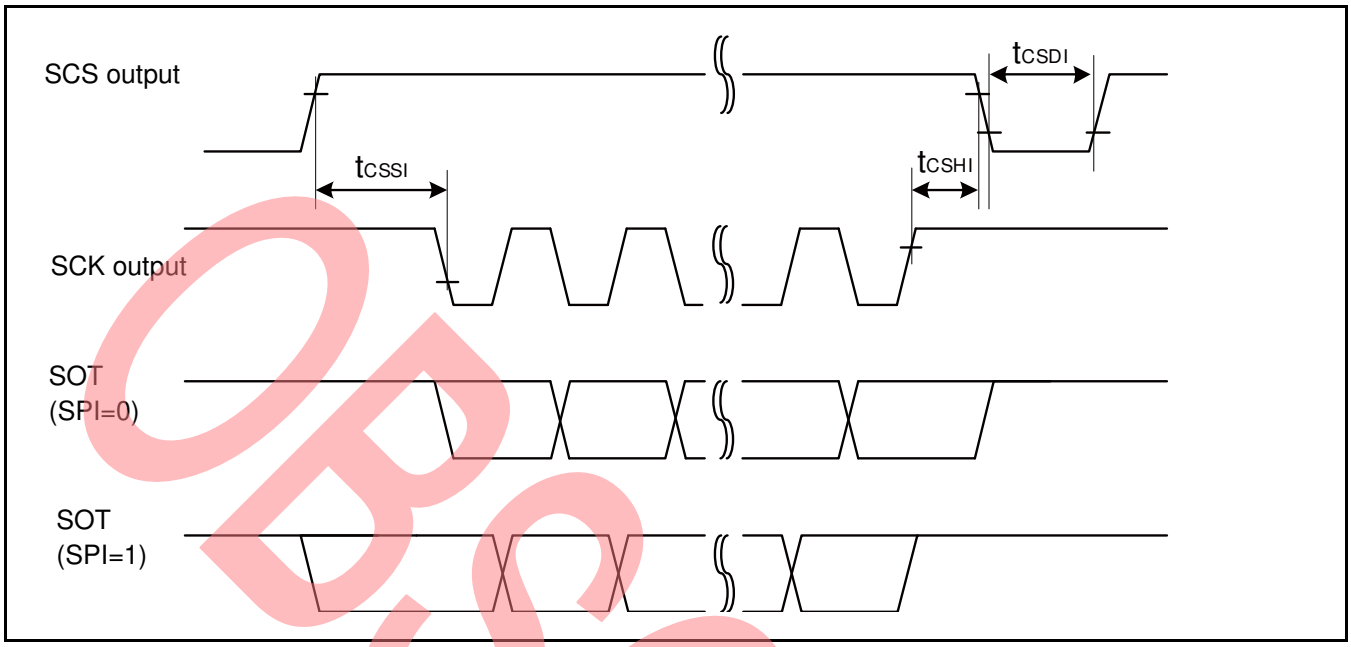
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

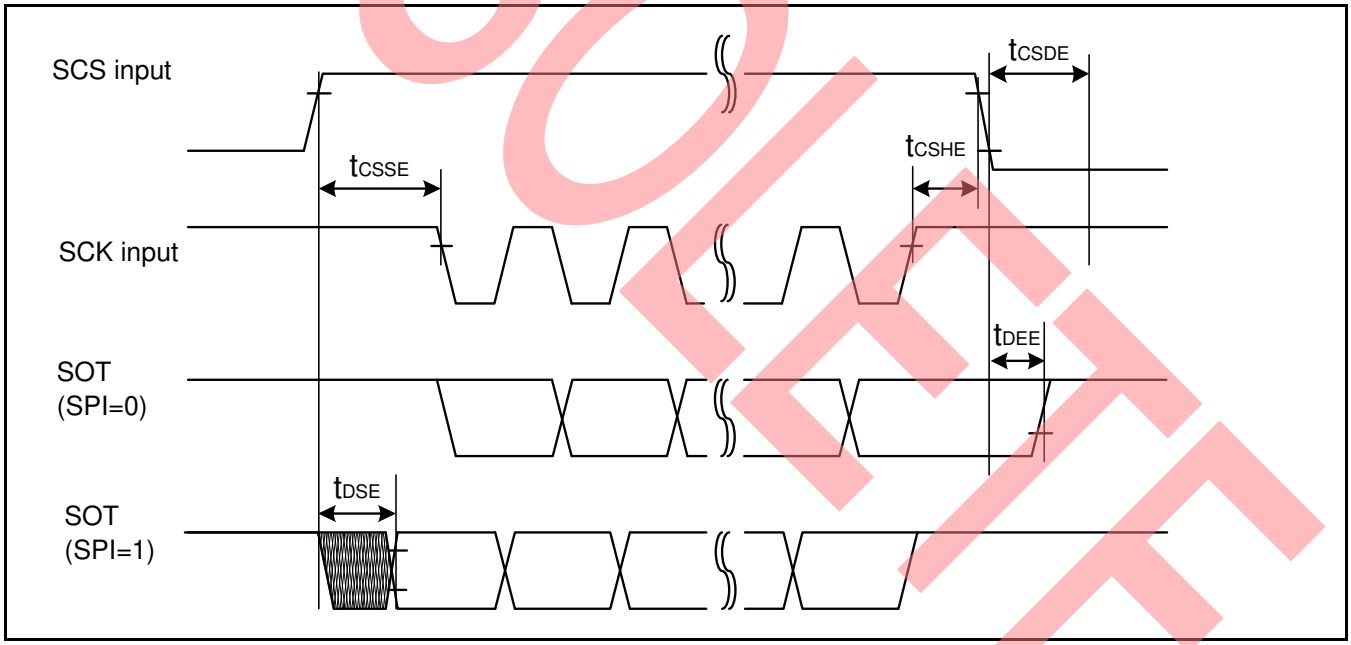
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

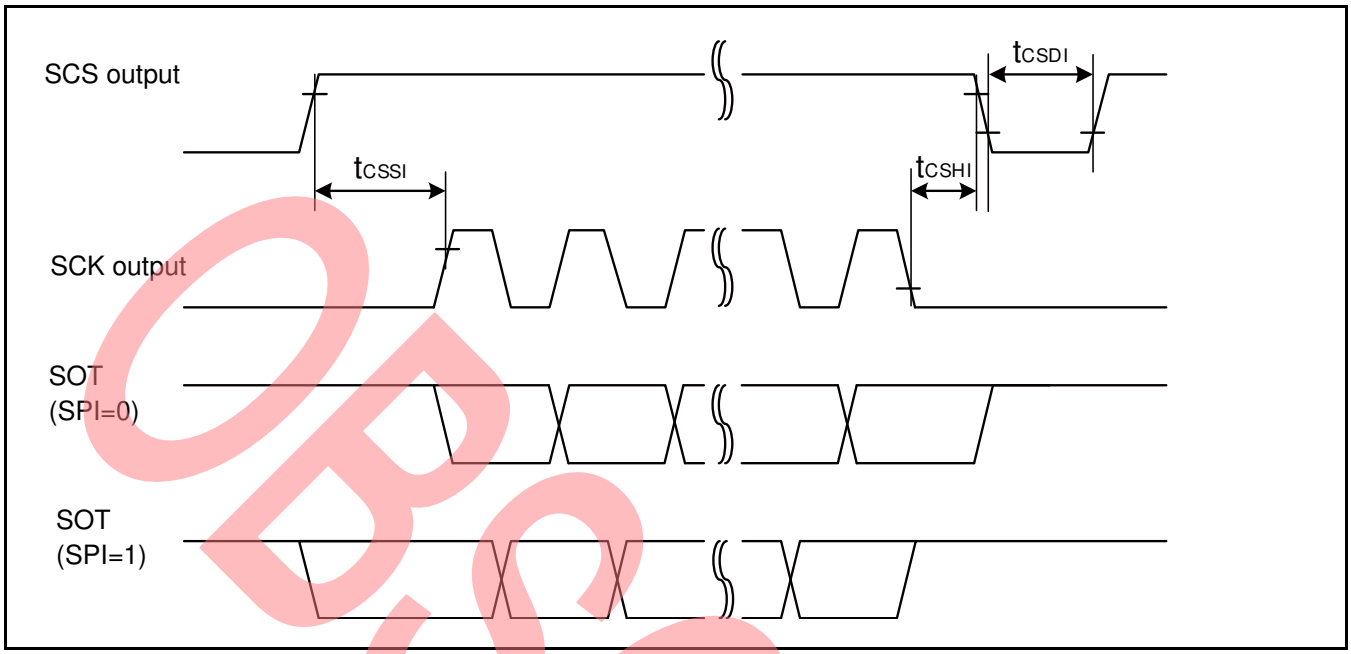
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

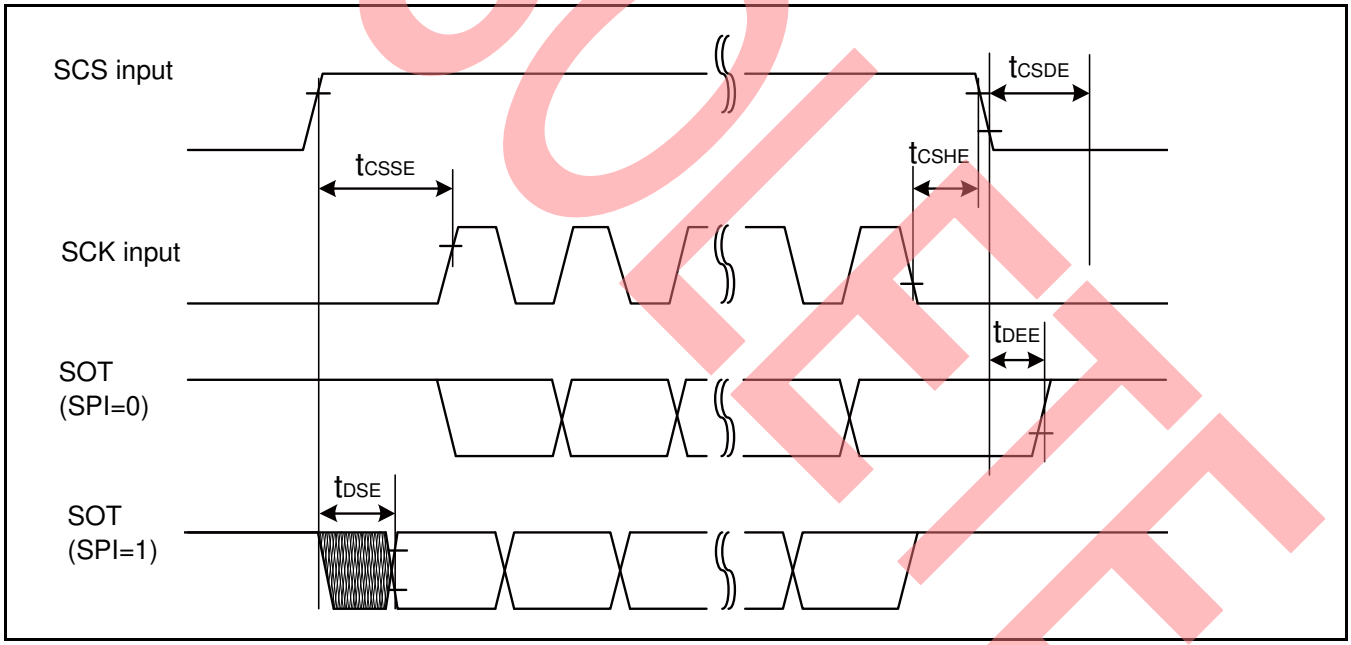
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

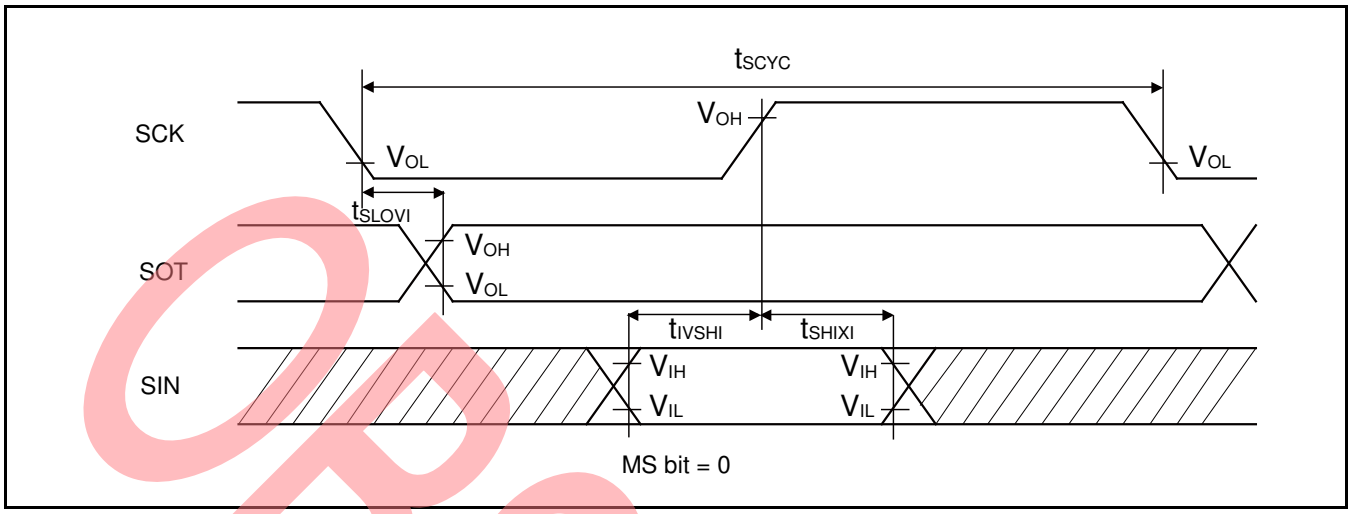
High-speed Synchronous Serial (SPI = 0, SCINV = 0)

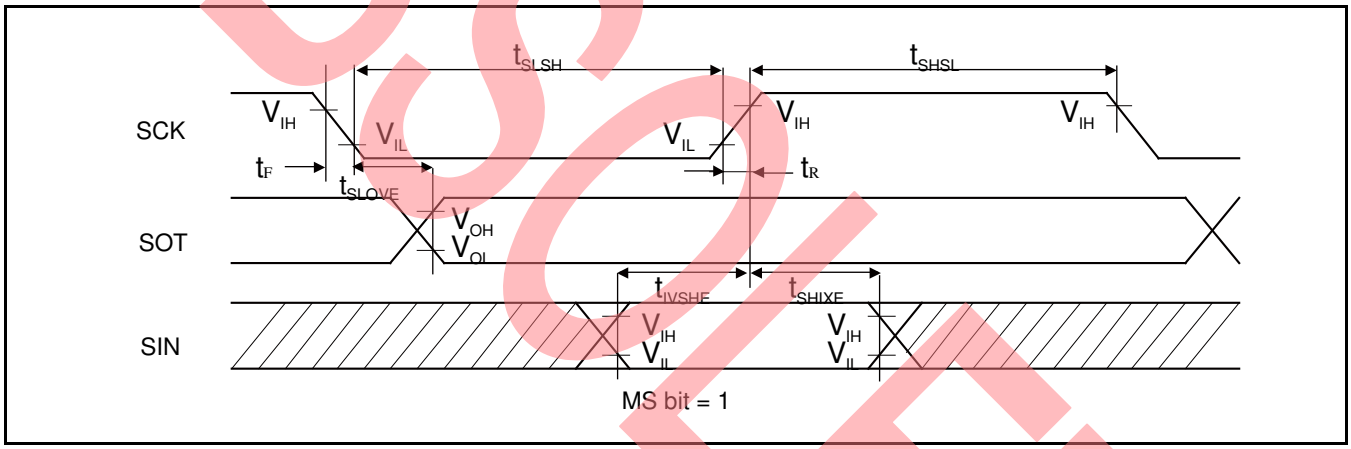
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIH
VIH
tF
tR
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

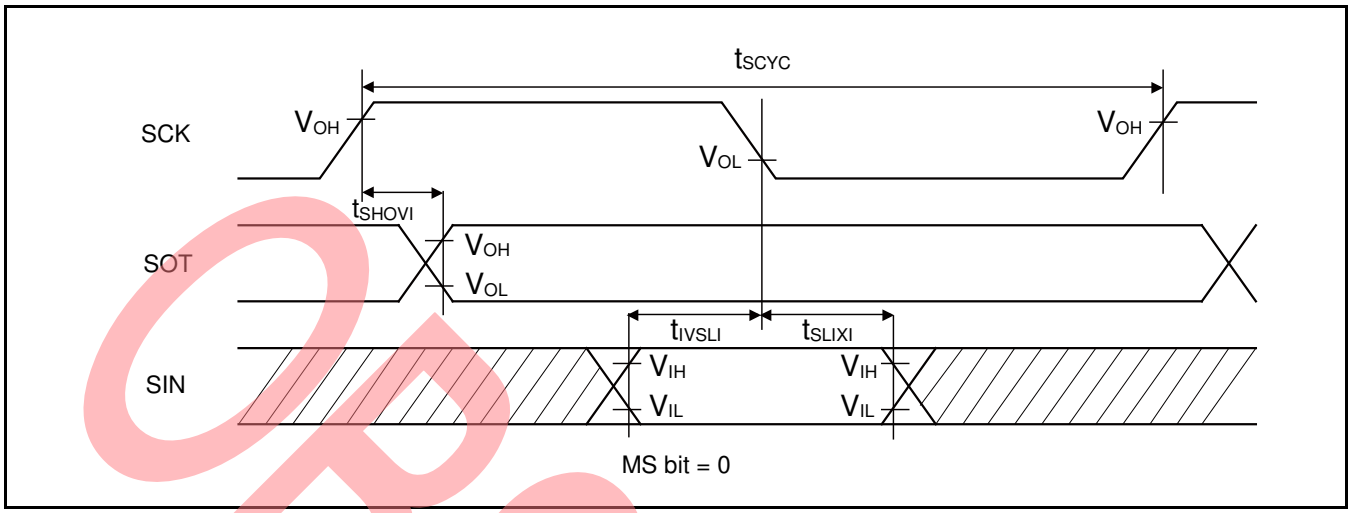
High-speed Synchronous Serial (SPI = 0, SCINV = 1)

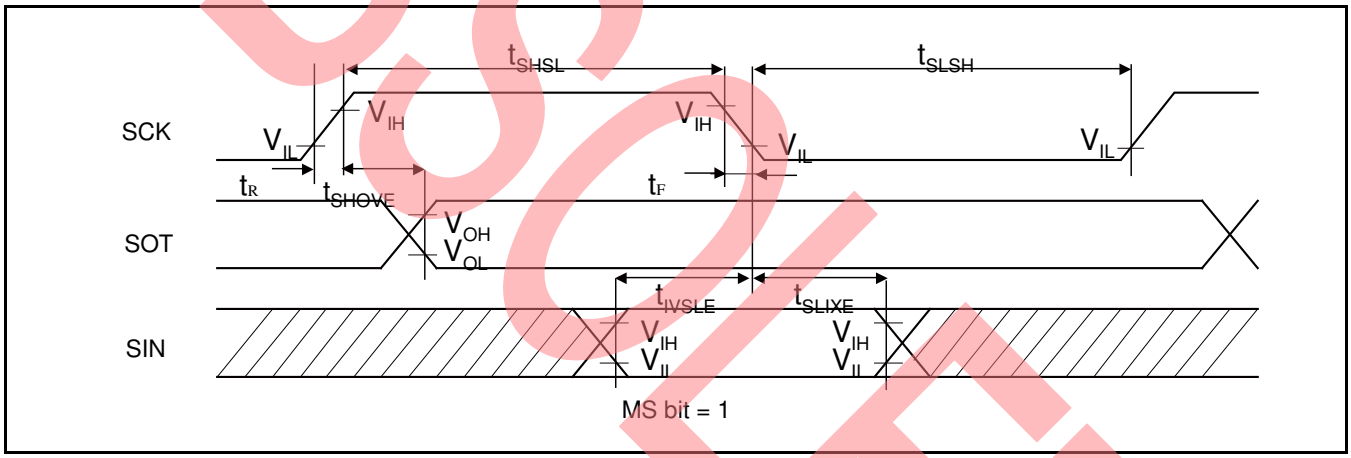
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK ↓ →SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP} - 5$	-	$2t_{CYCP} - 5$	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↑ →SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK ↓ →SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*


tSCYC
SCK
VOH
VOL
VOH
tSHOVI
SOT
VOH
VOL
tIVSLI
tSLIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSHSL
tSLSH
SCK
VIL
VIH
VIH
VIL
VIL
tR
tSHOVE
tF
SOT
VOH
VOL
tIVSLE
tSLIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

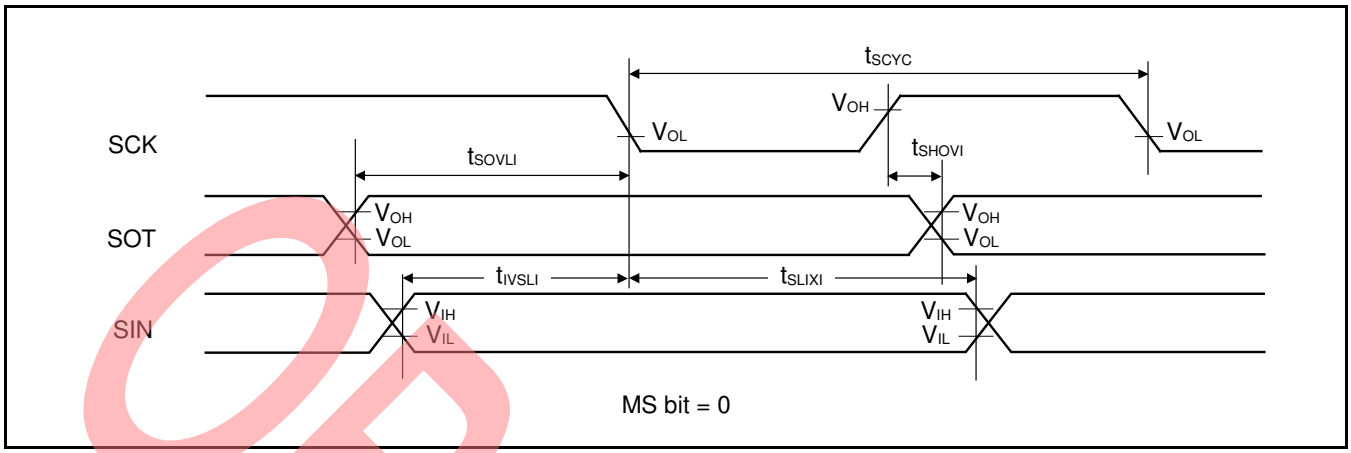
High-speed Synchronous Serial (SPI = 1, SCINV = 0)

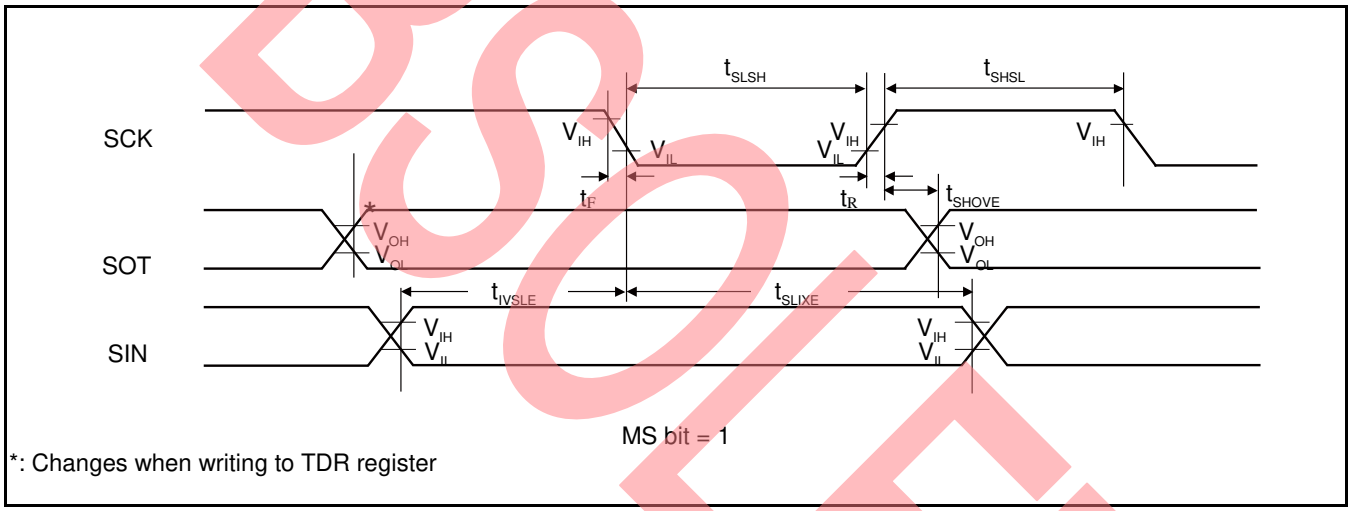
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*





*: Changes when writing to TDR register

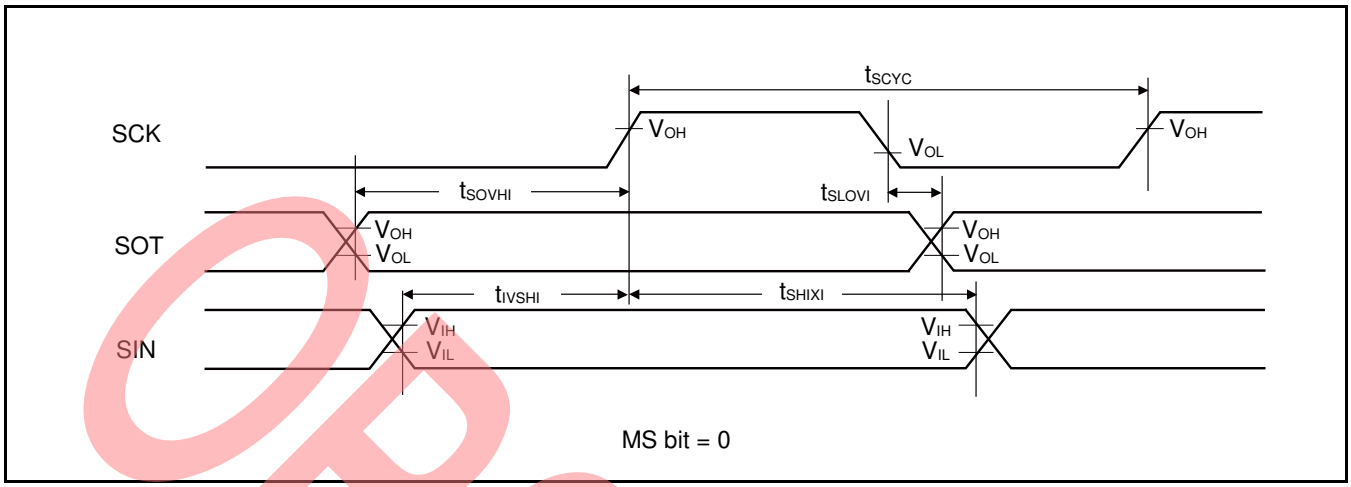
High-speed Synchronous Serial (SPI = 1, SCINV = 1)

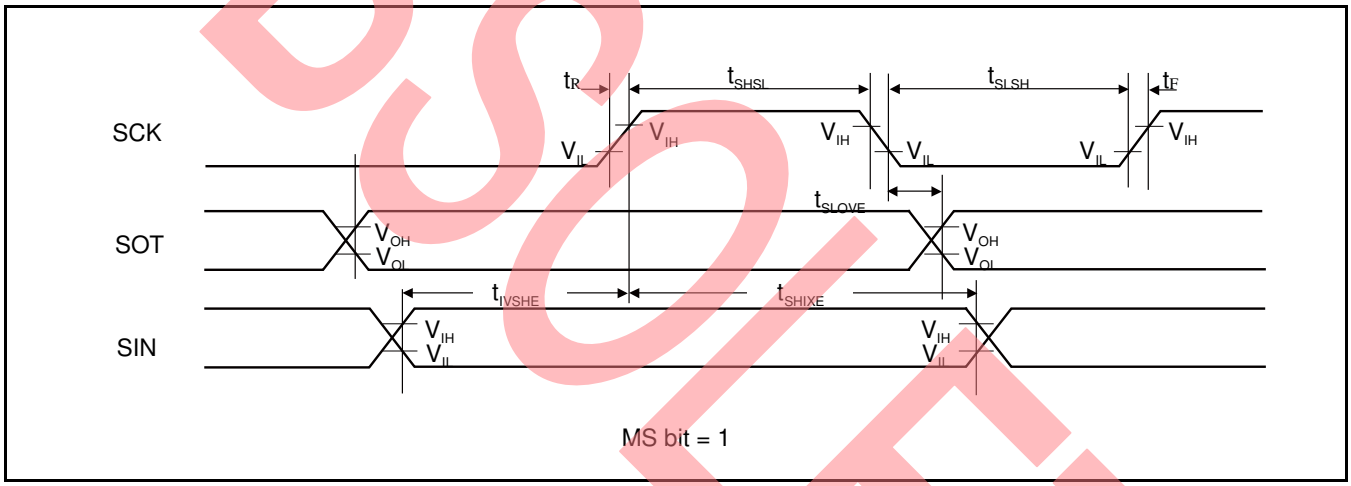
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Internal shift clock operation	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ →SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK ↑ →SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ →SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK ↑ →SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*


SCK
SOT
SIN
tSCYC
VOH
VOL
tSOVHI
tSLOVI
tIVSHI
tSHIXI
VIH
VIL
MS bit = 0


SCK
SOT
SIN
tR
tSHSL
tSLSH
tF
VIH
VIL
tSLOVE
VOH
VOL
tIVSHE
tSHIXE
MS bit = 1

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

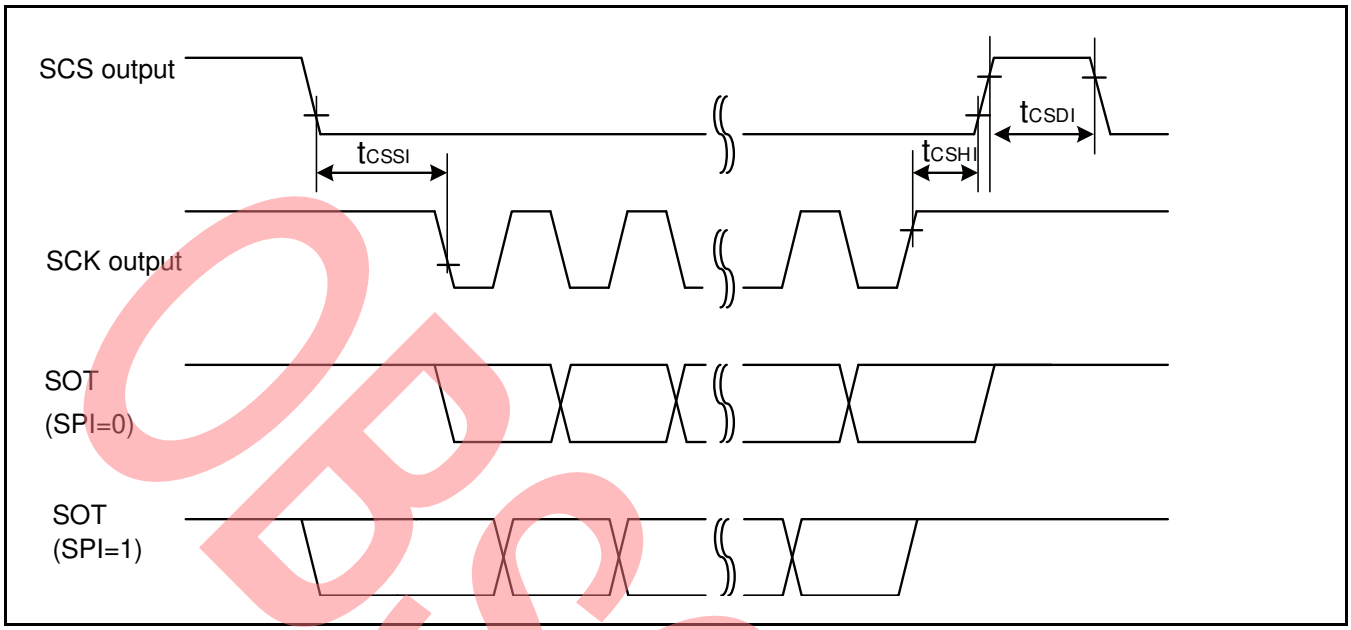
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

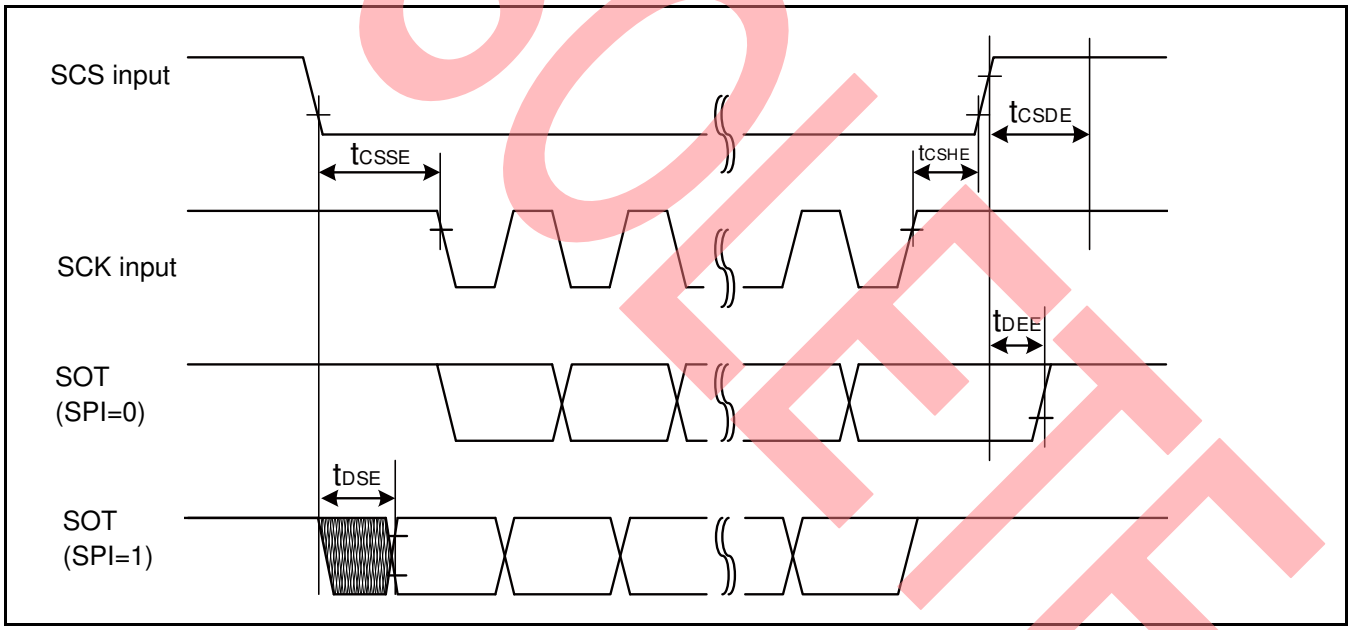
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual.*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

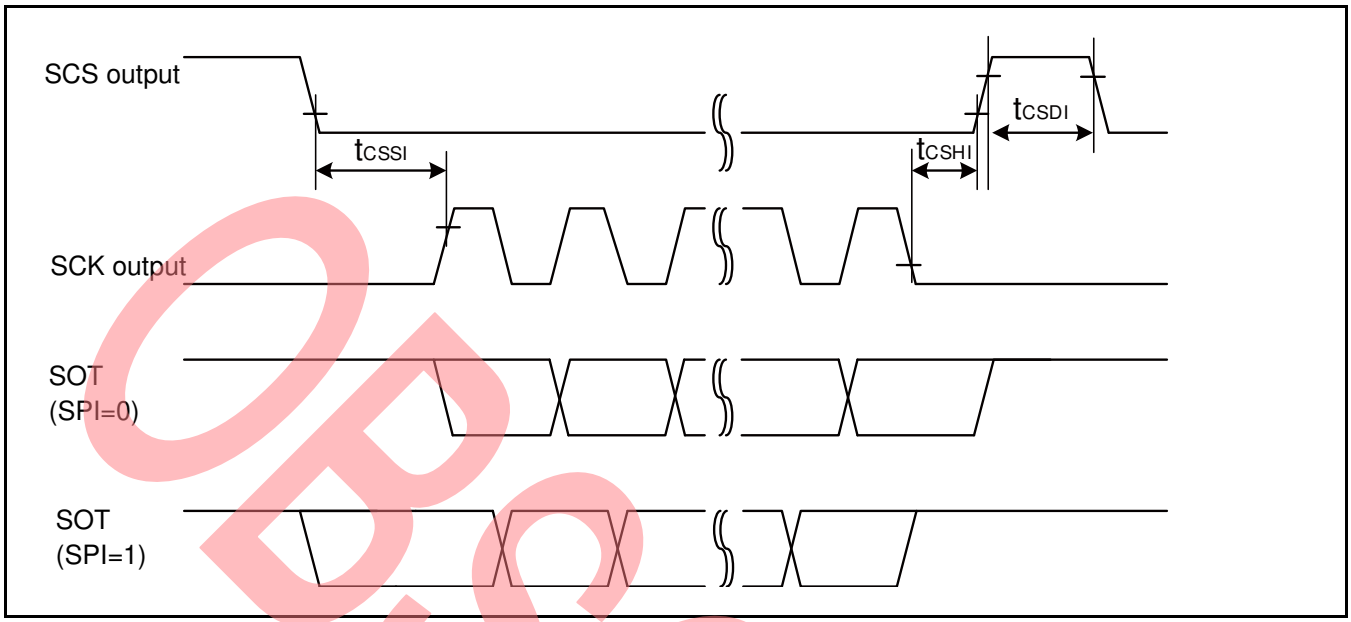
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

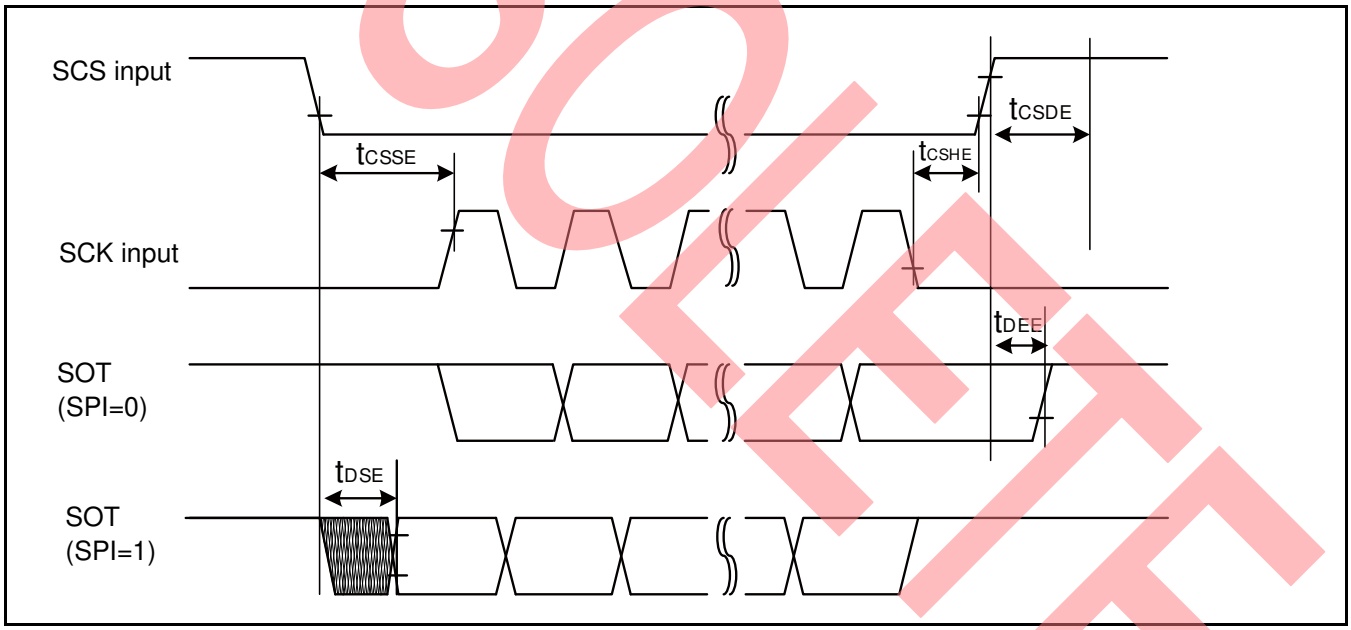
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

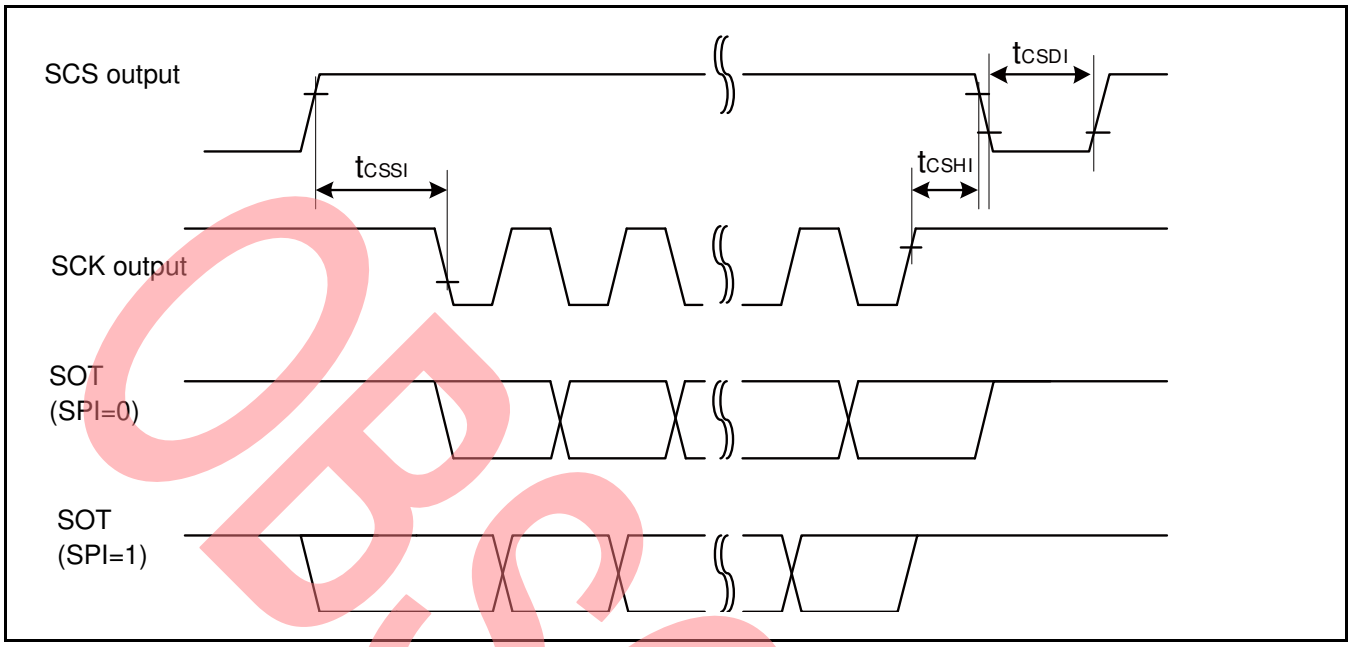
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

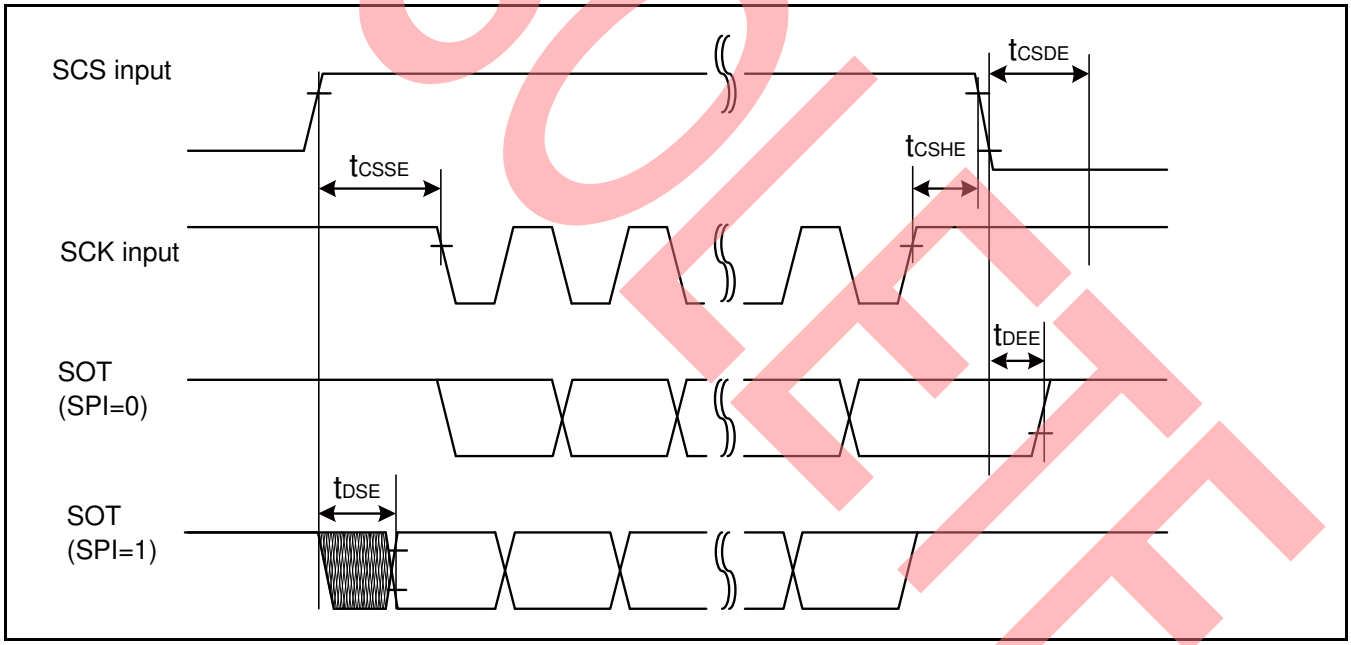
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

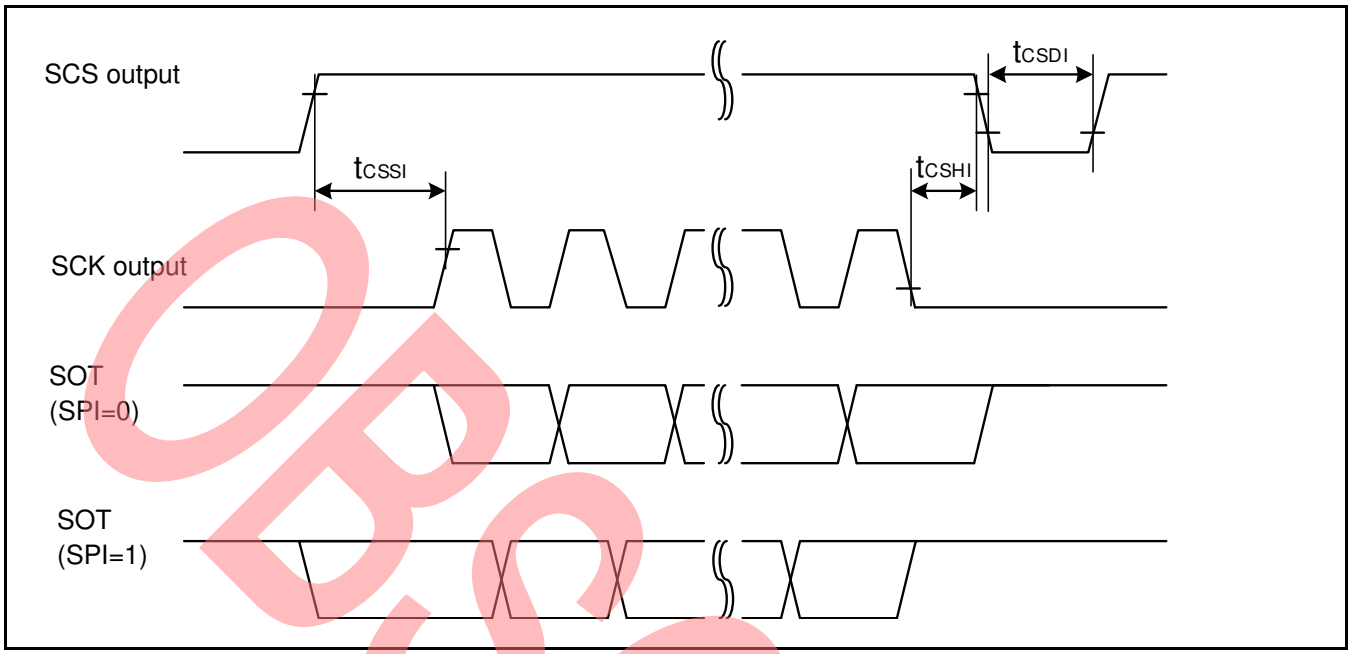
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

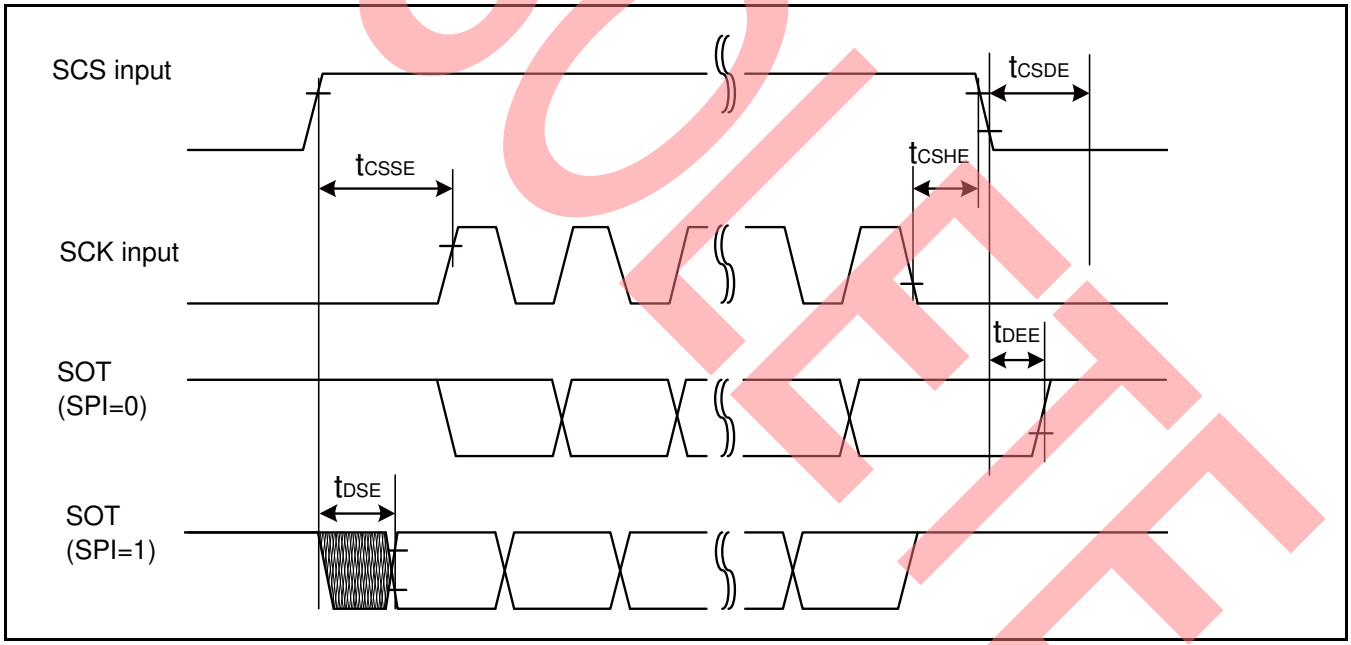
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*

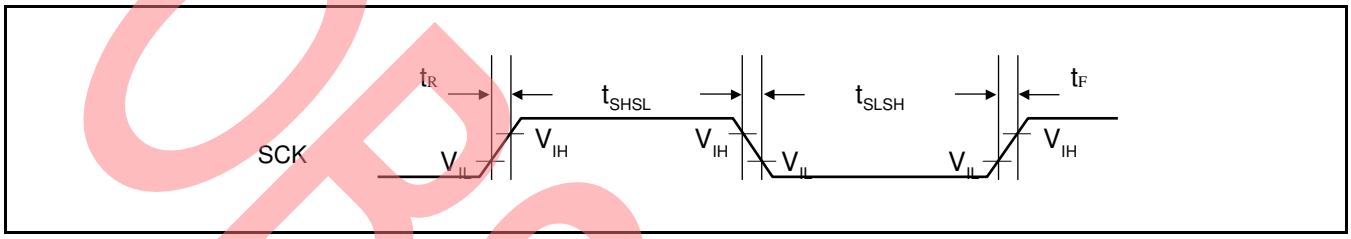

SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.4.12 External Input Timing

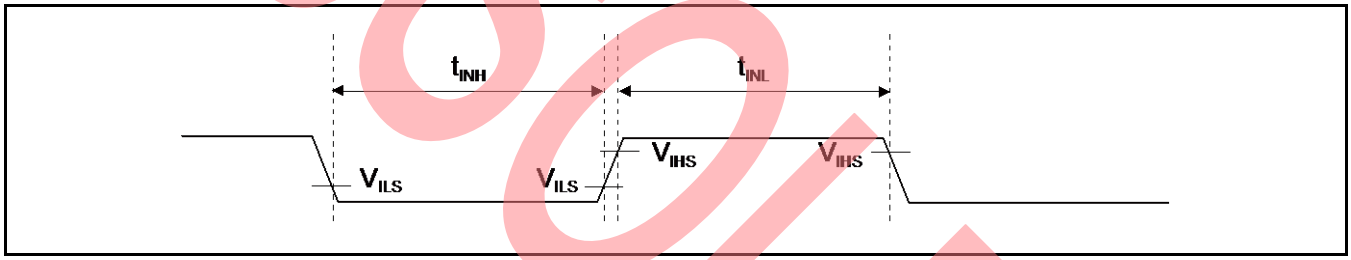
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode. About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see 8. Block Diagram in this data sheet.

*2: When in Stop mode, in timer mode.

*3: When in deep standby RTC mode, in deep standby Stop mode.

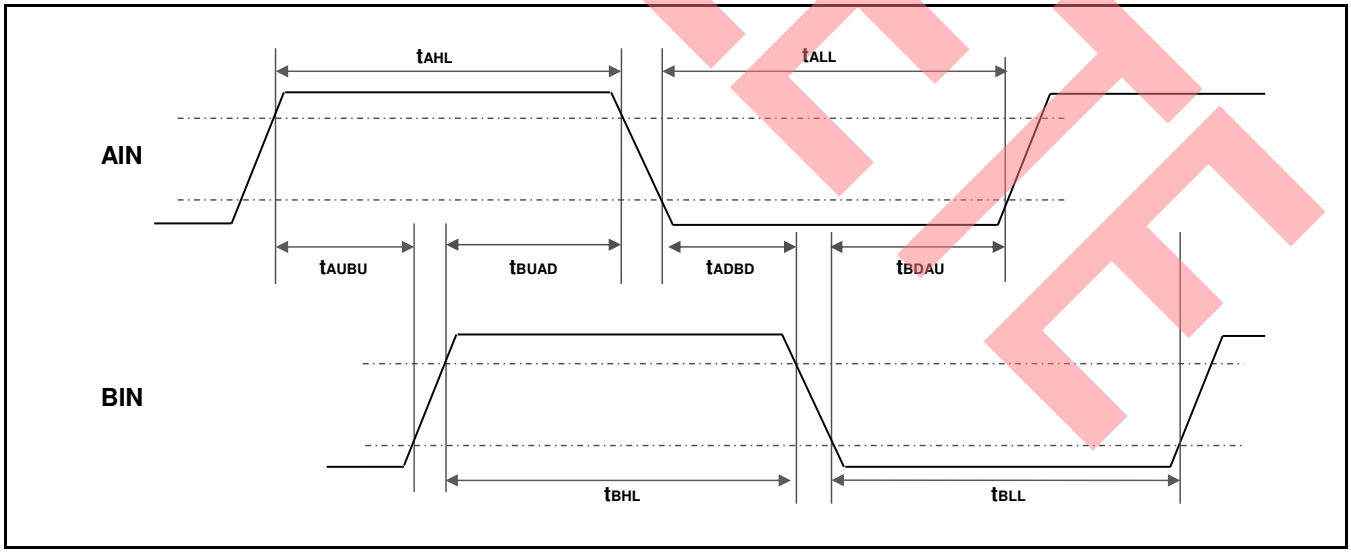


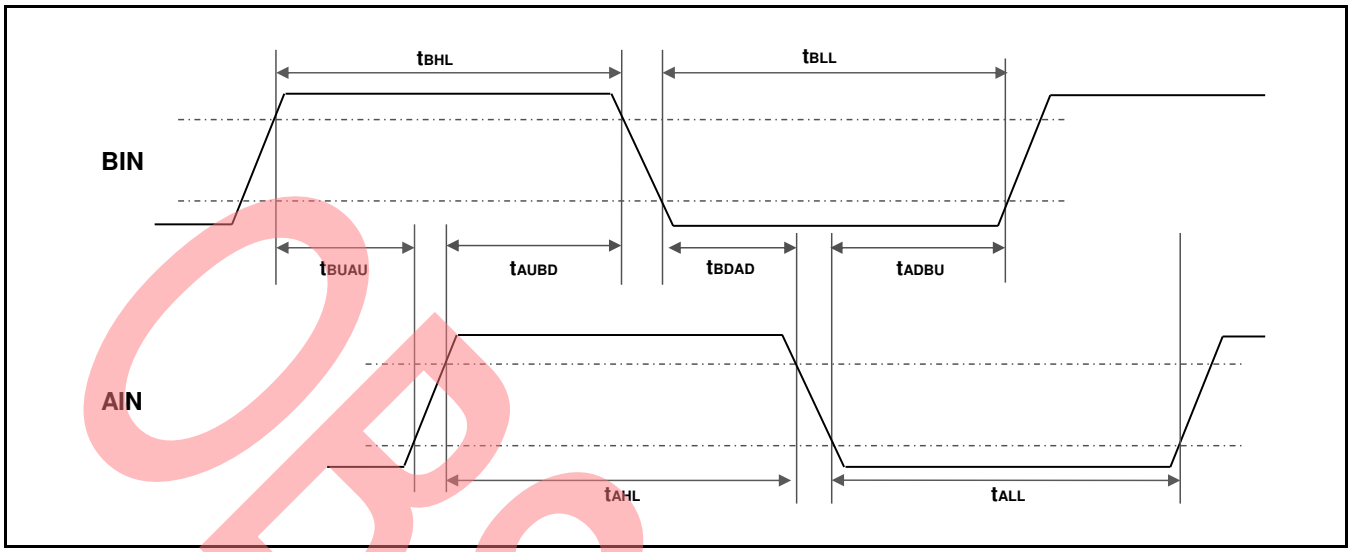
12.4.13 Quadrature Position/Revolution Counter Timing

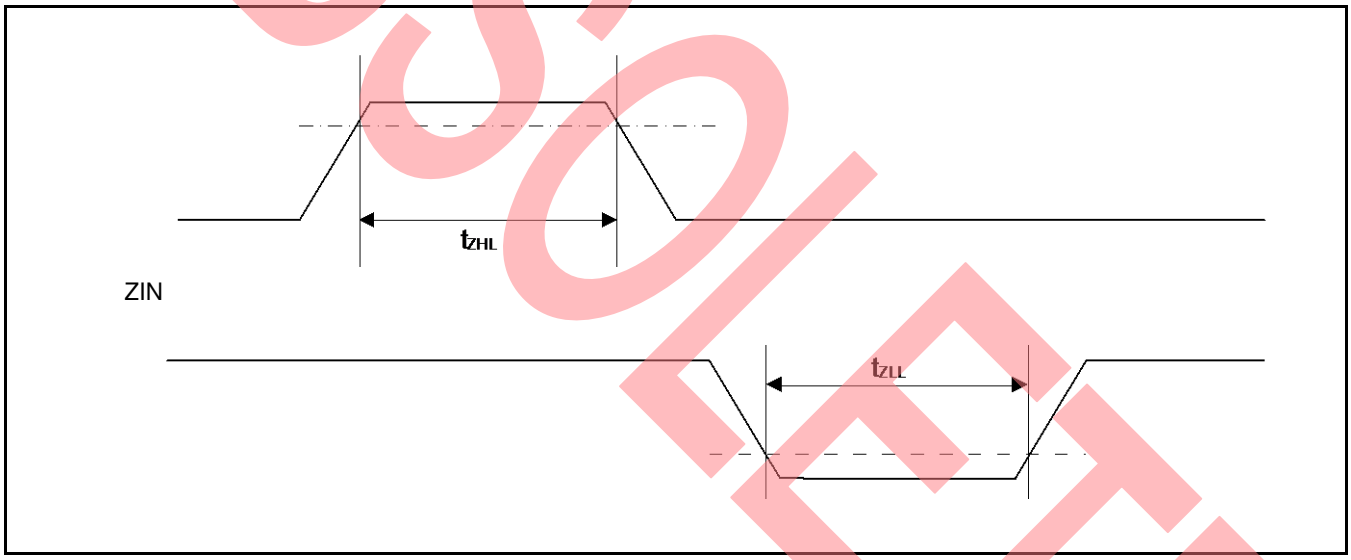
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

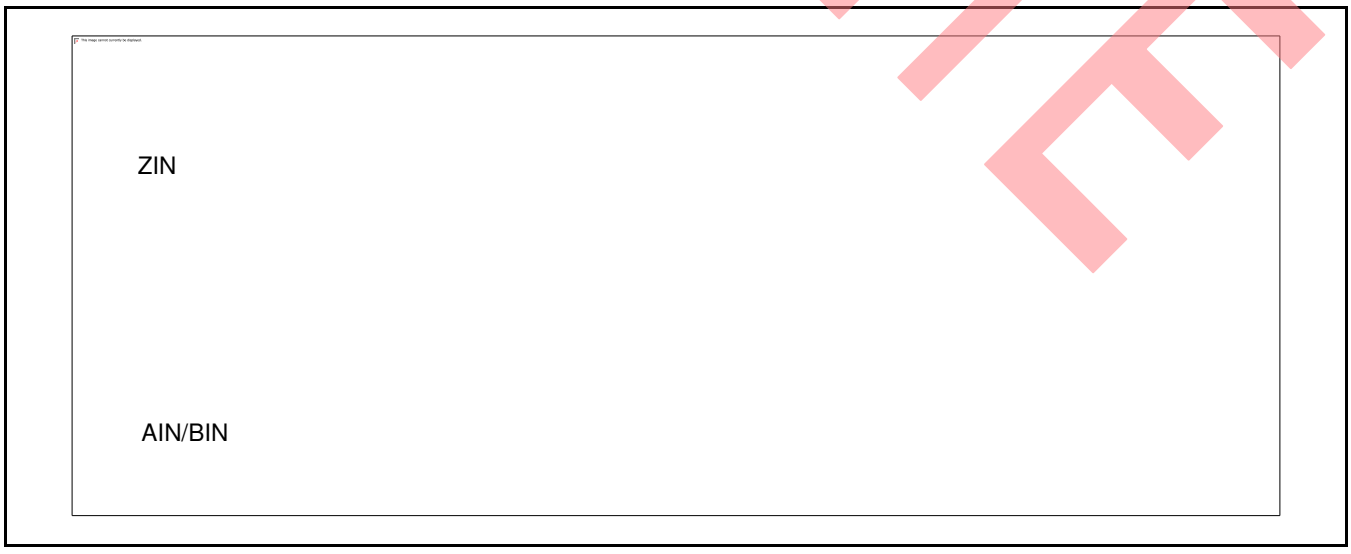
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 8. Block Diagram in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
AIN/BIN

12.4.14 I²C Timing

Standard-mode, Fast-mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP}<40 MHz	2t_{CYCP}*4	-	2t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP}<60 MHz	4t_{CYCP}*4	-	4t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP}<80 MHz	6t_{CYCP}*4	-	6t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP}<100 MHz	8t_{CYCP}*4	-	8t_{CYCP}*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	10t_{CYCP}*4	-	10t_{CYCP}*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	12t_{CYCP}*4	-	12t_{CYCP}*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	14t_{CYCP}*4	-	14t_{CYCP}*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	16t_{CYCP}*4	-	16t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I²C is connected, see 8.Block Diagram in this data sheet.
When using Standard-mode, the peripheral bus clock must be set more than 2 MHz.
When using Fast-mode, the peripheral bus clock must be set more than 8 MHz.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

Fast Mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	1000	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		0.26	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP}<80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP}<100 MHz	8 t_{CYCP}*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	10 t_{CYCP}*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	12 t_{CYCP}*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	14 t_{CYCP}*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	16 t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

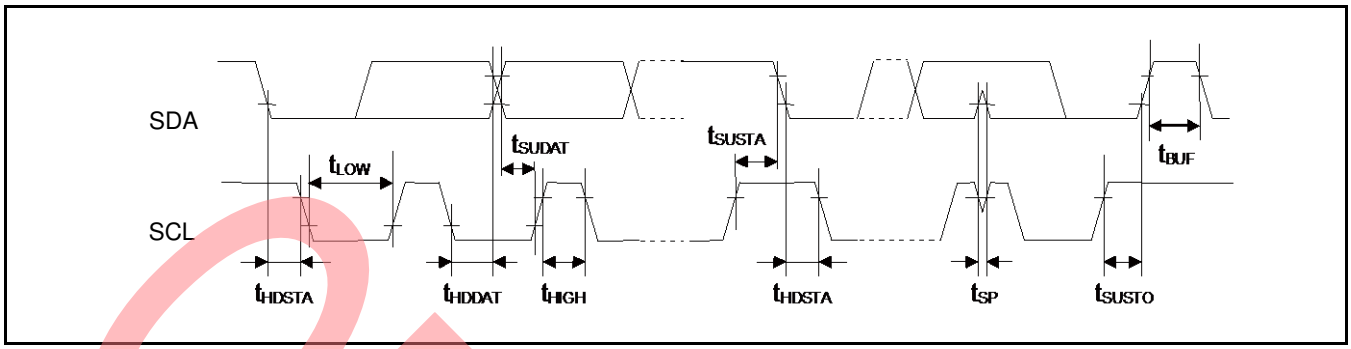
2: The maximum t_{HDDAT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 8.Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (MN709-00001) for the details.


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

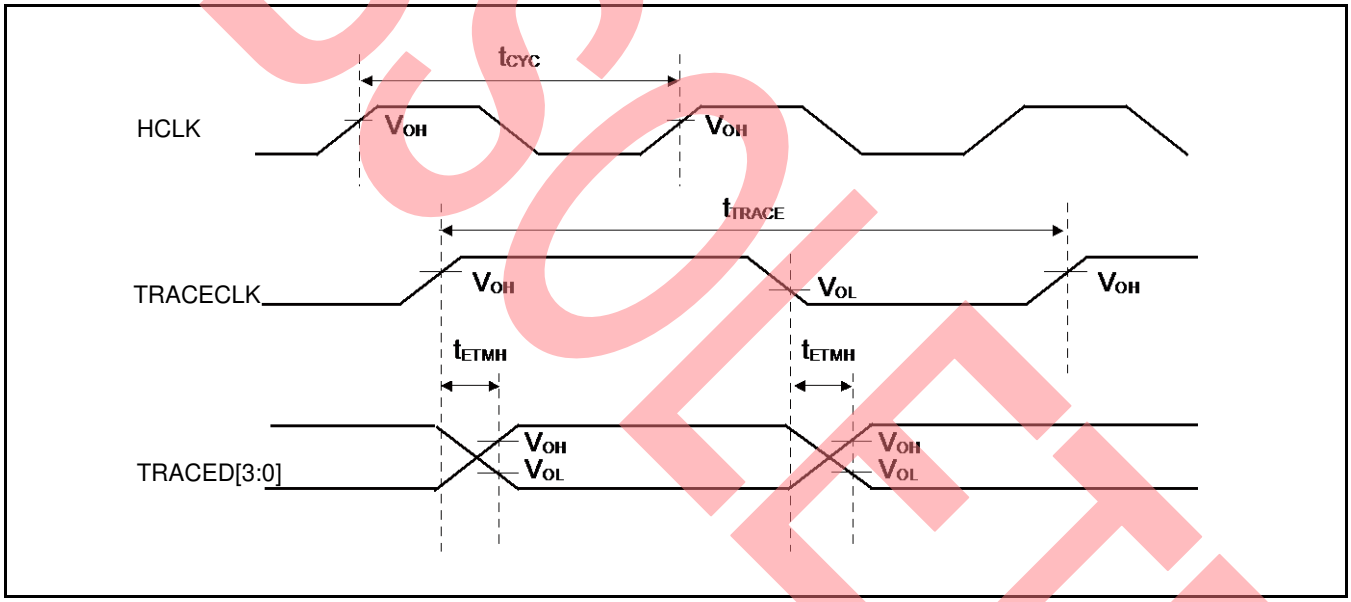
12.4.15 ETM Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	$V_{CC} \geq 4.5$ V	2	9	ns	
			$V_{CC} < 4.5$ V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5$ V	-	50	MHz	
			$V_{CC} < 4.5$ V	-	32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5$ V	20	-	ns	
			$V_{CC} < 4.5$ V	31.25	-	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*



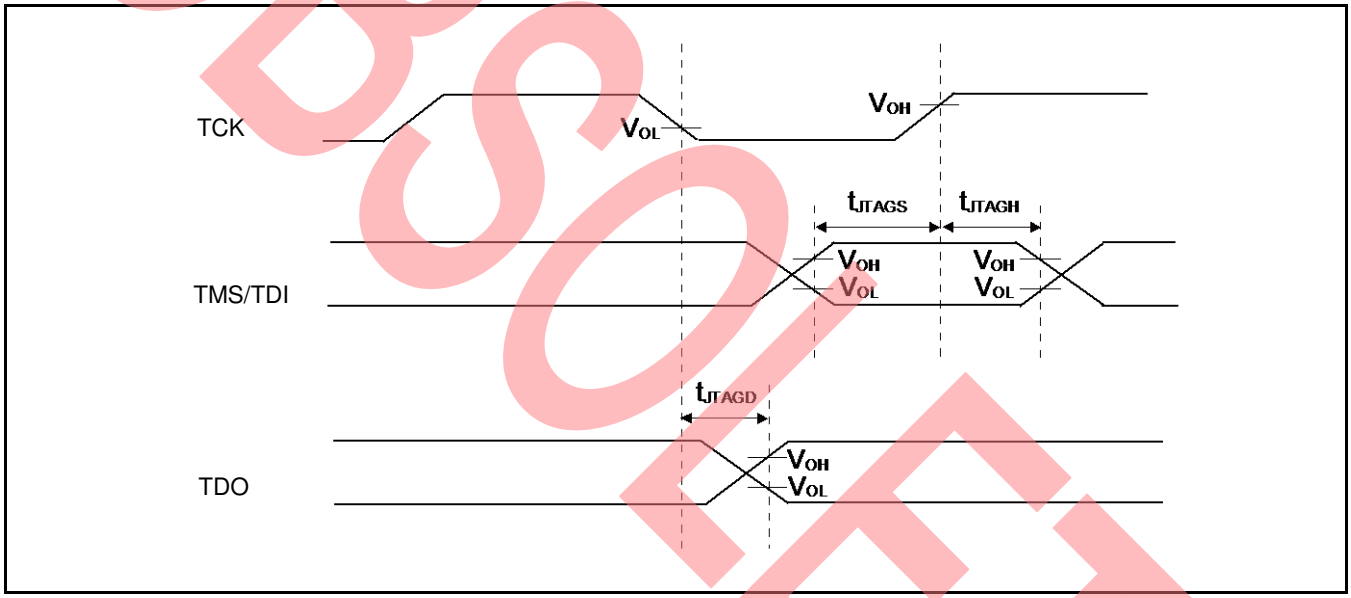
12.4.16 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L= 30 pF.*



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

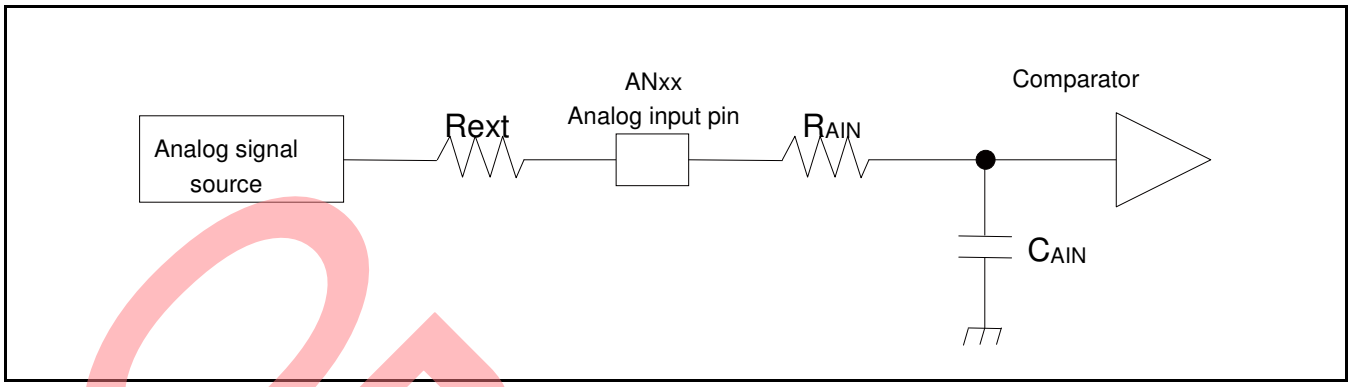
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	-	±4.5	LSB	AVRH = 2.7 V to 5.5 V Offset calibration when used
Differential Nonlinearity	-	-	-	-	±2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	±2	±7	LSB	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH±2	AVRH±7	LSB	
Total error	-	-	-	±3	±8	LSB	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1unit operation
			-	1.0	18	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1unit operation AVRH=5.5 V
				0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The condition of the minimum conversion time is when the value of sampling time: 150 ns, the value of compare time: 350 ns (AV_{CC} ≥ 4.5 V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}). For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog macro part(MN709-00001). The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V < AV_{CC} < 5.5 V

Input resistance of A/D = 1.8 kΩ at 2.7 V < AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 12.05 pF at 2.7 V < AV_{CC} < 5.5 V

Rext: Output impedance of external circuit

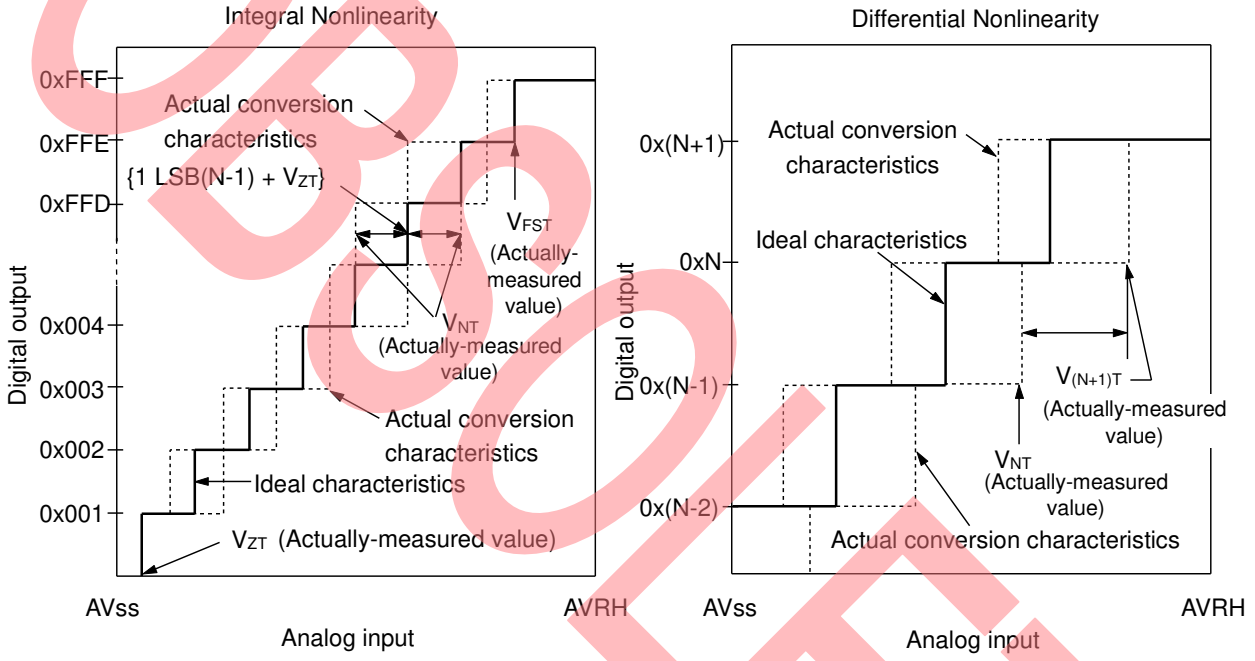
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

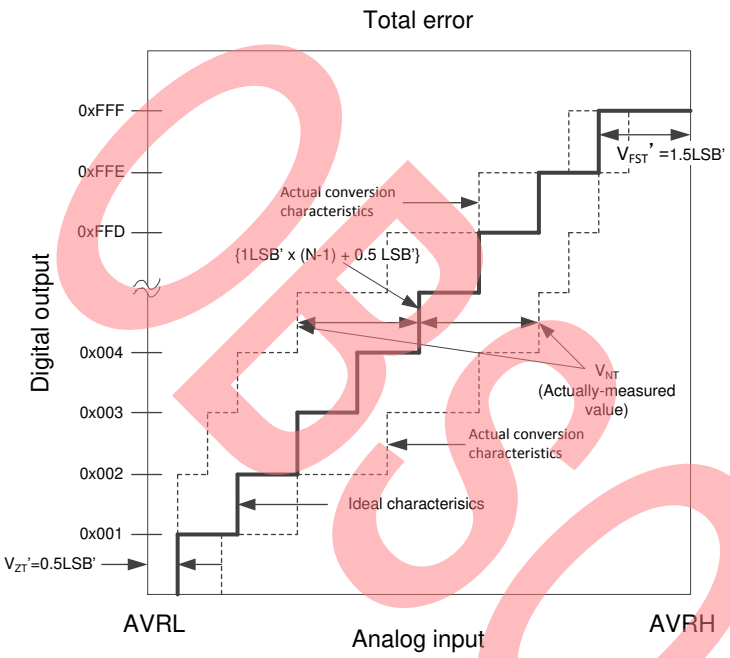
N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

■ Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'}\ [LSB]$$

$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{4096}\ [V]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}' : A voltage for causing transition of digital output from (N-1) to N

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7Vto5.5V, VS_S = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20 pF
	tc100		2.79	3.42	4.06	µs	Load 100 pF
Integral Nonlinearity*	INL		- 16	-	+ 16	LSB	
Differential Nonlinearity*	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC}=3.3 V
			400	510	620	µA	D/A 1unit operation AV_{CC}=5.0 V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8 MainFlash Memory Write/Erase Characteristics

(VCC = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time	Write cycles < 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	13.6	68	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.9 WorkFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	-	20	200	µs	Not including system-level overhead time
Chip erase time	-	1.2	6	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write cycles (cycle)	Data hold time (year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.10Standby Recovery Time

12.10.1 Recovery Cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

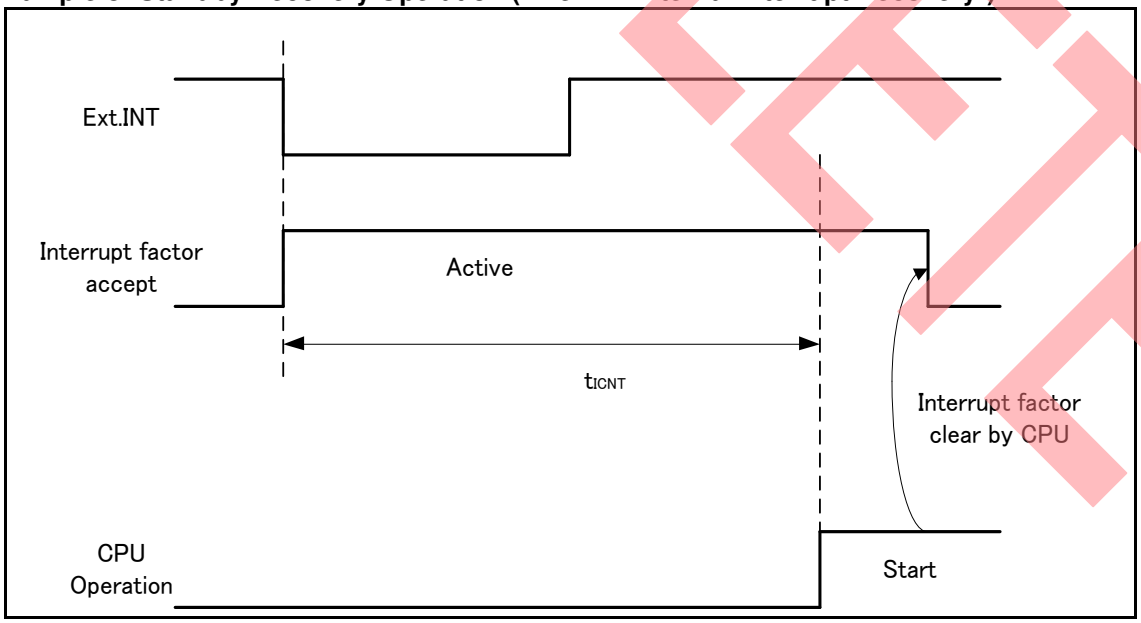
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode stop mode (Low-speed CR/sub run mode return)		270	540		
Deep standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep standby stop mode with RAM retention		365	667	µs	with RAM retention

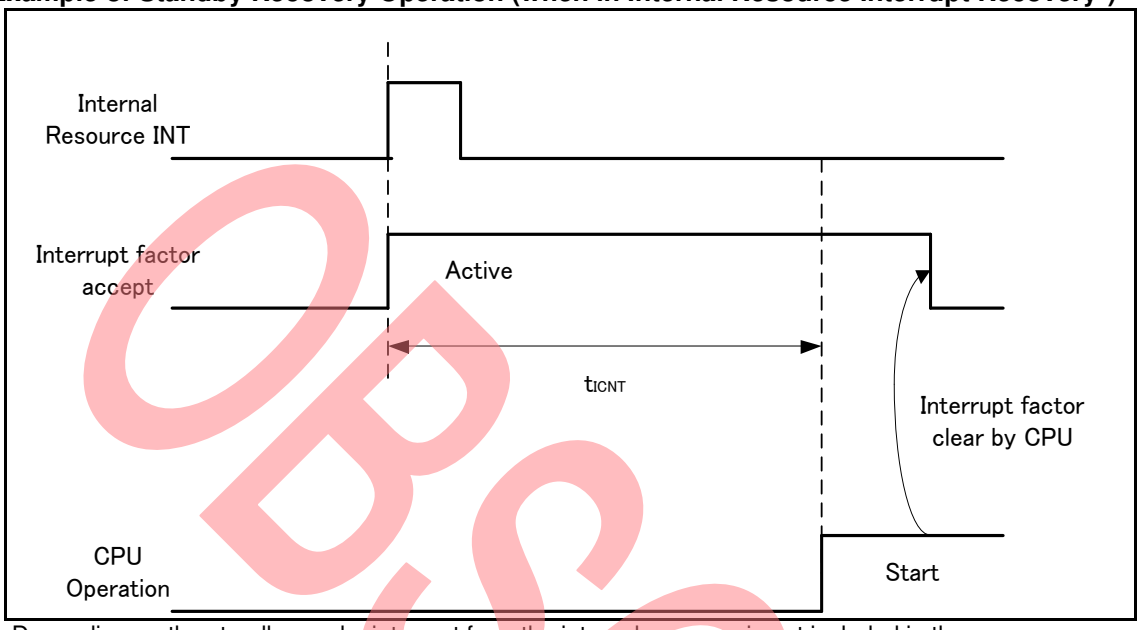
*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)



*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part(MN709-00001).
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in"FM4 Family Peripheral Manual Main part(MN709-00001).*

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

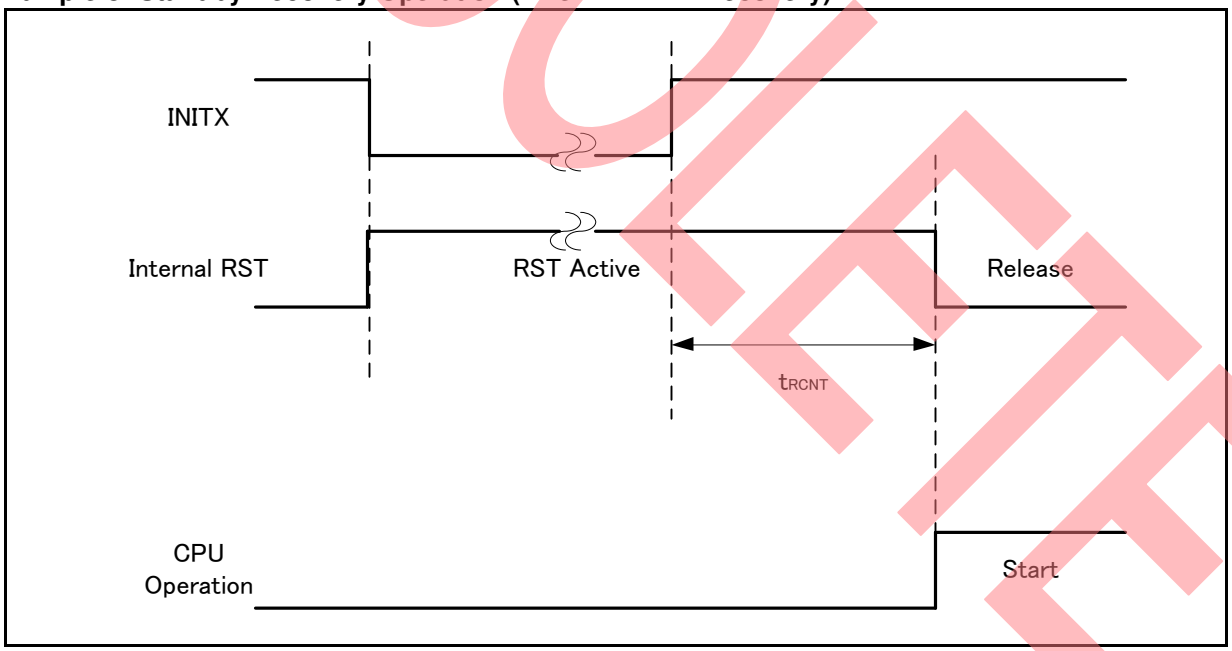
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

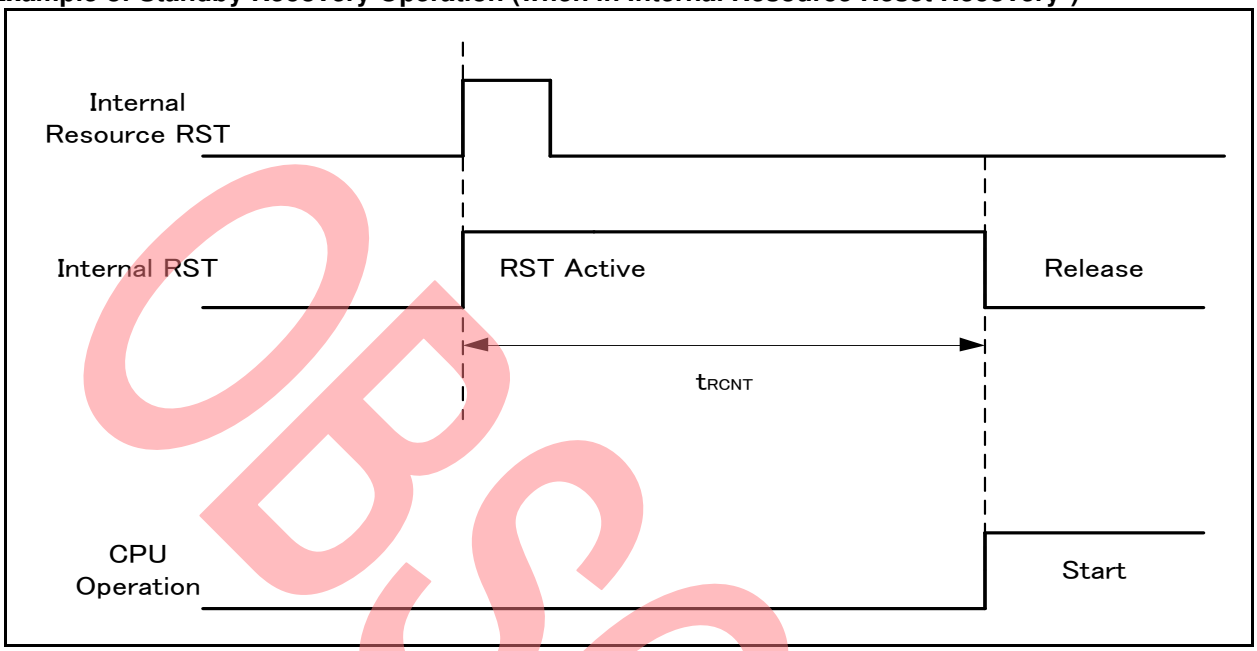
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR timer mode Main timer mode PLL timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep standby stop mode with RAM retention				µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part(MN709-00001).*
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See (6) Power-on Reset Timing in 12.4 AC Characteristics in 12. Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

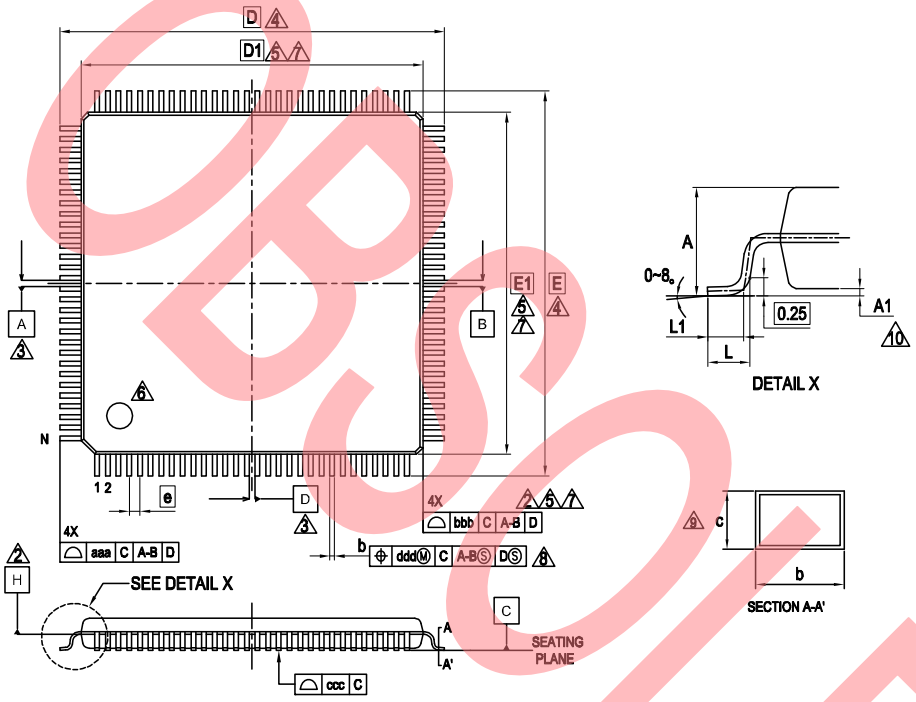
13. Ordering Information

Part Number	Package
S6E2H16G0A GV20000	Plastic LQFP (0.5-mm pitch), 120 pin (LQM120)
S6E2H14G0A GV20000	
S6E2H16F0A GV20000	Plastic LQFP (0.5-mm pitch), 100 pin (LQI100)
S6E2H14F0A GV20000	
S6E2H16E0A GV20000	Plastic LQFP (0.5-mm pitch), 80 pin (LQH080)
S6E2H14E0A GV20000	
S6E2H16G0A GB30000	Plastic FBGA (0.5-mm pitch), 121 pin (FDI121)
S6E2H14G0A GB30000	

14. Package Dimensions

Package Type	Package Code
LQFP 120	LQM120

LQM120 , 120 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQM120		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.50 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	120		

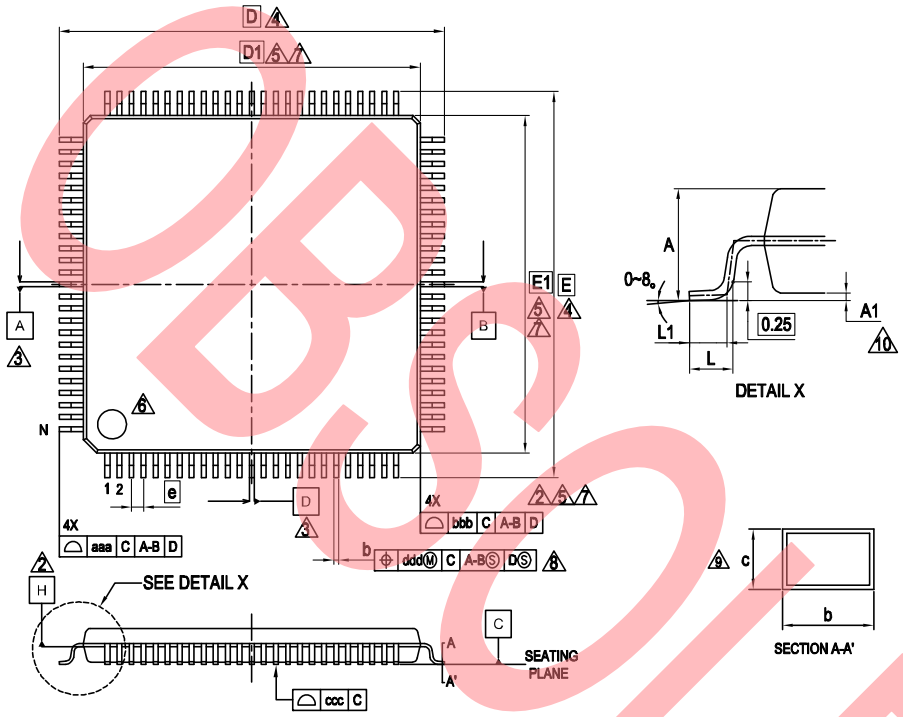
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
LQFP 100	LQI100

LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	100		

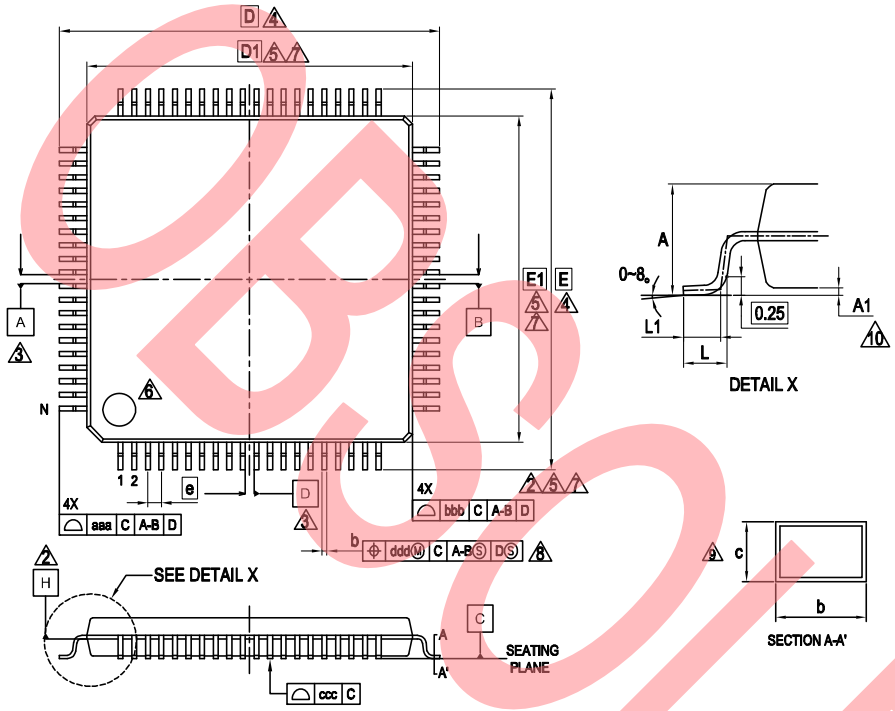
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
LQFP 80	LQH080

LQH080 , 80 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQH080		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	0.20	0.25
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	80		

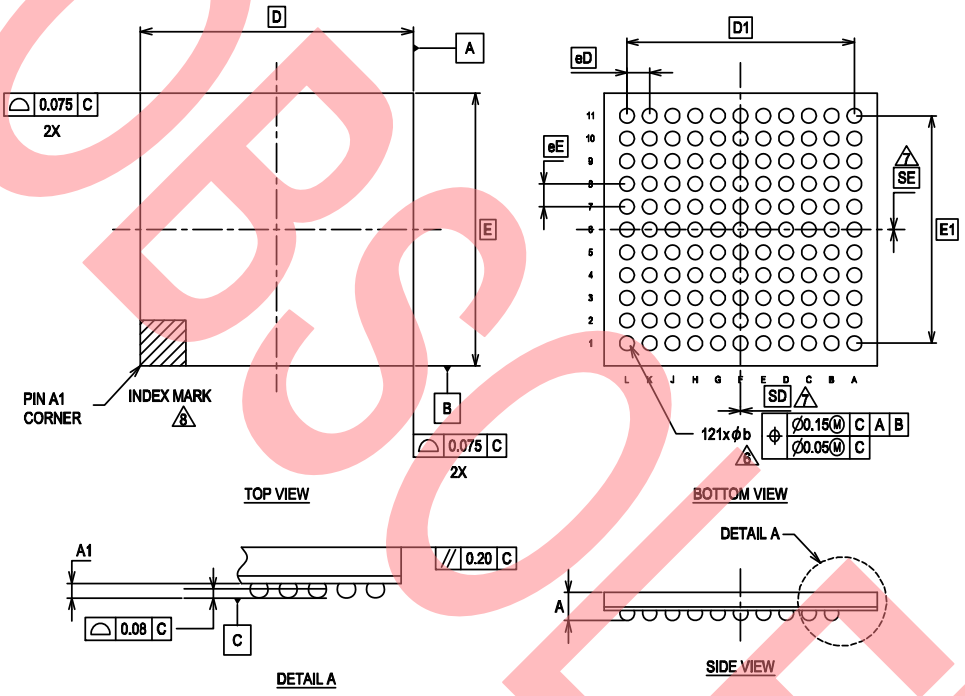
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Package Type	Package Code
FBGA 121	FDI121

FDI121 121 ball Low Profile Fine Pitch Ball Grid Array Package



PACKAGE	FDI121			NOTE
SYMBOL	MIN.	NOM.	MAX.	
A	—	—	1.20	PROFILE
A_1	0.20	—	—	TERMINAL HEIGHT
D		6.00 BSC.		BODY SIZE
E		6.00 BSC.		BODY SIZE
D_1		5.00 BSC.		MATRIX FOOTPRINT
E_1		5.00 BSC.		MATRIX FOOTPRINT
MD		11		MATRIX SIZE D DIRECTION
ME		11		MATRIX SIZE E DIRECTION
n		121		BALL COUNT
Φb	0.27	0.32	0.37	BALL DIAMETER
eD		0.50 BSC.		BALL PITCH
eE		0.50 BSC.		BALL PITCH
SD / SE		0.00		SOLDER BALL PLACEMENT

1. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE=0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE=e/
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0B

Document History

Document Title: S6E2H1 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 001-98940

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4869576	YUIA	08/18/2015	New Spec.
*A	4932844	YUIA	10/02/2015	Changed status from Preliminary to Final. Updated 12.2 Recommended Operating Conditions: Added the “Smoothing capacitor (C_S)”. Added the “Current Value” in “Maximum leak current at operating”. Updated 12.3.1 Current Rating: Updated Table 12-1 ~ 12-9: Added the “MAX” value. Updated Table 12-11: Added voltage and temperature information. Updated 12.10.1 Recovery Cause: Interrupt/WKUP: Updated Recovery Count Time. Updated 12.10.2 Recovery Cause: Reset: Updated Recovery Count Time.
*B	5027946	YUIA	11/26/2015	Updated 2 Packages: Changed FBGA to“Supported” from “Under development”. Updated 4 Pin Description: Added “Note” about TAP pins. Updated 12.5 12-bit A/D Converter: Updated “Zero transition” and “Full-scale transition” value. Added “Total error”.
*C	5748731	MBGR	05/24/2017	Making datasheet obsolete. Combined with specification 001-98943

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