User's Guide

TPS8213x Power Module Evaluation Module User's Guide

ABSTRACT

The PWR720 evaluation module (EVM) facilitates the evaluation of the TPS82130/40/50 MicroSiP™ power modules. The device outputs a 1.8-V output voltage at up to 3-A of output current from input voltages between 3 V and 17 V.

Table of Contents

List of Figures

List of Tables

1 Introduction

The TPS82130 is a 3-A, synchronous, step-down module in a 2.8- × 3.0- × 1.53-mm package. The inductor and IC are included in the device. The TPS82140 and TPS82150 are pin-to-pin compatible power modules supporting lower output currents. See Table 1-1 for a summary of the PWR720 EVMs.

Table 1-1. PWR720 EVM Options

Orderable EVM Number	IC Part Number	Maximum Output Current
TPS82130EVM-720 (PWR720-001)	TPS82130	3000 mA
TPS82140EVM-720 (PWR720-002)	TPS82140	2000 mA
TPS82150EVM-720 (PWR720-003)	TPS82150	1000 mA

1.1 Performance Specification

Table 1-2 provides a summary of the PWR720 EVM performance specifications.

Table 1-2. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input Voltage		3		17	V
Output Voltage Setpoint			1.8		V
Output Current	TPS82130EVM-720	0		3000	mA
Output Current	TPS82140EVM-720	0		2000	mA
Output Current	TPS82150EVM-720	0		1000	mA

1.2 Thermal Data

Table 1-3 shows the PWR720 EVM thermal data after considering the printed-circuit board (PCB) design of real applications. Compared to the JEDEC values listed in the data sheet, the PWR720 EVM design uses thicker copper on the 2 internal layers, has bigger planes connecting to the IC, and uses a thinner PCB. These improve the thermal performance. But the PCB is smaller than the standard JEDEC PCB, and this decreases the thermal performance. Overall, these differences improve the thermal performance and more closely match a real end application.

Table 1-3. PWR720 EVM Thermal Data

Thermal Metric(1)		TPS821x0EVM-720	TPS821x0 Data Sheet (JEDEC 51-5)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.1	58.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	9.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.9	
ψ_{JB}	Junction-to-board characterization parameter	14.0	14.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.3	21.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

1.3 Modifications

The PCB for this EVM is designed to accommodate some modifications by the user. Additional input and output capacitors can be added.

1.3.1 Input and Output Capacitors

C5 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.

C6, C7, and C8 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response. The total output capacitance must remain within the recommended range in the data sheet for proper operation.

2 Setup

This section describes how to properly use the PWR720 EVM.

2.1 Input/Output Connector Descriptions

J1 – VIN	Positive input connection from the input supply for the EVM
J2 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J3 – GND	Return connection from the input supply for the EVM
J4 – VOUT	Output voltage connection
J5 – S+/S-	Output voltage sense connections. Measure the output voltage at this point.
J6 – GND	Output return connection
J7 – PG/GND	The PG output appears on pin 1 of this header with a convenient ground on pin 2.
J8 – SS/TR & GND	The SS/TR input appears on pin 1 of this header with a convenient ground on pin 2.
JP1 – EN	EN pin input jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.
JP2 – PG Pullup Voltage	PG pin pullup voltage jumper. Place the supplied jumper on JP2 to connect the PG pin pullup resistor to Vout. Alternatively, the jumper can be removed and a different voltage can be supplied on pin 2 to pull up the PG pin to a different level. This externally applied voltage should remain below 6 V.

2.2 Setup

To operate the EVM, set jumpers JP1 and JP2 to the desired position per Section 2.1. Connect the input supply to J1 and J3 and connect the load to J4 and J6.

3 PWR720 EVM Test Results

The PWR720 EVM was used to take all the data in the TPS821x0 data sheet (SLVSCY5, SLVSDN3, or SLVSDN4). See the device data sheet for the performance of this EVM.

WARNING

Hot surface. Contact may cause burns. Do not touch!

4 Board Layout

This section provides the PWR720 EVM board layout and illustrations in Figure 4-1 through Figure 4-6. The Gerbers are available on the EVM product page: TPS82130EVM-720, TPS82140EVM-720, or TPS82150EVM-720. Rev B of the PCB just corrected typographical errors in the A version.

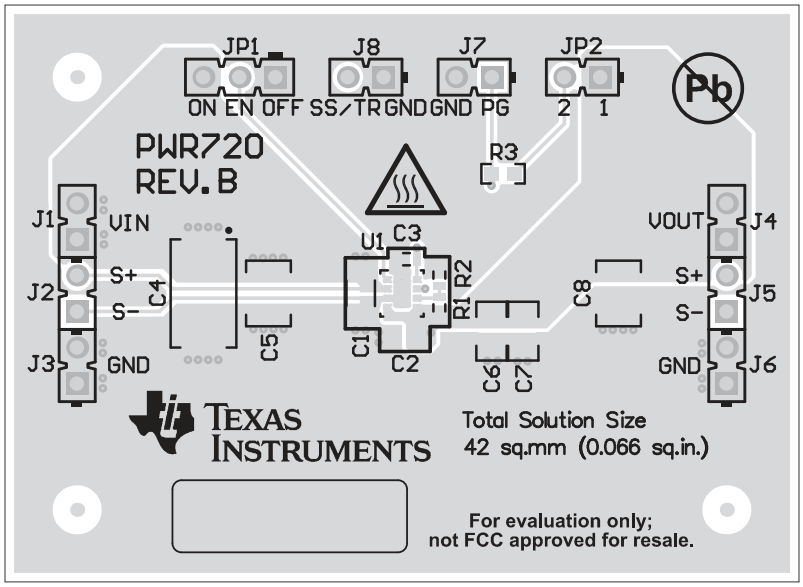

Figure 4-1. Top Assembly

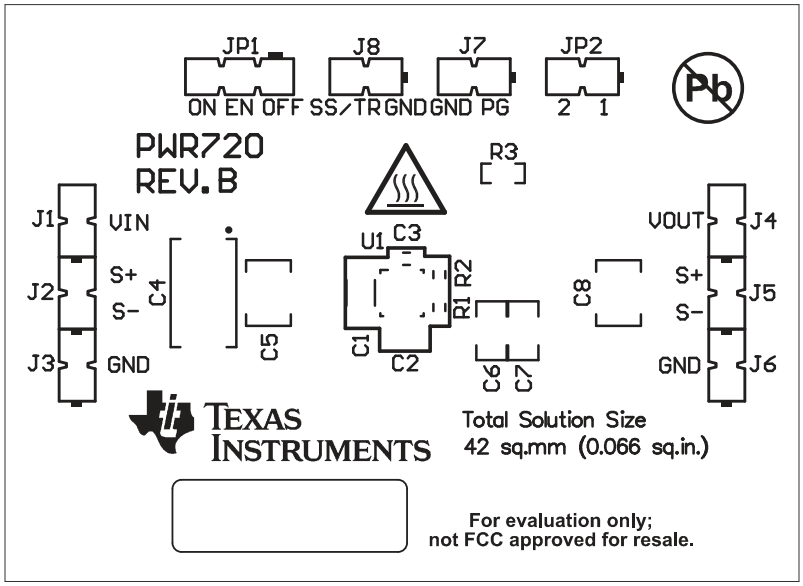

Figure 4-2. Top Overlay

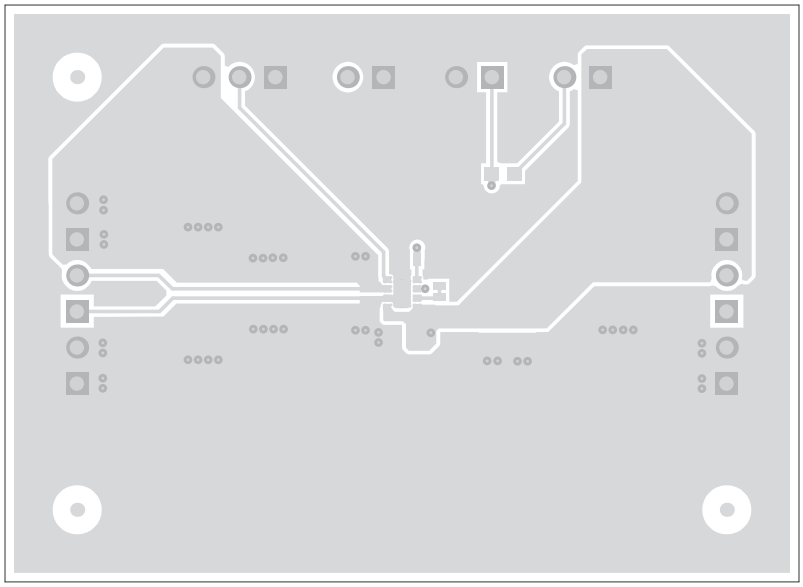

Figure 4-3. Top Layer

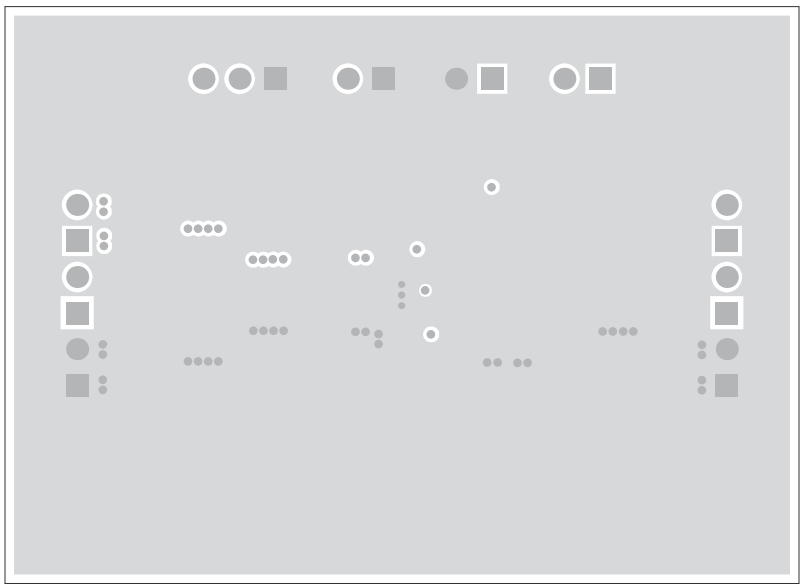

Figure 4-4. Internal Layer 1

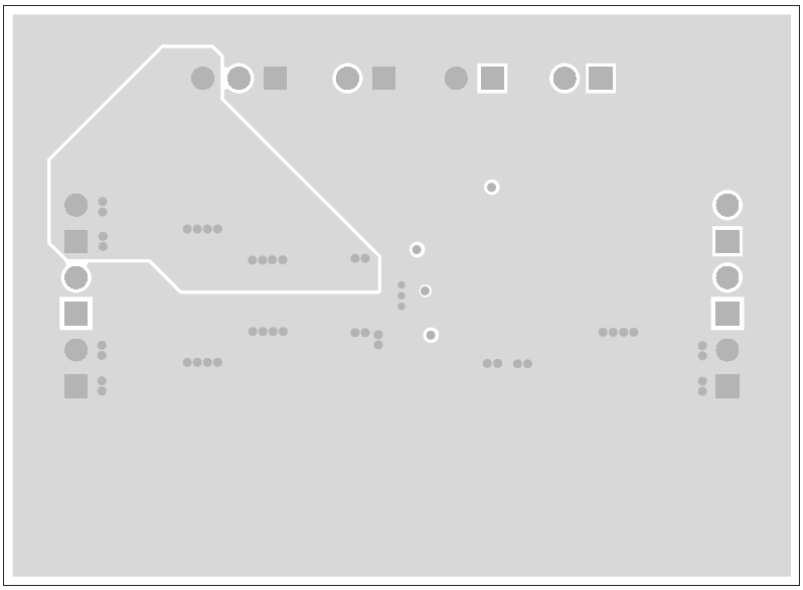

Figure 4-5. Internal Layer 2

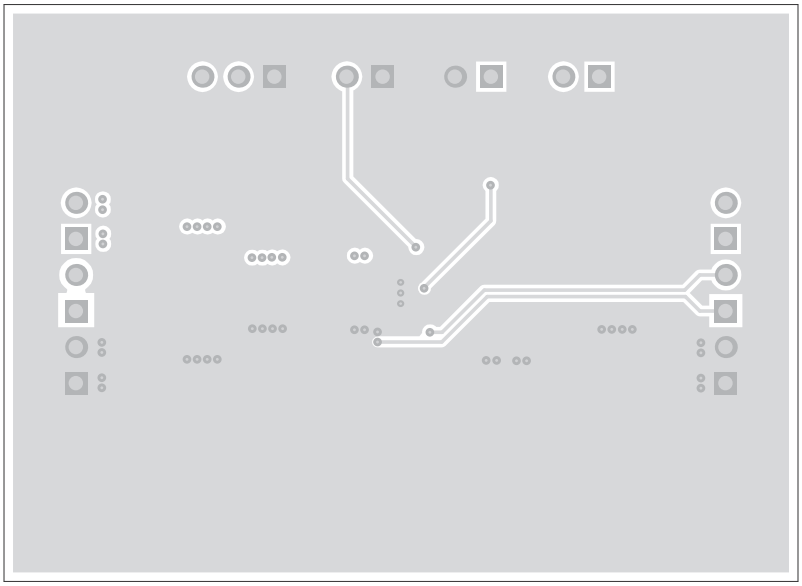

Figure 4-6. Bottom Layer

5 Schematic and Bill of Materials

This section provides the PWR720 EVM schematic and bill of materials (BOM).

5.1 Schematic

Figure 5-1 illustrates the EVM schematic.

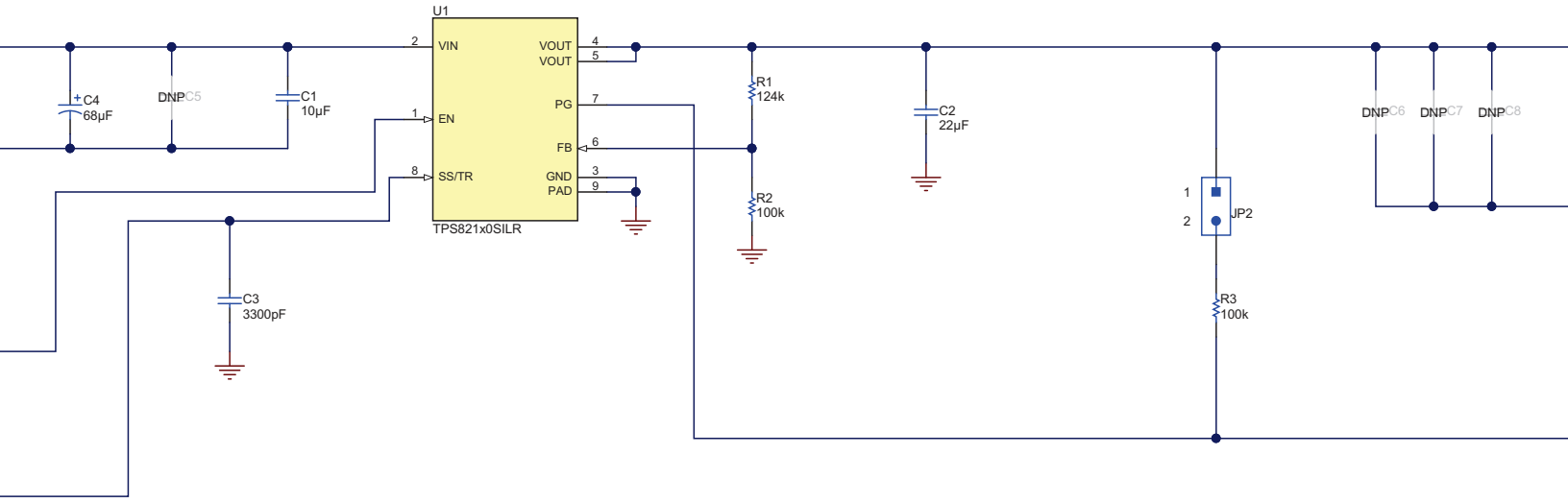

Figure 5-1. PWR720 EVM Schematic

5.2 Bill of Materials

Table 5-1 lists the BOM for this EVM.

Table 5-1. PWR720 EVM Bill of Materials

Count								
-001	-002	-003	Ref Des	Value	Description	Size	Part Number	Manufacturer
1	1	1	C1	10 µF	CAP, CERM, 10 µF, 25 V, +/- 20%, X7R	1206	C3216X7R1E106M160AE	TDK
1	1	1	C2	22 µF	CAP, CERM, 22 µF, 10 V, +/- 20%, X7S	0805	C2012X7S1A226M125AC	TDK
1	1	1	C3	3300 pF	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	Std	Std
1	1	1	C4	68 µF	CAP, TA, 68 µF, 25 V, +/- 20%, 0.125 ohm, SMD	7343-43	TPSE686M025R0125	AVX
1	1	1	R1	124 k	RES, 124 k, 1%, 0.1 W, 0603	0603	Std	Std
2	2	2	R2, R3	100 k	RES, 100 k, 1%, 0.1 W, 0603	0603	Std	Std
1	0	0	U1	TPS82130	3A, High Efficiency Step Down MicroSiP Module with Integrated Inductor	3 x 2.8 mm	TPS82130SIL	Texas Instruments
0	1	0	U1	TPS82140	2A, High Efficiency Step Down MicroSiP Module with Integrated Inductor	3 x 2.8 mm	TPS82140SIL	Texas Instruments
0	0	1	U1	TPS82150	1A, High Efficiency Step Down MicroSiP Module with Integrated Inductor	3 x 2.8 mm	TPS82150SIL	Texas Instruments

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2017) to Revision C (May 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.....2
- Updated user's guide title..... 2

Changes from Revision A (June 2016) to Revision B (May 2017) **Page**

- EVM user's guide revision B supports the addition of TPS82140EVM-720 and TPS82150EVM-720.....1
- Added *PWR720 EVM Options* table.....2
- Changed *Performance Specification Summary* table to include TPS82140EVM-720 and TPS82150EVM-720. 3
- Changed schematic to a generic device name - TPS821x0SILR, from TPS82130SILR.....8
- Changed *PWR720 EVM Bill of Materials* table to include TPS82140EVM-720 and TPS82150EVM-720..... 8

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