1.5-W CONSTANT OUTPUT POWER CLASS-D AUDIO AMPLIFIER WITH INTEGRATED BOOST CONVERTER

FEATURES

- **High Efficiency Integrated Boost Converter (Over 90% Efficiency)**
- **1.5-W into an 8-Ω Load from a 3.6-V Supply**
- **Operates from 2.5 V to 5.5 V**
- **Efficient Class-D Prolongs Battery Life**
- **Independent Shutdown for Boost Converter and Class-D Amplifier**
- **Differential Inputs Reduce RF Common Noise**
- **Built-in INPUT Low Pass Filter Decreases RF and Out of Band Noise Sensitivity**
- **Synchronized Boost and Class-D Eliminates Beat Frequencies**
- **Thermal and Short-Circuit Protection**
- **Available in 16-ball WCSP and 20-Lead QFN Packages**
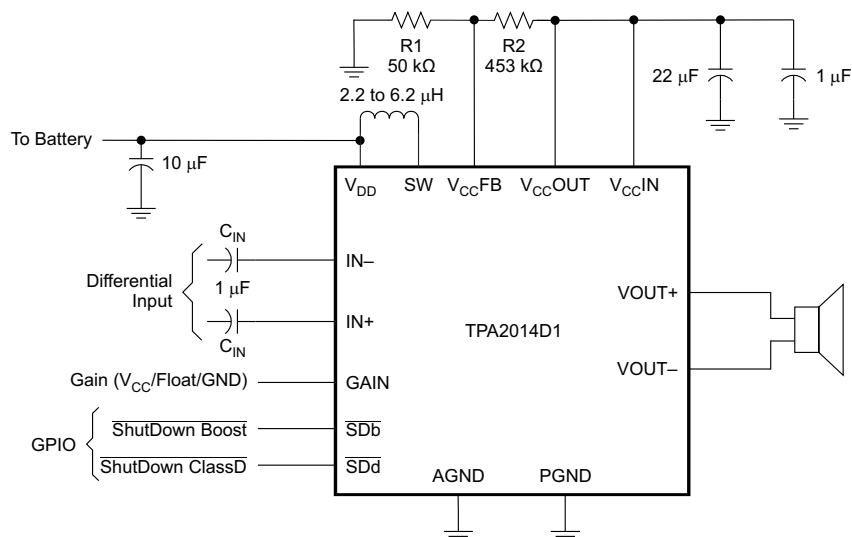- **3 Selectable Gain Settings of 2 V/V, 6 V/V, and 10 V/V**

APPLICATIONS

- **Cell Phones**
- **PDA**
- **GPS**
- **Portable Electronics**

DESCRIPTION

The TPA2014D1 is a high efficiency Class-D audio power amplifier with an integrated boost converter. It drives up to 1.5 W (10% THD+N) into a 8 Ω speaker from a 3.6 V supply. With 85% typical efficiency, the TPA2014D1 helps extend battery life when playing audio.

The built-in boost converter generates a higher voltage rail for the Class-D amplifier. This provides a louder audio output than a stand-alone amplifier connected directly to the battery. It also maintains a consistent loudness, regardless of battery voltage. Additionally, the boost converter can be used to supply external devices.

The TPA2014D1 has an integrated low pass filter to improve RF rejection and reduce out-of-band noise, increasing the signal to noise ratio (SNR). A built-in PLL synchronizes the boost converter and Class-D switching frequencies, thus eliminating beat frequencies and improving audio quality. All outputs are fully protected against shorts to ground, power supply, and output-to-output shorts.
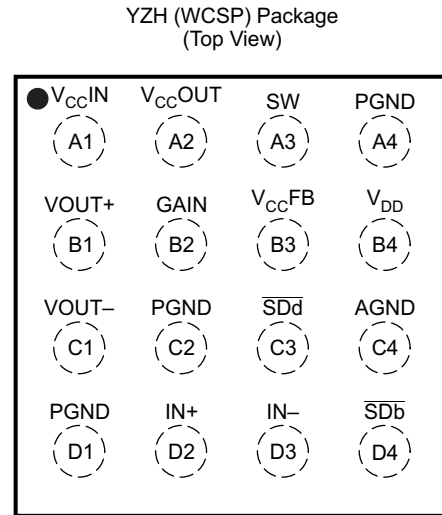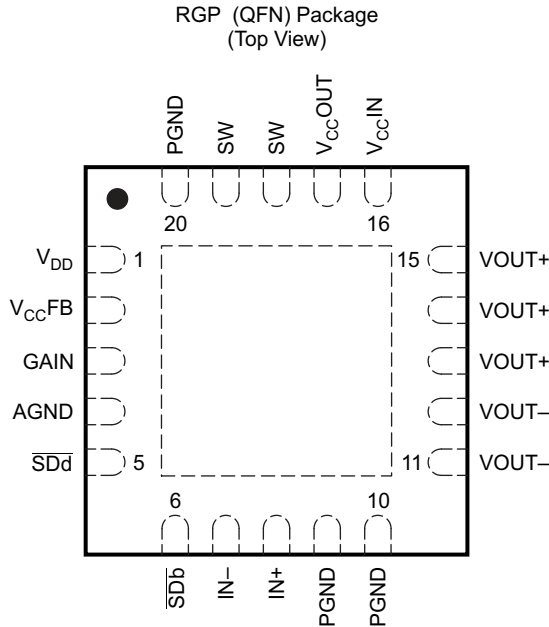
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008, Texas Instruments Incorporated

TPA2014D1

![Texas Instruments logo]

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

RGP (QFN) Package
(Top View)

YZH (WCSP) Package
(Top View)

BOOST CONVERTER TERMINAL FUNCTIONS

| TERMINAL			I/O	DESCRIPTION
NAME	QFN	WCSP		
IN+	8	D2	I	Positive audio input
IN−	7	D3	I	Negative audio input
VOUT+	13, 14, 15	B1	O	Positive audio output
VOUT−	11, 12	C1	O	Negative audio output
$\overline{SDb}$	6	D4	I	Shutdown terminal for the Boost Converter
$\overline{SDd}$	5	C3	I	Shutdown terminal for the Class D Amplifier
SW	18, 19	A3	−	Boost and rectifying switch input
$V_{CC}OUT$	17	A2	−	Boost converter output - connect to $V_{CC}IN$
GAIN	3	B2	I	Gain selection pin
$V_{CC}IN$	16	A1	−	Class-D audio power amplifier voltage supply - connect to $V_{CC}OUT$
$V_{CC}FB$	2	B3	I	Voltage feedback
V_{DD}	1	B4	−	Supply voltage
AGND	4	C4	−	Analog ground - connect all GND pins together
PGND	9, 10, 20	D1, C2, A4	−	Power ground - connect all GND pins together
Thermal Pad	Die Pad	N/A	P	Solder the thermal pad on the bottom of the QFN package to the GND plane of the PCB. It is required for mechanical stability and will enhance thermal performance.

Product Folder Link(s): *TPA2014D1*

Functional Block Diagram
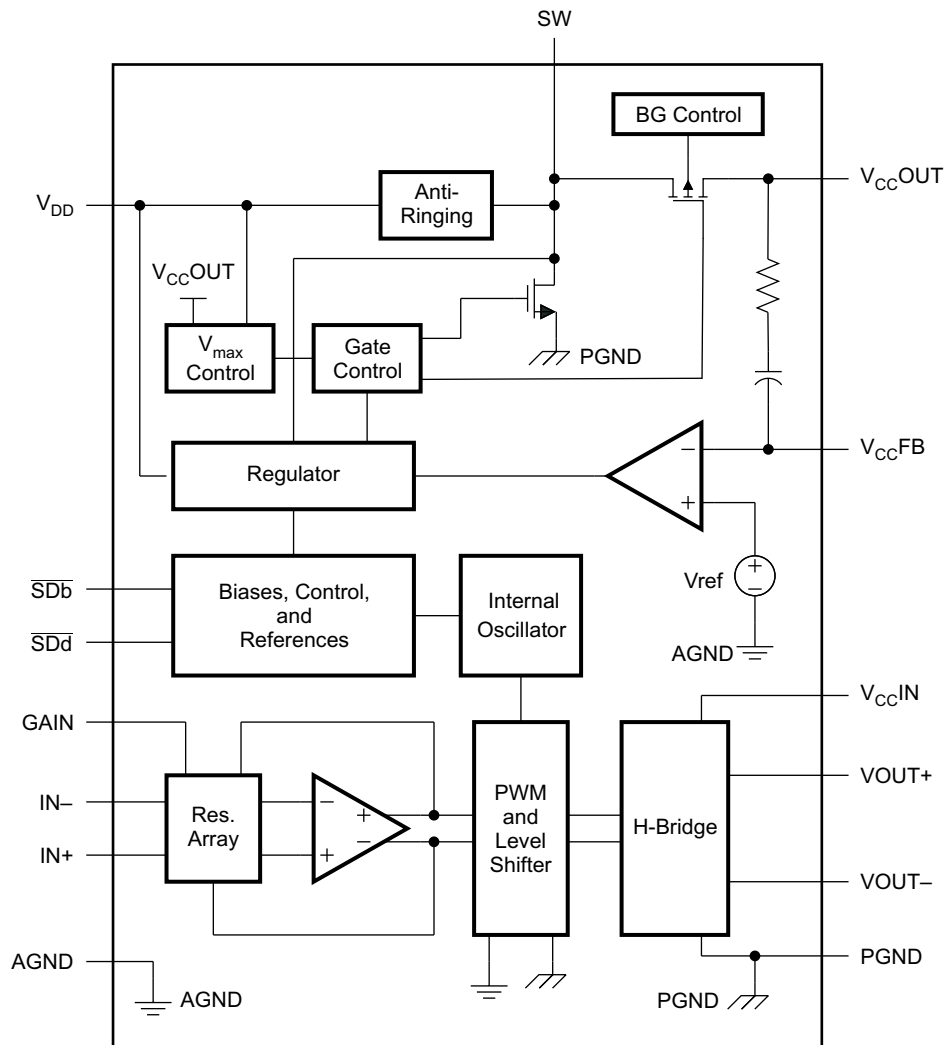
Table 1. BOOST CONVERTER MODE CONDITION

CASE	OUTPUT CURRENT	MODE OF OPERATION
$V_{DD} < V_{CC}$	Low	Continuous (fixed frequency)
$V_{DD} < V_{CC}$	High	Continuous (fixed frequency)
$V_{DD} \geq V_{CC}$	Low	Discontinuous (variable frequency)
$V_{DD} \geq V_{CC}$	High	Discontinuous (variable frequency)

Table 2. DEVICE CONFIGURATION

$\overline{SDb}$	$\overline{SDd}$	Boost Converter	Class D Amplifier	Comments
low	low	OFF	OFF	Device is in shutdown mode Iq ≤ 1 µA
low	high	OFF	ON	Boost converter is off. Class-D Audio Power Amplifier (APA) can be driven by an external pass transistor connected to the battery.
high	low	ON	OFF	Class-D APA is off. Boost Converter is on and can be used to drive an external device.
high	high	ON	ON	Boost converter and Class-D APA are on. Normal operation. Boost converter can be used to drive an external device in parallel to the Class-D APA within the limits of the boost converter output current.

TPA2014D1

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
V_{DD}	Supply voltage	–0.3 to 6	V
V_I	Input voltage, Vi: $\overline{SDb}$, $\overline{SDd}$, IN+, IN–, $V_{CC}FB$	–0.3 to V_{DD} + 0.3	V
	Continuous total power dissipation	See Dissipation Rating Table	
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	T_A ≤ 25°C	DERATING FACTOR[1]	T_A = 70°C	T_A = 85°C
16 ball WCSP	1.5 W	12.4 mW/°C	1 W	0.8 W
20 pin QFN	2.5 W	20.1 mW/°C	1.6 W	1.3 W

(1) Derating factor measured with JEDEC High K board.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES[1]	PART NUMBER	SYMBOL
–40°C TO 85°C	16-ball, 2.275 mm × 2.275 mm WCSP (+0.01/-0.09 mm tolerance)	TPA2014D1YZH	CEJ
	20-pin, 4 mm × 4 mm QFN	TPA2014D1RGP[2]	CEK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The RGP package is only available taped and reeled. To order, add suffix *R* to the end of the part number for a reel of 3000 (e.g., TPA2014D1RGPR).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.5	5.5	V
V_{IH}	High-level input voltage	$\overline{SDb}$, $\overline{SDd}$	1.3		V
V_{IL}	Low-level input voltage	$\overline{SDb}$, $\overline{SDd}$		0.35	V
$|I_{IH}|$	High-level input current	$\overline{SDb}$ = $\overline{SDd}$ = 5.8 V, V_{DD} = 5.5 V		1	µA
$|I_{IL}|$	Low-level input current	$\overline{SDb}$ = $\overline{SDd}$ = -0.3 V, V_{DD} = 5.5 V		20	µA
T_A	Operating free-air temperature		–40	85	°C

Product Folder Link(s): TPA2014D1

DC CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Class-D audio power amplifier voltage supply range, V_{CC}IN		3		5.5	V
I_{SD}	Shutdown quiescent current	$\overline{SDd} = \overline{SDb}$ = 0 V, V_{DD} = 2.5 V, R_L = 8 Ω		0.04	1.5	µA
		$\overline{SDd} = \overline{SDb}$ = 0 V, V_{DD} = 3.6 V, R_L = 8 Ω		0.04	1.5	
		$\overline{SDd} = \overline{SDb}$ = 0 V, V_{DD} = 4.5 V, R_L = 8 Ω		0.02	1.5	
		$\overline{SDd} = \overline{SDb}$ = 0.35 V, V_{DD} = 2.5 V, R_L = 8 Ω		0.03	1.5	
		$\overline{SDd} = \overline{SDb}$ = 0.35 V, V_{DD} = 3.6 V, R_L = 8 Ω		0.03	1.5	
		$\overline{SDd} = \overline{SDb}$ = 0.35 V, V_{DD} = 4.5 V, R_L = 8 Ω		0.02	1.5	
I_{DD}	Boost converter quiescent current	$\overline{SDd}$ = 0 V, $\overline{SDb}$ = 1.3 V, V_{DD} = 3.6 V, V_{CC} = 5.5 V, No Load, No Filter		1.3		mA
I_{CC}	Class D amplifier quiescent current	V_{DD} = 3.6, V_{cc} = 5.5 V, No Load, No Filter		4.3	6	mA
		V_{DD} = 4.5, V_{cc} = 5.5 V, No Load, No Filter		3.6	6	
I_{DD}	Boost converter and audio power amplifier quiescent current, Class D[1]	$\overline{SDd} = \overline{SDb}$ = 1.3V, V_{DD} = 3.6, V_{cc} = 5.5 V, No Load, No Filter		16.5	23	mA
		$\overline{SDd} = \overline{SDb}$ = 1.3V, V_{DD} = 4.5, V_{cc} = 5.5 V, No Load, No Filter		11	18.5	
f	Boost converter switching frequency		500	600	700	kHz
	Class D switching frequency		250	300	350	kHz
UVLO	Under voltage lockout				1.7	V
GAIN	Gain input low level	Gain = 2 V/V (6dB)		0	0.35	V
	Gain input mid level	Gain = 6 V/V (15.5 dB) (floating input)	0.7	0.8	1	V
	Gain input high level	Gain = 10 V/V (20 dB)	1.35			V
POR_D	Class D Power on reset ON threshold			2.8		V

(1) I_{DD} is calculated using $I_{DD} = (I_{CC} \times V_{CC})/(V_{DD} \times \eta)$, where I_{CC} is the class D amplifier quiescent current; η = 40%, which is the boost converter efficiency when class D amplifier has no load. To achieve the minimal 40% η, it is recommended to use the suggested inductors in table 4 and to follow the layout guidelines.

BOOST CONVERTER DC CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Output voltage range		3		5.5	V
V_{FB}	Feedback voltage		490	500	510	mV
I_{OL}	Output current limit, Boost_max			750		mA
R_{ON_PB}	PMOS switch resistance			220		mΩ
R_{ON_NB}	NMOS resistance			170		mΩ
	Line regulation	No Load, 1.8 V < V_{DD} < 5.2 V, V_{CC} = 5.5 V		3		mV/V
	Load regulation	V_{DD} = 3.6 V, 0 < I_L < 500 mA, V_{CC} = 5.5 V		30		mV/A
I_L	Start up current limit, Boost			$0.4 \times I_{Boost}$		mA

CLASS D AMPLIFIER DC CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMR	Input common mode range	V_{in} = ±100 mV, V_{DD} = 2.5 V, V_{CC} = 3 V, R_L = 8 Ω	0.5		2.2	V
		V_{in} = ±100 mV, V_{DD} = 2.5 V, V_{CC} = 3.6 V, R_L = 8 Ω	0.5		2.8	
		V_{in} = ±100 mV, V_{DD} = 3.6 V, V_{CC} = 5.5 V, R_L = 8 Ω	0.5		4.7	
CMRR	Input common mode rejection	R_L = 8 Ω, V_{icm} = 0.5 and V_{icm} = V_{CC} − 0.8, differential inputs shorted		−75		dB
V_{OO}	Output offset voltage Class-D	V_{CC} = 3.6 V, Av = 2 V/V, IN+ = IN− = V_{ref}, R_L = 8 Ω		1	6	mV
		V_{CC}= 3.6 V, Av = 6 V/V, IN+ = IN− = V_{ref}, R_L = 8 Ω		1	6	
		V_{CC}= 3.6 V, Av = 10 V/V, IN+ = IN− = V_{ref}, R_L = 8 Ω		1	6	
		V_{CC} = 5.5 V, Av = 2 V/V, IN+ = IN− = V_{ref}, R_L = 8 Ω		1	6	
R_{in}	Input Impedance	Gain = 2 V/V (6 dB)		32		kΩ
		Gain = 6 V/V (15.5 dB)		15		
		Gain = 10 V/V (20 dB)		9.5		
$R_{DS(on)}$	OUTP High-side FET On-state series resistance	I_{OUTx} = −300 mA; V_{CC} = 3.6 V		0.36		Ω
	OUTP Low-side FET On-state series resistance			0.36		
$R_{DS(on)}$	OUTN High-side FET On-state series resistance			0.36		
	OUTN Low-side FET On-state series resistance			0.36		
A_V	Low Gain	GAIN ≤ 0.35 V	1.8	2	2.2	V/V
	Mid Gain	GAIN = 0.8 V	5.7	6	6.3	V/V
	High Gain	GAIN ≥ 1.35 V	9.5	10	10.5	V/V

AC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.6V, R_L = 8 Ω + 33 µH, L = 6.2 µH (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{START}	Start up time	2.5 V ≤ V_{DD} ≤ 5.5 V, C_{IN} ≤ 1 µF		7.5		ms
η	Efficiency	THD+N = 1%, V_{CC} = 5 V, V_{DD} = 3.6 V, Pout = 1.2 W, C_{boost}= 47µF		85%		
		THD+N = 1%, V_{CC} = 5 V, V_{DD} = 4.2 V, Pout = 1.2 W		87.5%		
	Thermal Shutdown	Threshold		150		°C

CLASS D AMPLIFIER AC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.6V, R_L = 8 Ω + 33 μH, L = 6.2 μH, V_{CC} = 5 V, Gain = 2 V/V(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR Class-D	Output referred power supply rejection ratio	V_{DD} = 3.6 V, V_{CC} = 5, 200 mV$_{PP}$ ripple, f = 217 Hz		−91		dB
THD+N Class-D	Total harmonic distortion + noise	f = 1 kHz, P_o = 1.2 W, V_{CC} = 5 V		1%		
		f = 1 kHz, P_o = 1.5 W, V_{CC} = 5 V		10%		
		f = 1 kHz, P_o = 1 W, V_{CC} = 5 V		0.1%		
Vn Class-D	Output integrated noise floor	Av = 6 dB (2V/V)		31		μVrms
	Output integrated noise floor A-weighted	Av = 6 dB (2V/V)		23		
P_O	Maximum output power	THD+N = 10%, V_{CC} = 5 V, V_{DD} = 3.6V ,		1.5		W
		THD+N = 1%, V_{CC} = 5 V, V_{DD} = 3.6V ,		1.2		
		THD+N = 0.1%, V_{CC} = 5 V, V_{DD} = 3.6V ,		1		

TEST SET-UP FOR GRAPHS
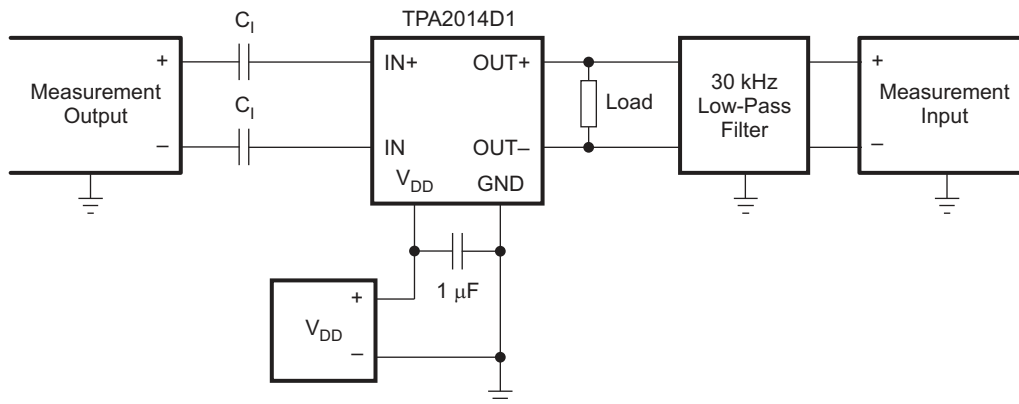
(1) C_I was shorted for any common-mode input voltage measurement. All other measurements were taken with a 1-μF C_I (unless otherwise noted).

(2) A 33-μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (1-kΩ, 4.7-nF) is used on each output for the data sheet graphs.

(4) L = 6.2 μH is used for the boost converter unless otherwise noted.
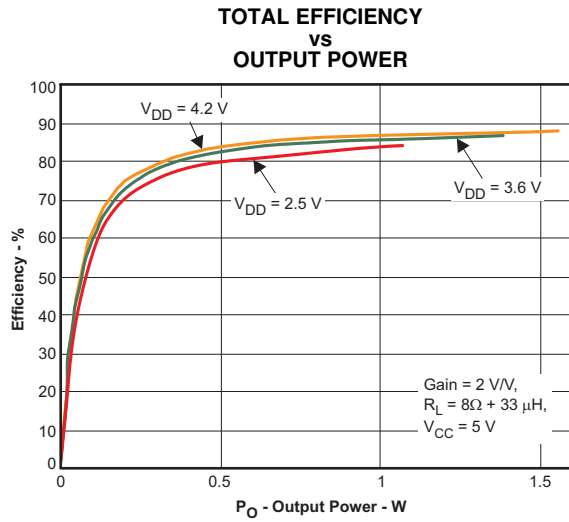
TYPICAL CHARACTERISTICS
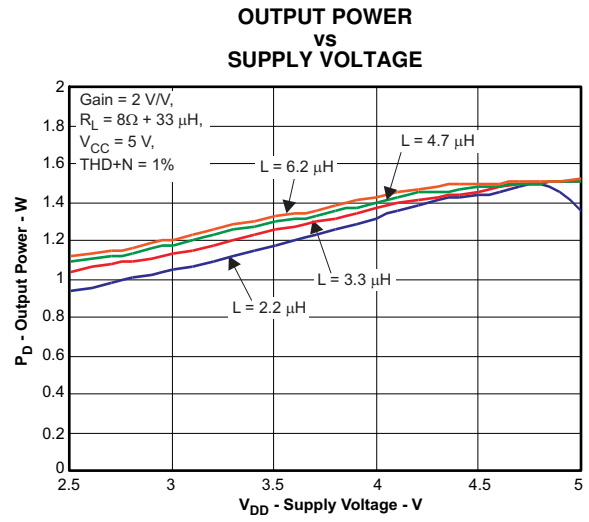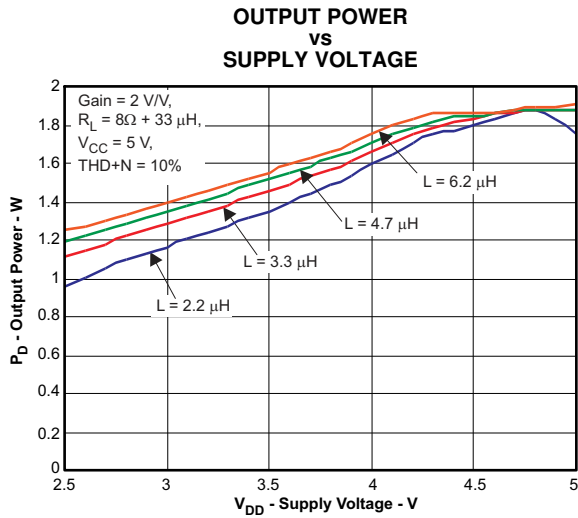
TOTAL EFFICIENCY
vs
OUTPUT POWER

Figure 1.

OUTPUT POWER
vs
SUPPLY VOLTAGE

Figure 2.

OUTPUT POWER
vs
SUPPLY VOLTAGE

Figure 3.

TOTAL POWER DISSIPATION
vs
OUTPUT POWER

Figure 4.

Product Folder Link(s): *TPA2014D1*

TYPICAL CHARACTERISTICS (continued)

TOTAL SUPPLY CURRENT
vs
OUTPUT POWER

Figure 5.

OUTPUT POWER
vs
LOAD

Figure 6.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER
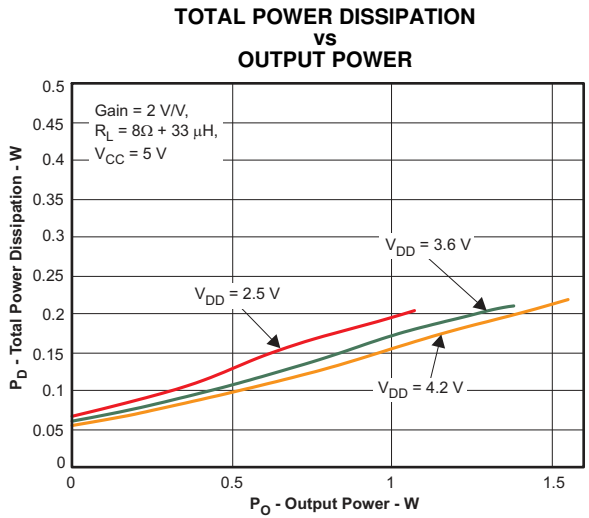
Figure 7.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY
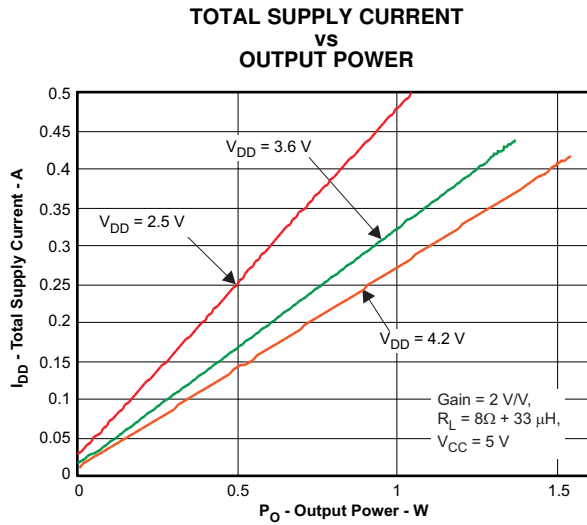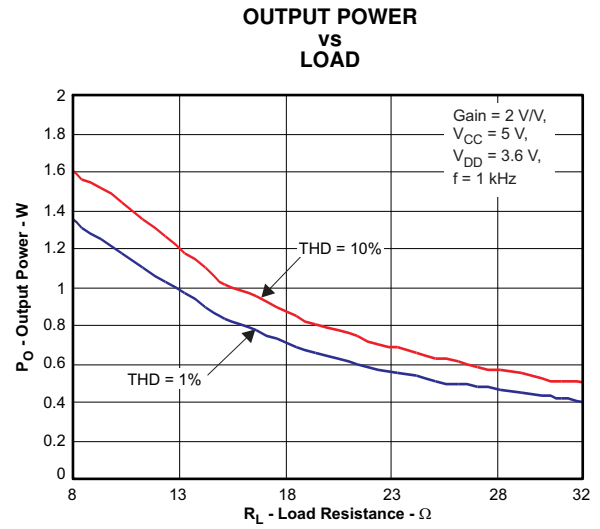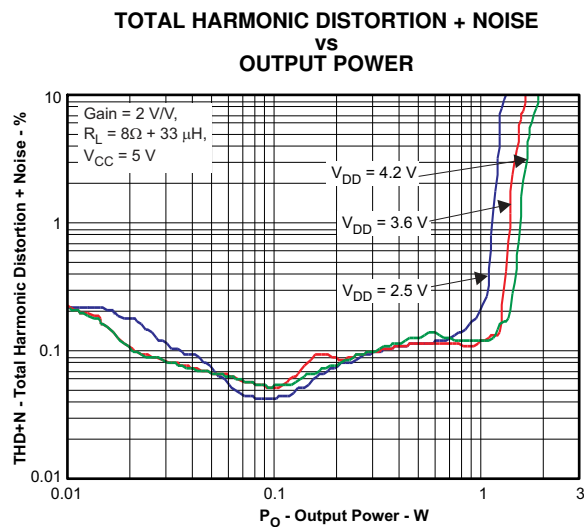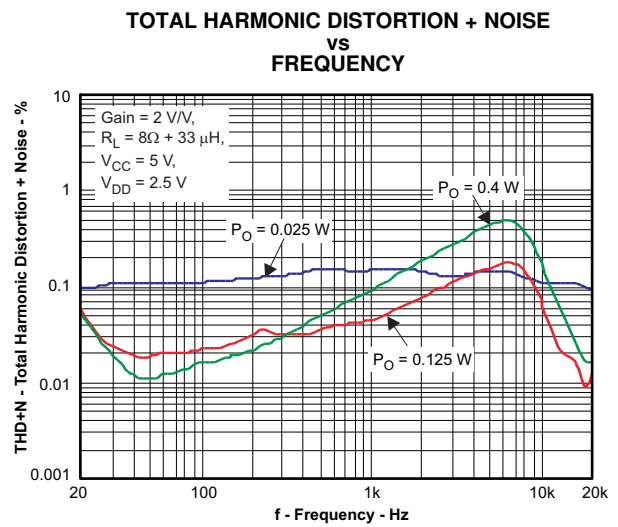
Figure 8.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY
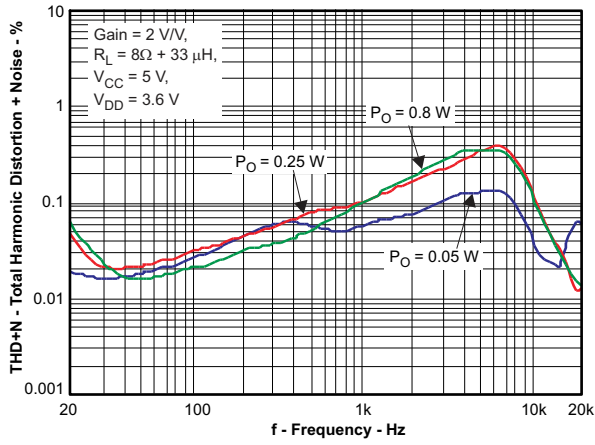
Figure 9.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY
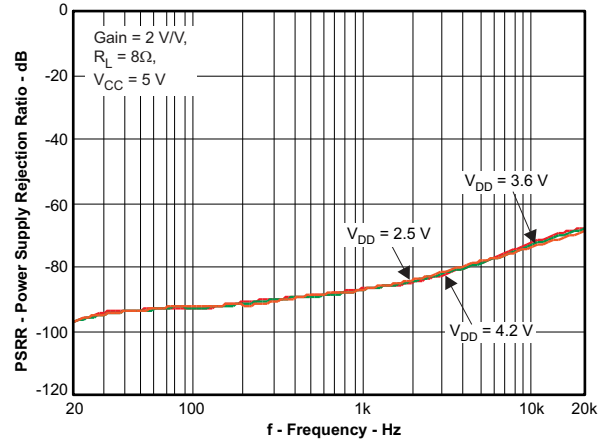
Figure 10.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY
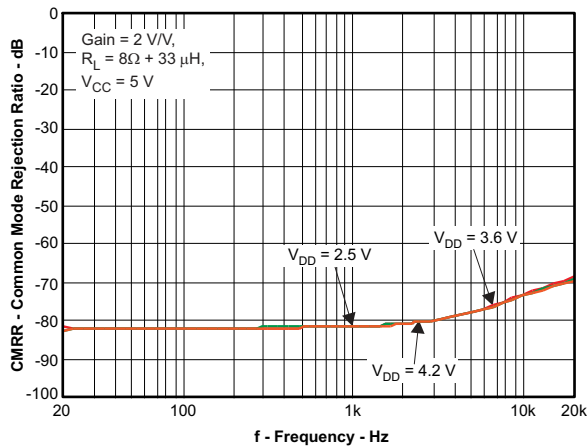
Figure 11.

BOOST EFFICIENCY
vs
OUTPUT CURRENT

Figure 12.

Product Folder Link(s): *TPA2014D1*

TYPICAL CHARACTERISTICS (continued)

**BOOST EFFICIENCY
vs
SUPPLY VOLTAGE**

Figure 13.

**MAXIMUM CONTINUOUS OUTPUT CURRENT
vs
SUPPLY VOLTAGE (BOOST)**
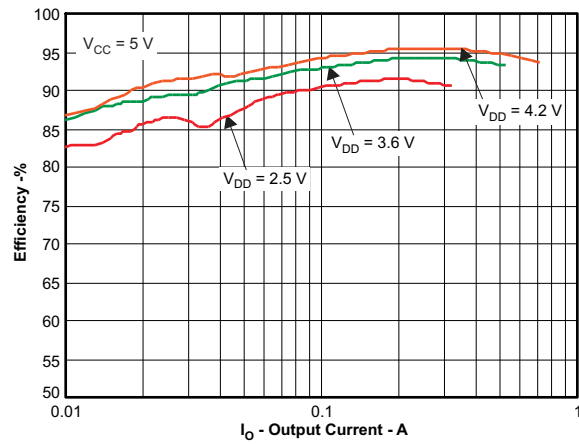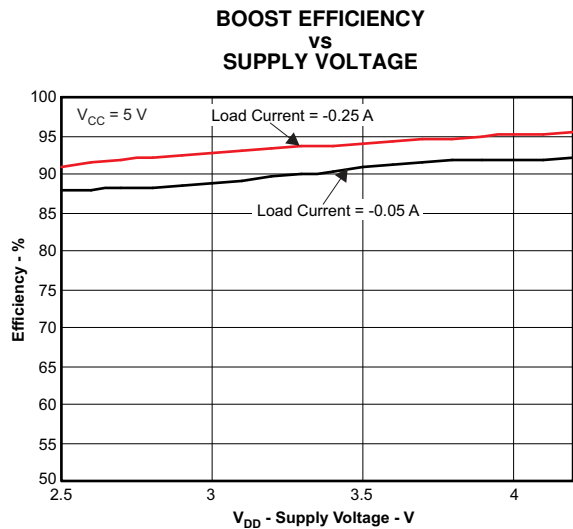
Figure 14.

Start-Up Time

Figure 15.

Product Folder Link(s): TPA2014D1

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA2014D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier with common-mode feedback. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{CC}/2$ regardless of the common-mode voltage at the input. The fully differential TPA2014D1 can still be used with a single-ended input; however, the TPA2014D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. The inputs of the TPA2014D1 can be biased anywhere within the common mode input voltage ran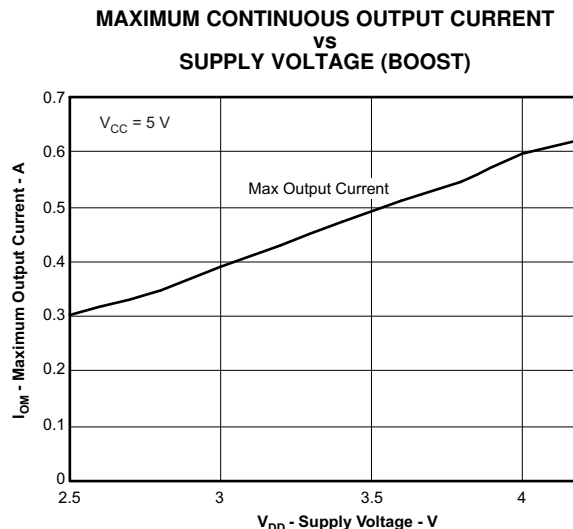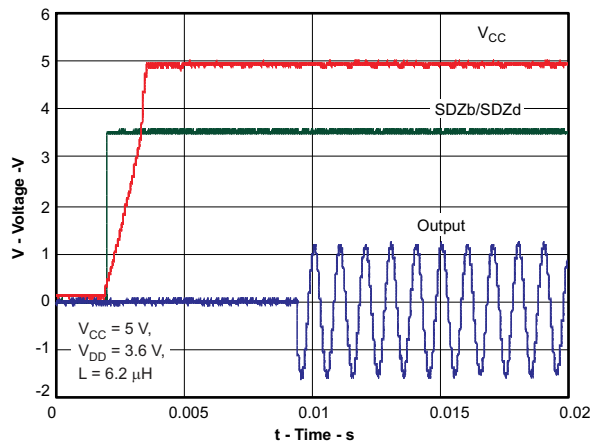ge listed in the Recommended Operating Conditions table. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
  - The fully differential amplifier does not require a bypass capacitor. Any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal better than the typical audio amplifier.

BOOST CONVERTER

The TPA2014D1 consists of a boost converter and a Class-D amplifier. The boost converter takes a low supply voltage, V_{DD}, and increases it to a higher output voltage, V_{CC}. V_{CC} is the supply voltage for the Class-D amplifier.

The two main passive components necessary for the boost converter are the boost inductor and the boost capacitor. The boost inductor stores current, and the boost capacitor stores charge. As the Class-D amplifier depletes the charge in the boost capacitor, the boost inductor charges it back up with the stored current. The cycle of charge/discharge occurs at a frequency of f_{boost}.

The TPA2014D1 allows a range of V_{CC} voltages, including setting V_{CC} lower than V_{DD}.

Boost Terms

The following is a list of terms and definitions used in the boost equations found later in this document.

C	Minimum boost capacitance required for a given ripple voltage on V_{CC}.
L	Boost inductor
f_{boost}	Switching frequency of the boost converter.
I_{CC}	Current pulled by the Class-D amplifier from the boost converter.
I_L	Average current through the boost inductor.
R1 and R2	Resistors used to set the boost voltage.
V_{CC}	Boost voltage. Generated by the boost converter. Voltage supply for the Class-D amplifier.
V_{DD}	Supply voltage to the IC.
ΔI_L	Ripple current through the inductor.
ΔV	Ripple voltage on V_{CC} due to capacitance.

Product Folder Link(s): *TPA2014D1*

SETTING THE BOOST VOLTAGE

Use Equation 1 to determine the value of R1 for a given V_{CC}. The maximum recommended value for V_{CC} is 5.5 V. The typical value of the V_{CC}FB pin is 500 mV. The current through the resistor divider should be about 100 times greater than the current into the V_{CC}FB pin, typically 0.01 µA. Based on those two values, the recommended value of R2 is 500 kΩ. V_{CC} must be greater than 3 V and less than or equal to 5.5 V.

$$V_{CC} = \left(\frac{0.5 \times (R1 + R2)}{R1} \right)$$

(1)

INDUCTOR SELECTION

SURFACE MOUNT INDUCTORS

Working inductance decreases as inductor current increases. If the drop in working inductance is severe enough, it may cause the boost converter to become unstable, or cause the TPA2014D1 to reach its current limit at a lower output power than expected. Inductor vendors specify currents at which inductor values decrease by a specific percentage. This can vary by 10% to 35%. Inductance is also affected by dc current and temperature.

TPA2014D1 INDUCTOR EQUATIONS

Inductor current rating is determined by the requirements of the load. The inductance is determined by two factors: the minimum value required for stability and the maximum ripple current permitted in the application.

Use Equation 2 to determine the required current rating. Equation 2 shows the approximate relationship between the average inductor current, I_L, to the load current, load voltage, and input voltage (I_{CC}, V_{CC}, and V_{DD}, respectively). Insert I_{CC}, V_{CC}, and V_{DD} into Equation 2 to solve for I_L. The inductor must maintain at least 90% of its initial inductance value at this current.

$$I_L = I_{CC} \times \left(\frac{V_{CC}}{V_{DD} \times 0.8} \right)$$

(2)

The minimum working inductance is 2.2 µH. A lower value may cause instability.

Ripple current, ΔI_L, is peak-to-peak variation in inductor current. Smaller ripple current reduces core losses in the inductor as well as the potential for EMI. Use Equation 3 to determine the value of the inductor, L. Equation 3 shows the relationship between inductance L, V_{DD}, V_{CC}, the switching frequency, f_{boost}, and ΔI_L. Insert the maximum acceptable ripple current into Equation 3 to solve for L.

$$L = \frac{V_{DD} \times (V_{CC} - V_{DD})}{\Delta I_L \times f_{boost} \times V_{CC}}$$

(3)

ΔI_L is inversely proportional to L. Minimize ΔI_L as much as is necessary for a specific application. Increase the inductance to reduce the ripple current. Note that making the inductance too large will prevent the boost converter from responding to fast load changes properly. Typical inductor values for the TPA2014D1 are 4.7 µH to 6.8 µH.

Select an inductor with a small dc resistance, DCR. DCR reduces the output power due to the voltage drop across the inductor.

CAPACITOR SELECTION

SURFACE MOUNT CAPACITORS

Temperature and applied dc voltage influence the actual capacitance of high-K materials.

Table 3 shows the relationship between the different types of high-K materials and their associated tolerances, temperature coefficients, and temperature ranges. Notice that a capacitor made with X5R material can lose up to 15% of its capacitance within its working temperature range.

High-K material is very sensitive to applied dc voltage. X5R capacitors can have losses ranging from 15 to 45% of their initial capacitance with only half of their dc rated voltage applied. For example, if 5 Vdc is applied to a 10 V, 1 µF X5R capacitor, the measured capacitance at that point may show 0.85 µF, 0.55 µF, or somewhere in between. Y5V capacitors have losses that can reach or exceed 50% to 75% of their rated value.

In an application, the working capacitance of components made with high-K materials is generally lower than nominal capacitance. A worst case result with a typical X5R material might be −10% tolerance, −15% temperature effect, and −45% dc voltage effect at 50% of the rated voltage. This particular case results in a working capacitance of 42% ($0.9 \times 0.85 \times 0.55$) of the nominal value.

Select high-K ceramic capacitors according to the following rules:

1. Use capacitors made of materials with temperature coefficients of X5R, X7R, or better.
2. Use capacitors with dc voltage ratings of at least twice the application voltage. Use minimum 10 V capacitors for the TPA2014D1.
3. Choose a capacitance value at least twice the nominal value calculated for the application. Multiply the nominal value by a factor of 2 for safety. If a 10 µF capacitor is required, use 20 µF.

The preceding rules and recommendations apply to capacitors used in connection with the TPA2014D1. The TPA2014D1 cannot meet its performance specifications if the rules and recommendations are not followed.

Table 3. Typical Tolerance and Temperature Coefficient of Capacitance by Material

Material	COG/NPO	X7R	X5R
Typical Tolerance	±5%	±10%	80/–20%
Temperature Coefficient	±30ppm	±15%	22/–82%
Temperature Range, °C	−55/125°C	−55/125°C	-30/85°C

Product Folder Link(s): *TPA2014D1*

TPA2014D1 CAPACITOR EQUATIONS

The value of the boost capacitor is determined by the minimum value of working capacitance required for stability and the maximum voltage ripple allowed on V_{CC} in the application. The minimum value of working capacitance is 10 µF. Do not use any component with a working capacitance less than 10 µF.

For X5R or X7R ceramic capacitors, Equation 4 shows the relationship between the boost capacitance, C, to load current, load voltage, ripple voltage, input voltage, and switching frequency (I_{CC}, V_{CC}, ΔV, V_{DD}, f_{boost} respectively). Insert the maximum allowed ripple voltage into Equation 4 to solve for C. A factor of 2 is included to implement the rules and specifications listed earlier.

$$C = 2 \times \frac{I_{CC} \times (V_{CC} - V_{DD})}{\Delta V \times f_{boost} \times V_{CC}}$$

(4)

For aluminum or tantalum capacitors, Equation 5 shows the relationship between he boost capacitance, C, to load current, load voltage, ripple voltage, input voltage, and switching frequency (I_{CC}, V_{CC}, ΔV, V_{DD}, f_{boost} respectively). Insert the maximum allowed ripple voltage into Equation 5 to solve for C. Solve this equation assuming ESR is zero.

$$C = \frac{I_{CC} \times (V_{CC} - V_{DD})}{\Delta V \times f_{boost} \times V_{CC}}$$

(5)

Capacitance of aluminum and tantalum capacitors is normally not sensitive to applied voltage so there is no factor of 2 included in Equation 5. However, the ESR in aluminum and tantalum capacitors can be significant. Choose an aluminum or tantalum capacitor with ESR around 30 mΩ. For best performance using of tantalum capacitor, use at least a 10 V rating. Note that tantalum capacitors must generally be used at voltages of half their ratings or less.

Submit Documentation Feedback

Product Folder Link(s): *TPA2014D1*

RECOMMENDED INDUCTOR AND CAPACITOR VALUES BY APPLICATION

Use Table 4 as a guide for determining the proper inductor and capacitor values.

Table 4. Recommended Values

Class-D Output Power (W)[1]	Class-D Load (Ω)	Minimum V_{DD} (V)	Required V_{CC} (V)	Max I_L (A)	L (μH)	Inductor Vendor Part Numbers	Max ΔV (mV$_{PP}$)	C[2] (μF)	Capacitor Vendor Part Numbers
1	8	3	4.3	0.70	3.3	Toko DE2812C Coilcraft DO3314 Murata LQH3NPN3R3NG0	30	10	Kemet C1206C106K8PACTU Murata GRM32ER61A106KA01B Taiyo Yuden LMK316BJ106ML-T
1.2	8	3	5.0	0.9	4.7	Murata LQH43PN4R7NR0 Toko DE4514C Coilcraft LPS4018-472	30	22	Murata GRM32ER71A226KE20L Taiyo Yuden LMK316BJ226ML-T

(1)   All power levels are calculated at 1% THD unless otherwise noted
(2)   All values listed are for ceramic capacitors. The correction factor of 2 is included in the values.

CLASS-D REQUIREMENTS

DECOUPLING CAPACITORS

The TPA2014D1 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF as close as possible to the device VDD lead. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the TPA2014D1 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. Place a capacitor of 10 μF or greater between the power supply and the boost inductor. The capacitor filters out high frequency noise. More importantly, it acts as a charge reservoir, providing energy more quickly than the board supply, thus helping to prevent any droop.

INPUT CAPACITORS

The TPA2014D1 does not require input coupling capacitors if the design uses a differential source that is biased within the common mode input range. Use input coupling capacitors if the input signal is not biased within the recommended common-mode input range, if high pass filtering is needed, or if using a single-ended source.

The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in Equation 6.

$$f_C = \frac{1}{(2 \times \pi \times R_I C_I)}$$

(6)

The value of the input capacitor is important because it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones does not usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Use Equation 7 to find the required the input coupling capacitance.

$$C_I = \frac{1}{(2 \times \pi \times f_C \times R_I)}$$

(7)

Any mismatch in capacitance between the two inputs will cause a mismatch in the corner frequencies. Choose capacitors with a tolerance of ±10% or better.

Product Folder Link(s): *TPA2014D1*

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter is often used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and a low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

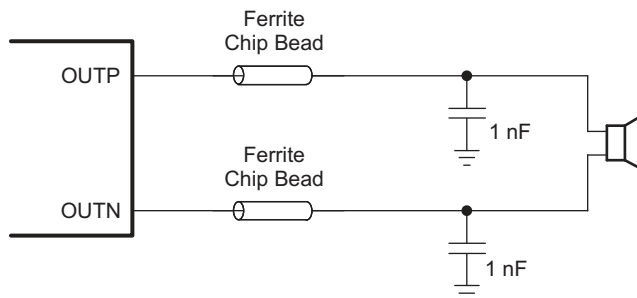Figure 16 shows a typical ferrite bead output filters.

Figure 16. Typical Ferrite Chip Bead Filter

Suggested Chip Ferrite Bead

Load	Vendor	Part Number	Size
8 Ω	Murata	BLM18EG121SN1	0603

OPERATION WITH DACs AND CODECs

When using switching amplifiers with CODECs and DACs, there may be an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC with the switching frequencies of the audio amplifier input stage. The noise increase is solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance.

The TPA2014D1 has a two pole low pass filter at the inputs. The cutoff frequency of the filter is set to approximately 100kHz. The integrated low pass filter of the TPA2014D1 eliminates the need for additional external filtering components. A properly designed additional low pass filter may be added without altering the performance of the device.

BYPASSING THE BOOST CONVERTER

Bypass the boost converter to drive the Class-D amplifier directly from the battery. Place a Shottky diode between the SW pin and the $V_{CC}IN$ pin. Select a diode that has an average forward current rating of at least 1A, reverse breakdown voltage of 10 V or greater, and a forward voltage as small as possible. See Figure 17 for an example of a circuit designed to bypass the boost converter.

Do not configure the circuit to bypass the boost converter if V_{DD} is higher than V_{CC} when the boost converter is enabled ($\overline{SDb} \geq 1.3$ V); V_{DD} must be lower than V_{CC} for proper operation. V_{DD} may be set to any voltage within the recommended operating range when the boost converter is disabled ($\overline{SDb} \leq 0.3$V).

Place a logic high on $\overline{SDb}$ to place the TPA2014D1 in boost mode. Place a logic low on $\overline{SDb}$ to place the TPA2014D1 in bypass mode.
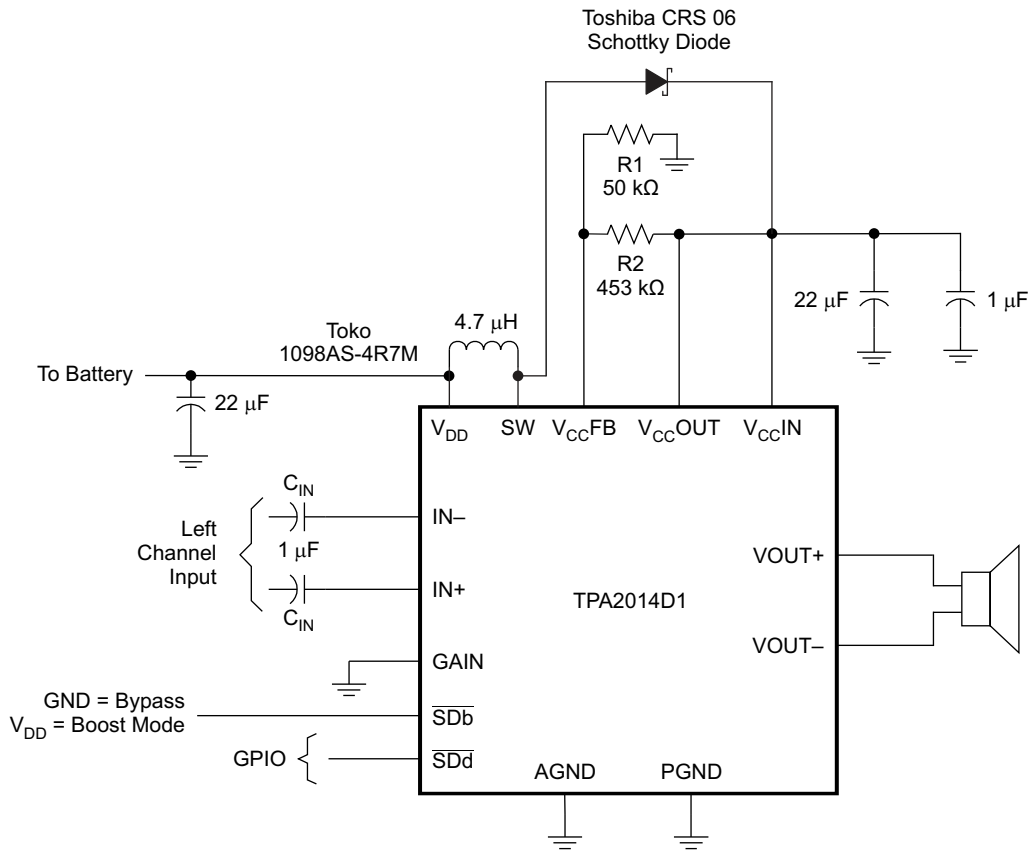
Figure 17. Bypass Circuit

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factors for the YZH and RGP packages are shown in the dissipation rating table. Apply the same principles to both packages. Using the YZH package, and converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0124} = 80.64°\text{C/W}$$

(8)

Given θ_{JA} of 80.64°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.193 W (V_{DD} = 3.6 V, P_O = 1.2 W), the maximum ambient temperature is calculated with the following equation:

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{Dmax} = 150 - 80.64\,(0.193) = 134°\text{C}$$

(9)

Equation 9 shows that the calculated maximum ambient temperature is 134°C at maximum power dissipation under the above conditions. The TPA2014D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

BOARD LAYOUT

In making the pad size for the WCSP balls, use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 18 and Table 5 show the appropriate diameters for a WCSP layout.
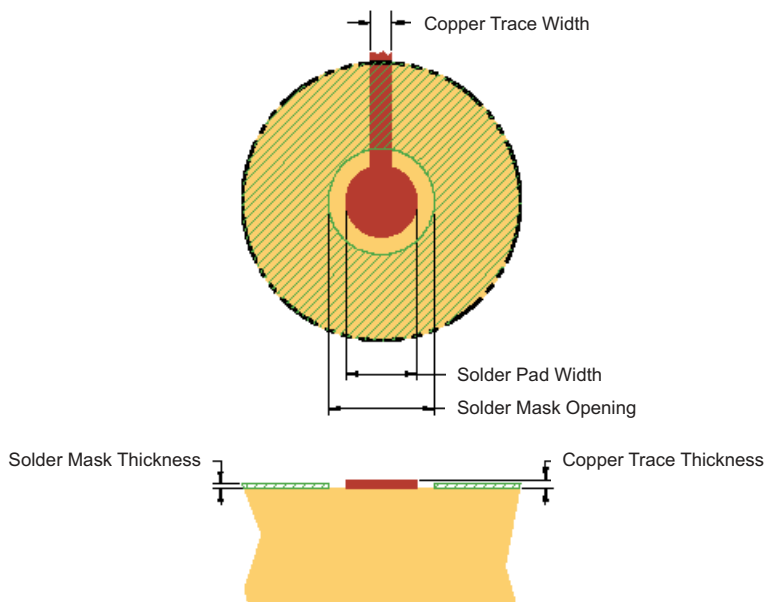
Figure 18. Land Pattern Dimensions

Table 5. Land Pattern Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 μm (+0.0, −25 μm)	375 μm (+0.0, −25 μm)	1 oz max (32 μm)	275 μm x 275 μm Sq. (rounded corners)	125 μm thick

NOTES:

1. Circuit traces from NSMD defined PWB lands should be 75 μm to 100 μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.

2. Recommend solder paste is Type 3 or Type 4.

3. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.

4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.

5. Solder mask thickness should be less than 20 μm on top of the copper circuit pattern.

6. Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.

7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Trace Width

Recommended trace width at the solder balls is 75 μm to 100 μm to prevent solder wicking onto wider PCB traces.

For high current pins (SW, PGND, VOUT+, VOUT−, V_{CC}IN, and V_{CC}OUT) of the TPA2014D1, use 100 μm trace widths at the solder balls and at least 500 μm PCB traces to ensure proper performance and output power for the device.

For low current pins (IN−, IN+, $\overline{SDd}$, $\overline{SDb}$, GAIN, V_{CC}FB, V_{DD}) of the TPA2014D1, use 75 μm to 100 μm trace widths at the solder balls. Run IN- and IN+ traces side-by-side to maximize common-mode noise cancellation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2014D1RGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CEK	Samples
TPA2014D1RGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CEK	Samples
TPA2014D1YZHR	ACTIVE	DSBGA	YZH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEJ	Samples
TPA2014D1YZHT	ACTIVE	DSBGA	YZH	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CEJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

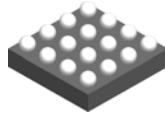| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2014D1RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2014D1RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA2014D1YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1
TPA2014D1YZHT	DSBGA	YZH	16	250	180.0	8.4	2.35	2.35	0.81	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

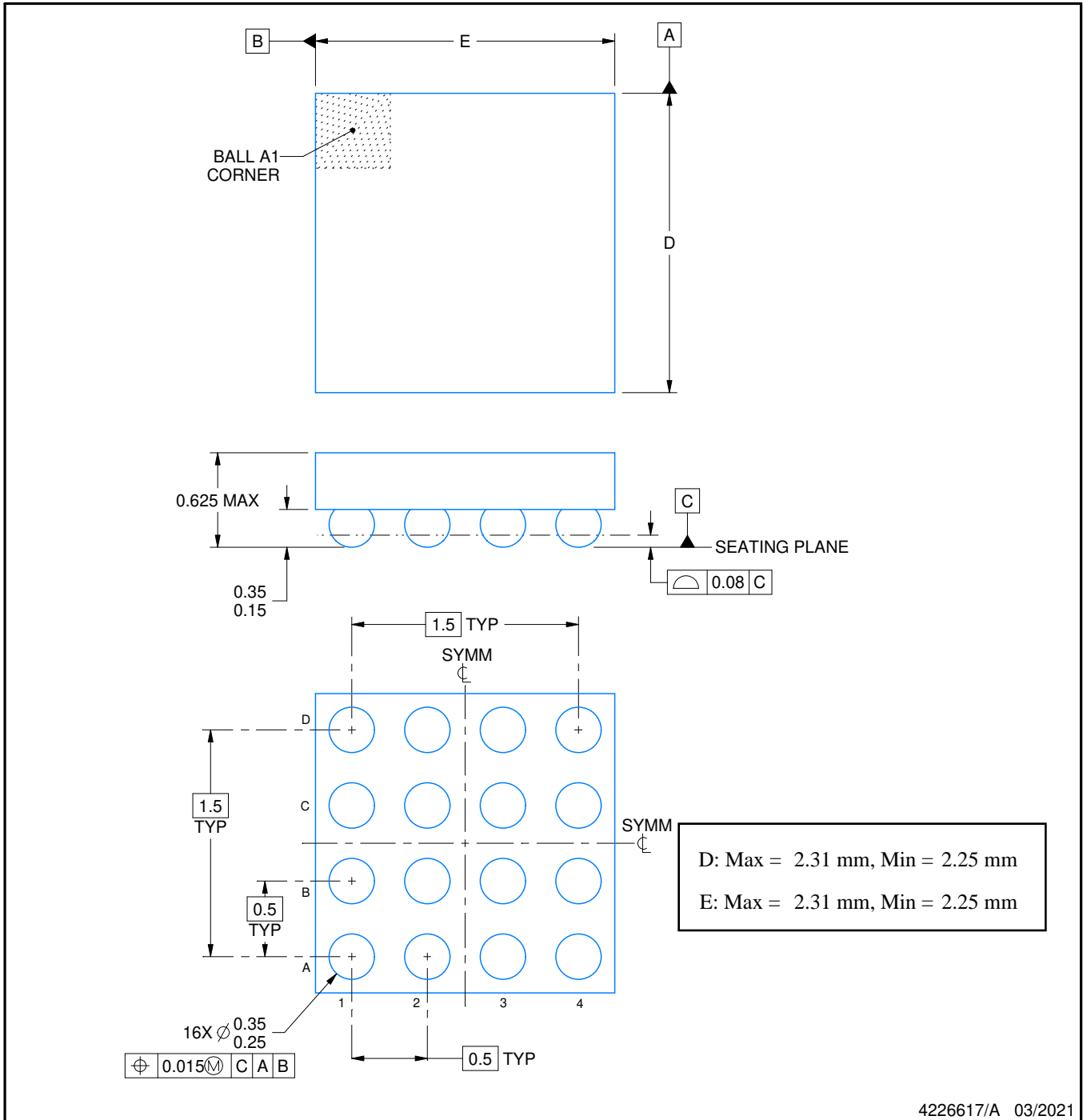| Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2014D1RGPR	QFN	RGP	20	3000	356.0	356.0	35.0
TPA2014D1RGPT	QFN	RGP	20	250	210.0	185.0	35.0
TPA2014D1YZHR	DSBGA	YZH	16	3000	182.0	182.0	20.0
TPA2014D1YZHT	DSBGA	YZH	16	250	182.0	182.0	20.0

B   E   A

BALL A1
CORNER

D

0.625 MAX

0.35
0.15

| C |

SEATING PLANE

△ 0.08 C

1.5 TYP

SYMM
℄

D

1.5
TYP

C

SYMM
℄

0.5
TYP

B

A

1   2   3   4

16X ⌀ 0.35
0.25

⊕ 0.015Ⓜ C A B

0.5 TYP

D: Max = 2.31 mm, Min = 2.25 mm

E: Max = 2.31 mm, Min = 2.25 mm
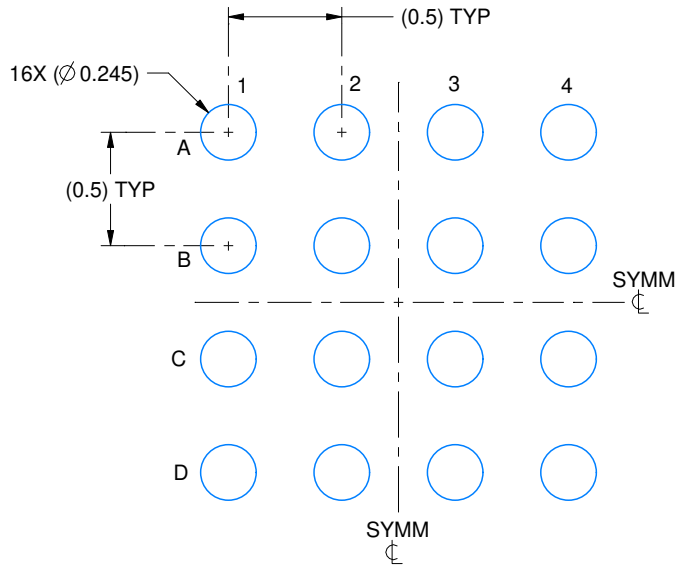
4226617/A   03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
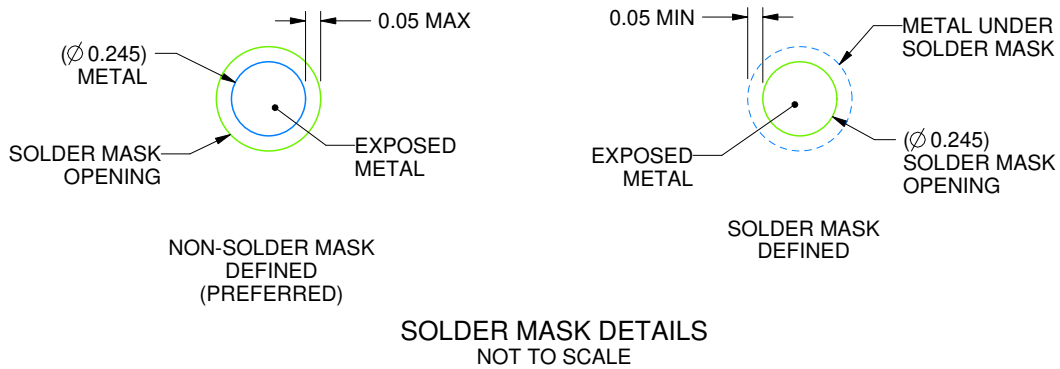2. This drawing is subject to change without notice.

(0.5) TYP

16X (⌀ 0.245)

(0.5) TYP

1 2 3 4

A

B   SYMM
           ℄

C

D

SYMM
℄

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

0.05 MAX

(⌀ 0.245)
METAL

SOLDER MASK
OPENING

EXPOSED
METAL

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL UNDER
SOLDER MASK

EXPOSED
METAL

(⌀ 0.245)
SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
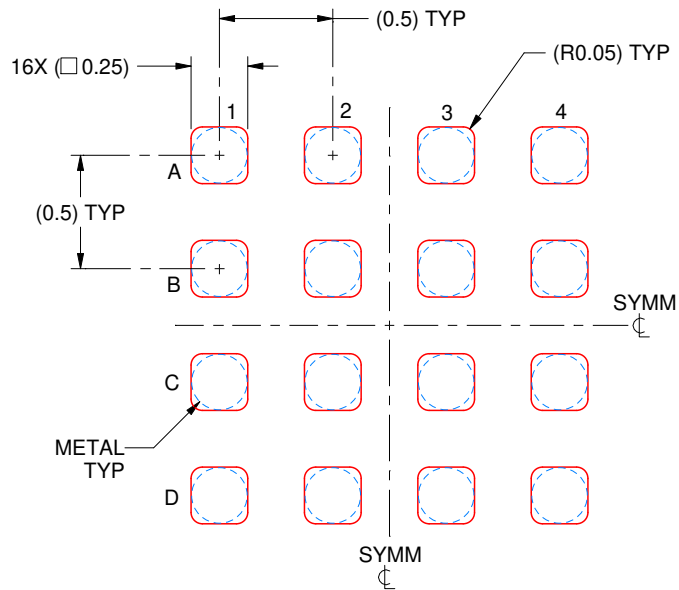NOT TO SCALE

4226617/A   03/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

TEXAS INSTRUMENTS
www.ti.com

16X (□ 0.25)

(0.5) TYP

(R0.05) TYP

(0.5) TYP

METAL
TYP

SYMM

SYMM

SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4226617/A   03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
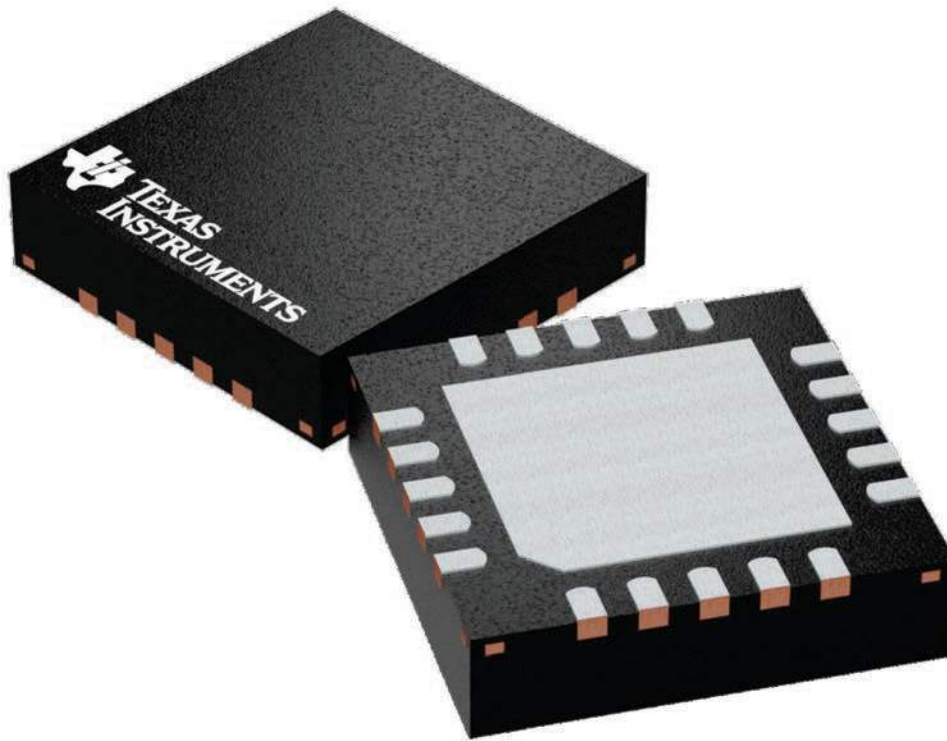
Images above are just a representation of the package family, actual package may vary.
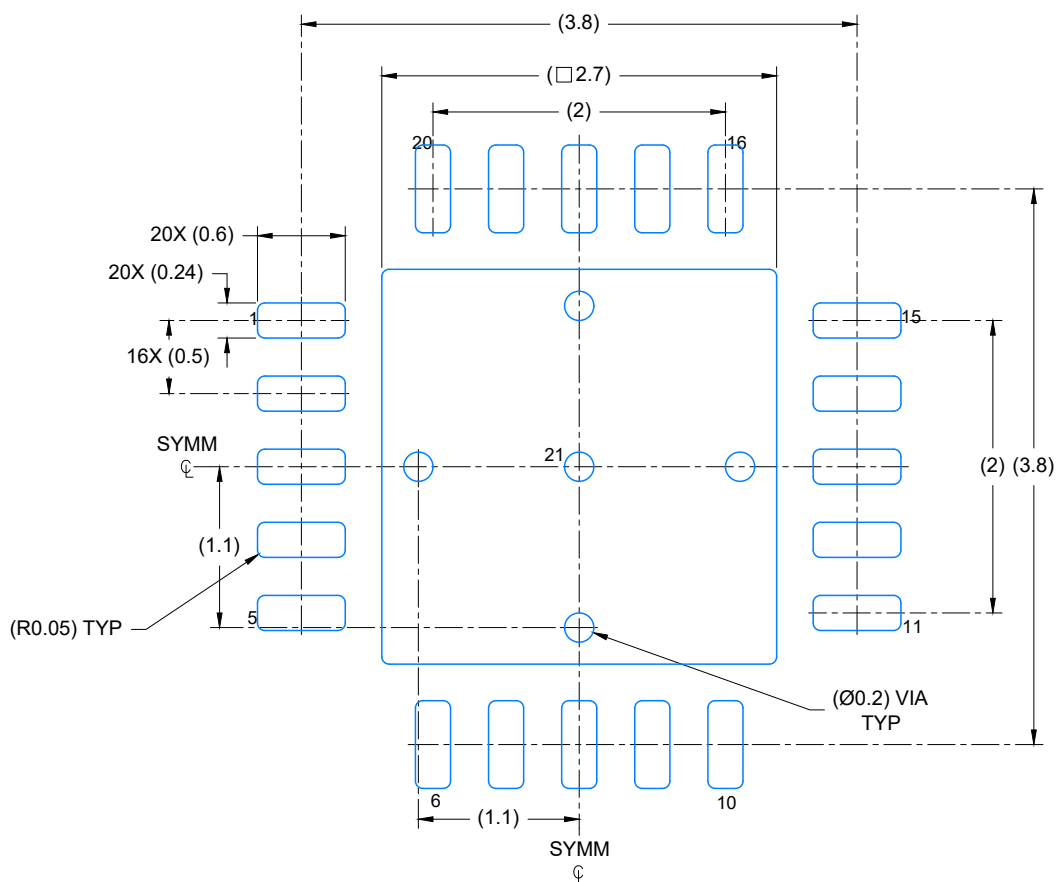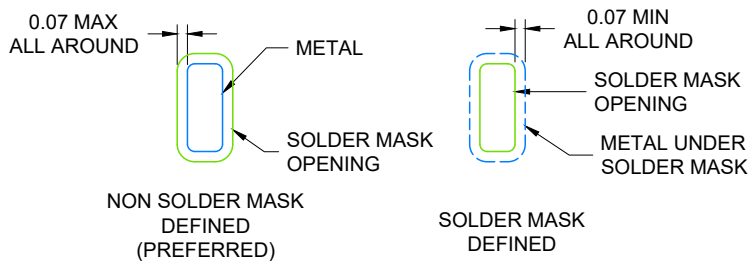Refer to the product data sheet for package details.

4224735/A
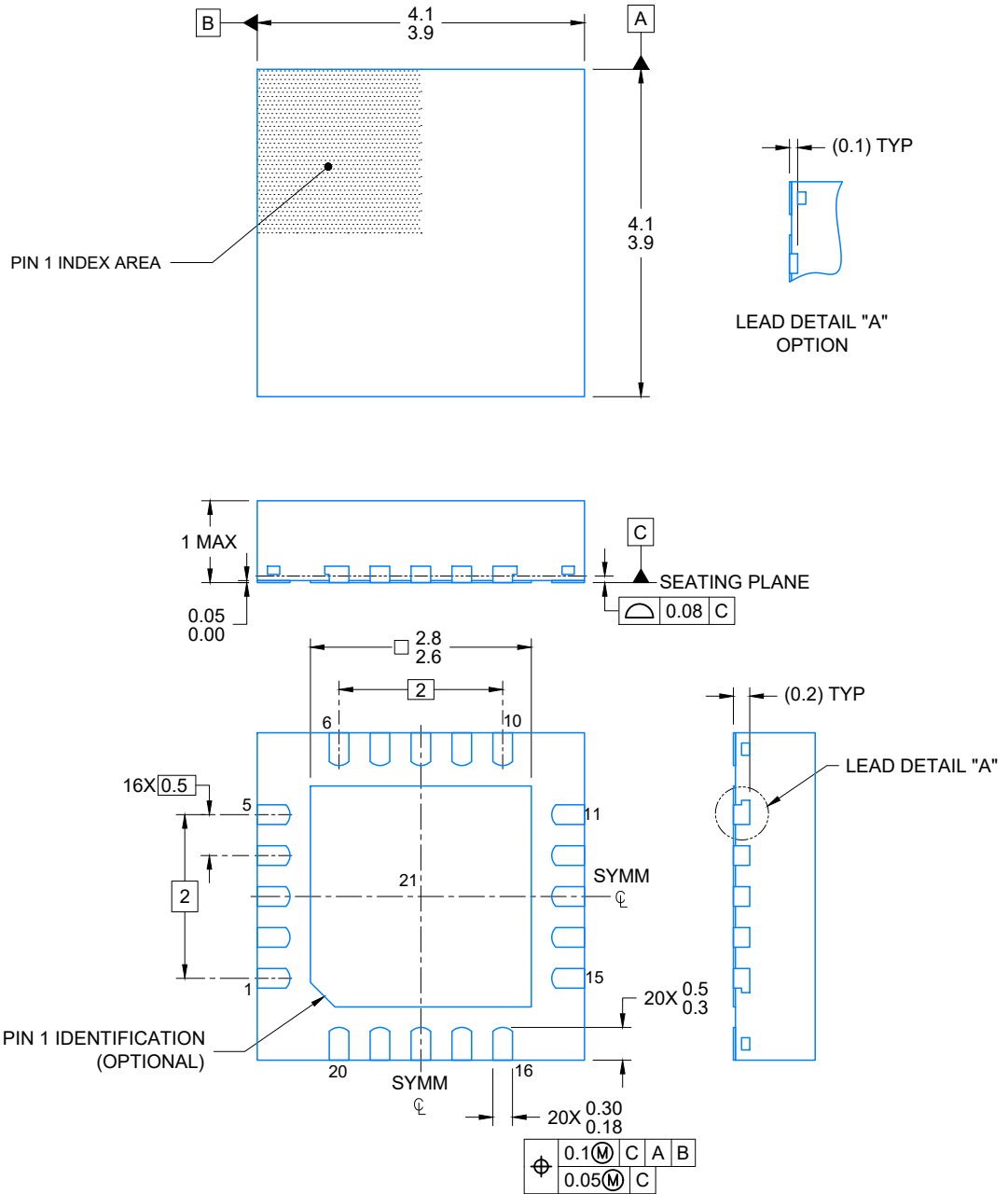
4219028/A   12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

(3.8)

(□2.7)

(2)

20

16

20X (0.6)

20X (0.24)

1

16X (0.5)

SYMM

(1.1)

(R0.05) TYP

5

15

11

(2) (3.8)

21

(Ø0.2) VIA
TYP

6

(1.1)

10

SYMM

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

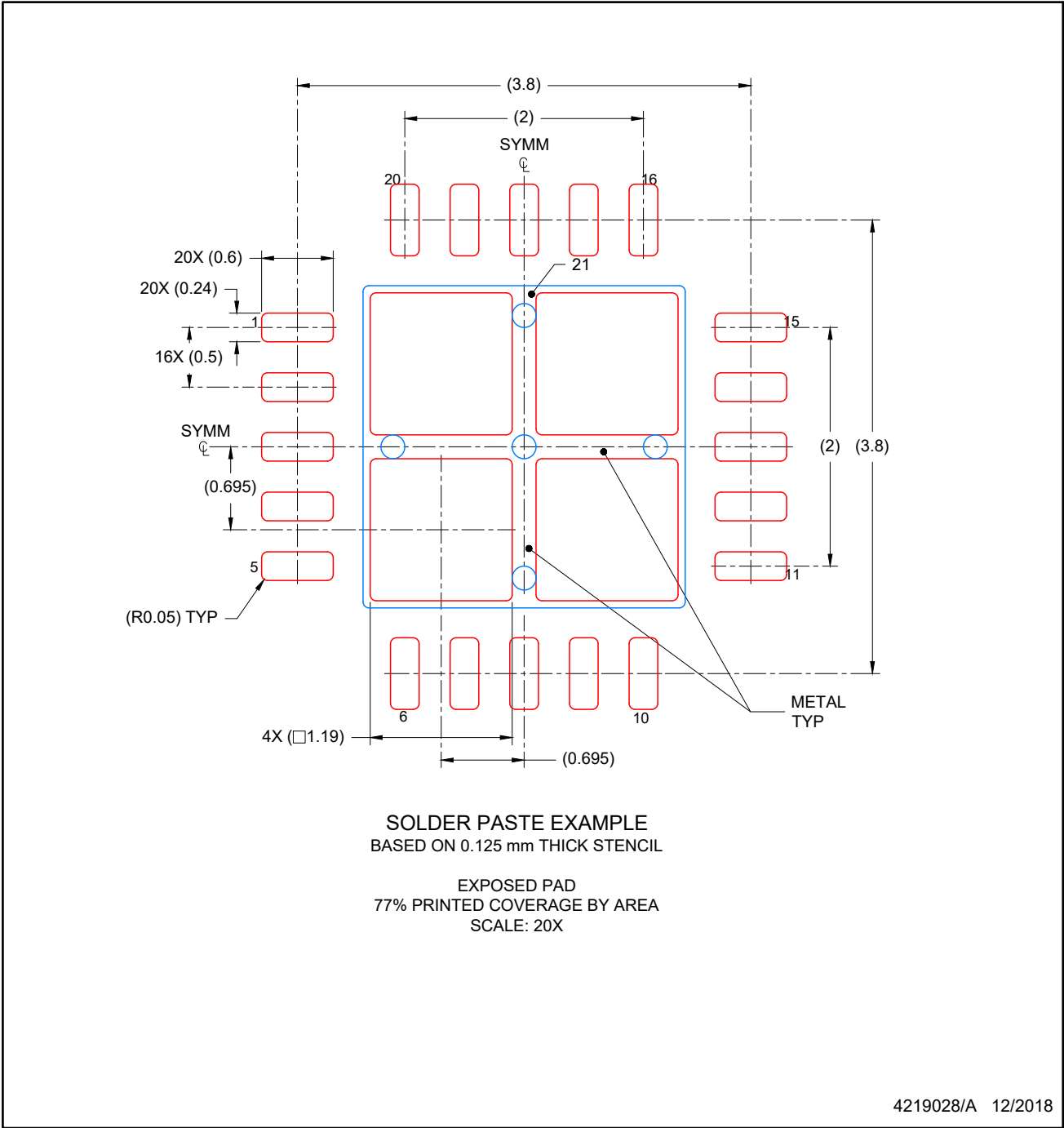4219028/A   12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED COVERAGE BY AREA
SCALE: 20X

4219028/A   12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated