

# 54/74193 54LS/74LS193

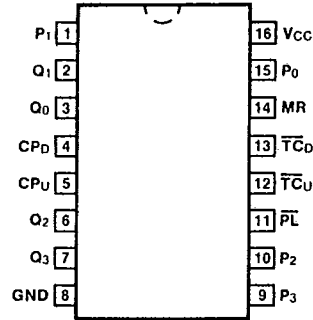
## UP/DOWN BINARY COUNTER (With Separate Up/down Clocks)

**DESCRIPTION** — The '193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ( $\overline{PL}$ ) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description and detail specifications please refer to the '192 data sheet.

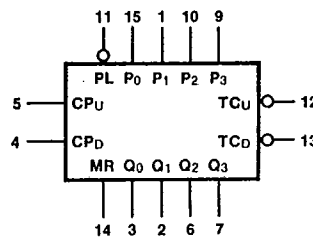
**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE   | MILITARY GRADE   | PKG TYPE |
|-----------------|---------|--|--|----------|
|                 |         | V <sub>CC</sub> = +5.0 V ±5%,<br>T <sub>A</sub> = 0°C to +70°C | V <sub>CC</sub> = +5.0 V ±10%,<br>T <sub>A</sub> = -55°C to +125°C |          |
| Plastic DIP (P) | A       | 74193PC, 74LS193PC   |  | 9B       |
| Ceramic DIP (D) | A       | 74193DC, 74LS193DC   | 54193DM, 54LS193DM   | 6B       |
| Flatpak (F)     | A       | 74193FC, 74LS193FC   | 54193FM, 54LS193FM   | 4L       |

**CONNECTION DIAGRAM  
PINOUT A**



**LOGIC SYMBOL**



V<sub>CC</sub> = Pin 16  
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES                       | DESCRIPTION                                      | 54/74 (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---------------------------------|--|-----------------------|-------------------------|
| CP <sub>U</sub>                 | Count Up Clock Input (Active Rising Edge)        | 1.0/1.0               | 0.5/0.25                |
| CP <sub>D</sub>                 | Count Down Clock Input (Active Rising Edge)      | 1.0/1.0               | 0.5/0.25                |
| MR                              | Asynchronous Master Reset Input (Active HIGH)    | 1.0/1.0               | 0.5/0.25                |
| $\overline{PL}$                 | Asynchronous Parallel Load Input (Active LOW)    | 1.0/1.0               | 0.5/0.25                |
| P <sub>0</sub> — P <sub>3</sub> | Parallel Data Inputs                             | 1.0/1.0               | 0.5/0.25                |
| Q <sub>0</sub> — Q <sub>3</sub> | Flip-flop Outputs                                | 20/10                 | 10/5.0 (2.5)            |
| $\overline{TC}_D$               | Terminal Count Down (Borrow) Output (Active LOW) | 20/10                 | 10/5.0 (2.5)            |
| $\overline{TC}_U$               | Terminal Count Up (Carry) Output (Active LOW)    | 20/10                 | 10/5.0 (2.5)            |

4

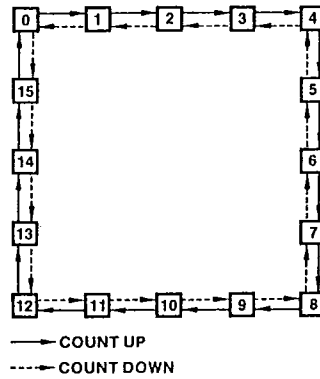
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MODE SELECT TABLE

| MR | $\overline{PL}$ | CP <sub>U</sub> | CP <sub>D</sub> | MODE           |
|----|-----------------|-----------------|-----------------|----------------|
| H  | X               | X               | X               | Reset (Asyn.)  |
| L  | L               | X               | X               | Preset (Asyn.) |
| L  | H               | H               | H               | No Change      |
| L  | H               | $\downarrow$    | H               | Count Up       |
| L  | H               | H               | $\downarrow$    | Count Down     |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

STATE DIAGRAM



LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

LOGIC DIAGRAM

