

# DDR 13-Bit to 26-Bit Registered Buffer

## Recommended Applications:

- DDR Memory Modules:
  - DDRI (PC1600, PC2100)
  - DDR333 (PC2700)
  - DDRI-400 (PC3200)
- Provides complete DDR DIMM solution with ICS93V857 or ICS95V857
- SSTL\_2 compatible data registers

## Product Features:

- Differential clock signals
- Meets SSTL\_2 signal data
- Supports SSTL\_2 class I specifications on outputs
- Low-voltage operation
  - $V_{DD} = 2.3V$  to  $2.7V$
- Available in 64 pin TSSOP and 56 pin MLF packages
- Exceeds ICSSSTVN16859 performance

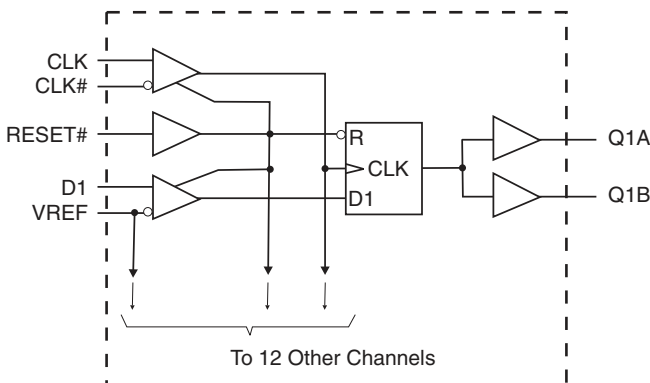
## Truth Table<sup>1</sup>

Inputs				Q Outputs
RESET#	CLK	CLK#	D	Q
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	$Q_0^{(2)}$

## Notes:

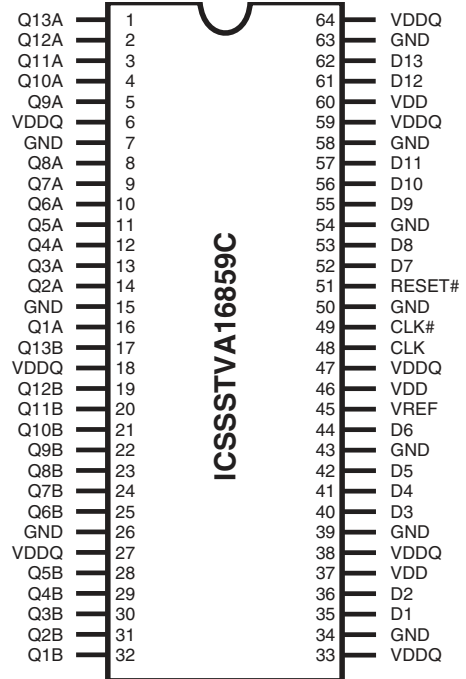
1. H = "High" Signal Level  
 L = "Low" Signal Level  
 ↑ = Transition "Low"-to-"High"  
 ↓ = Transition "High"-to-"Low"  
 X = Don't Care
2. Output level before the indicated steady state input conditions were established.

## Block Diagram



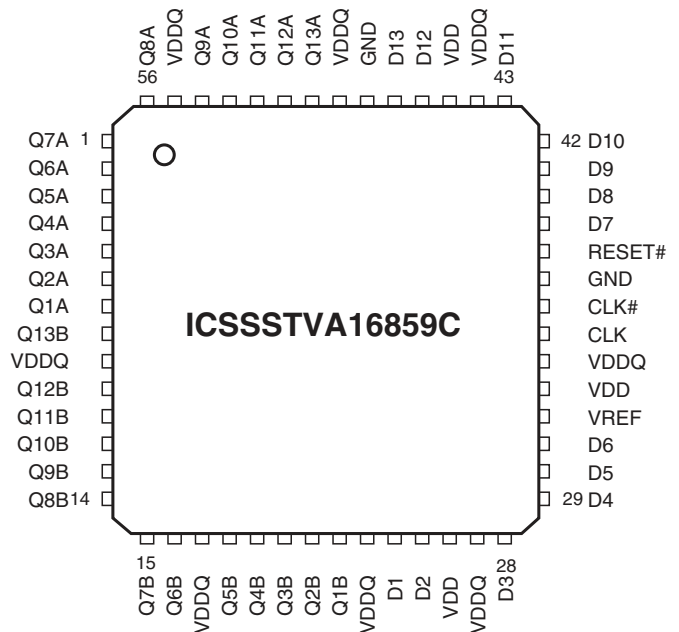
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## Pin Configurations



## 64-Pin TSSOP

6.10 mm. Body, 0.50 mm. Pitch



## 56-Pin VFQFN (MLF2)

# ICSSSTVA16859C

## General Description

The 13-bit-to-26-bit **ICSSSTVA16859C** is a universal bus driver designed for 2.3V to 2.7V  $V_{DD}$  operation and SSTL\_2 I/O levels, except for the LVCMOS RESET# input.

Data flow from D to Q is controlled by the differential clock (CLK/CLK#) and a control signal (RESET#). The positive edge of CLK is used to trigger the data flow and CLK# is used to maintain sufficient noise margins where as RESET#, an LVCMOS asynchronous signal, is intended for use at the time of power-up only. **ICSSSTVA16859C** supports low-power standby operation. A logic level “Low” at RESET# assures that all internal registers and outputs (Q) are reset to the logic “Low” state, and all input receivers, data (D) and clock (CLK/CLK#) are switched off. Please note that RESET# must always be supported with LVCMOS levels at a valid logic state because VREF may not be stable during power-up.

To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESET# must be held at a logic “Low” level during power up.

In the DDR DIMM application, RESET# is specified to be completely asynchronous with respect to CLK and CLK#. Therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic “Low” level quickly relative to the time to disable the differential input receivers. This ensures there are no glitches on the output. However, when coming out of low-power standby state, the register will become active quickly relative to the time to enable the differential input receivers. When the data inputs are at a logic level “Low” and the clock is stable during the “Low”-to-“High” transition of RESET# until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic “Low” level.

## Pin Configuration (64-Pin TSSOP)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1-5, 8-14, 16, 17, 19-25, 28-32	Q (13:1)	OUTPUT	Data output
7, 15, 26, 34, 39, 43, 50, 54, 58, 63	GND	PWR	Ground
6, 18, 27, 33, 38, 47, 59, 64	VDDQ	PWR	Output supply voltage, 2.5V nominal
35, 36, 40-42, 44, 52, 53, 55-57, 61, 62	D (13:1)	INPUT	Data input
48	CLK	INPUT	Positive master clock input
49	CLK#	INPUT	Negative master clock input
37, 46, 60	VDD	PWR	Core supply voltage, 2.5V nominal
51	RESET#	INPUT	Reset (active low)
45	VREF	INPUT	Input reference voltage, 2.5V nominal

## Pin Configuration (56-Pin MLF2)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1-8, 10-16, 18-22, 50-54, 56	Q (13:1)	OUTPUT	Data output
37, 48	GND	PWR	Ground
9, 17, 23, 27, 34, 44, 49, 55	VDDQ	PWR	Output supply voltage, 2.5V nominal
24, 25, 28-31, 39-43, 46, 47	D (13:1)	INPUT	Data input
35	CLK	INPUT	Positive master clock input
36	CLK#	INPUT	Negative master clock input
26, 33, 45	VDD	PWR	Core supply voltage, 2.5V nominal
38	RESET#	INPUT	Reset (active low)
32	VREF	INPUT	Input reference voltage, 2.5V nominal
-	Center PAD	PWR	Ground (MLF2 package only)

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## Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to 3.6V
Input Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5
Output Voltage <sup>1,2</sup>	-0.5 to V <sub>DDQ</sub> +0.5
Input Clamp Current	±50 mA
Output Clamp Current	±50 mA
Continuous Output Current	±50 mA
V <sub>DD</sub> , V <sub>DDQ</sub> or GND Current/Pin	±100 mA
Package Thermal Impedance <sup>3</sup>	55°C/W

### Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level V<sub>O</sub> > V<sub>DDQ</sub>.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operating Conditions - DDR/DDR333 (PC1600, PC2100, PC2700)

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V <sub>DD</sub>	Supply Voltage		2.3	2.5	2.7	V
V <sub>DDQ</sub>	I/O Supply Voltage		2.3	2.5	2.7	
V <sub>REF</sub>	Reference Voltage		1.15	1.25	1.35	
V <sub>TT</sub>	Termination Voltage		V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
V <sub>I</sub>	Input Voltage		0		V <sub>DDQ</sub>	
V <sub>IH(DC)</sub>	DC Input High Voltage	Data Inputs	V <sub>REF</sub> + 0.15			
V <sub>IH(AC)</sub>	AC Input High Voltage		V <sub>REF</sub> + 0.31			
V <sub>IL(DC)</sub>	DC Input Low Voltage				V <sub>REF</sub> - 0.15	
V <sub>IL(AC)</sub>	AC Input Low Voltage				V <sub>REF</sub> - 0.31	
V <sub>IH</sub>	Input High Voltage Level	RESET#	1.7			
V <sub>IL</sub>	Input Low Voltage Level				0.7	
V <sub>ICR</sub>	Common mode Input Range	CLK, CLK#	0.97		1.53	
V <sub>ID</sub>	Differential Input Voltage		0.36			
V <sub>IX</sub>	Cross Point Voltage of Differential Clock Pair		(V <sub>DDQ</sub> /2) - 0.2		(V <sub>DDQ</sub> /2) + 0.2	
I <sub>OH</sub>	High-Level Output Current				-16	mA
I <sub>OL</sub>	Low-Level Output Current				16	
T <sub>A</sub>	Operating Free-Air Temperature		0		70	°C

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICSSSTVA16859C

## Recommended Operating Conditions - DDRI-400 (PC3200)

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V <sub>DD</sub>	Supply Voltage		2.5	2.6	2.7	V
V <sub>DDQ</sub>	I/O Supply Voltage		2.5	2.6	2.7	
V <sub>REF</sub>	Reference Voltage		1.25	1.3	1.35	
V <sub>TT</sub>	Termination Voltage		V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
V <sub>I</sub>	Input Voltage		0		V <sub>DDQ</sub>	
V <sub>IH(DC)</sub>	DC Input High Voltage	Data Inputs	V <sub>REF</sub> + 0.15			
V <sub>IH(AC)</sub>	AC Input High Voltage		V <sub>REF</sub> + 0.31			
V <sub>IL(DC)</sub>	DC Input Low Voltage				V <sub>REF</sub> - 0.15	
V <sub>IL(AC)</sub>	AC Input Low Voltage				V <sub>REF</sub> - 0.31	
V <sub>IH</sub>	Input High Voltage Level	RESET#	1.7			
V <sub>IL</sub>	Input Low Voltage Level				0.7	
V <sub>ICR</sub>	Common mode Input Range	CLK, CLK#	0.97		1.53	
V <sub>ID</sub>	Differential Input Voltage		0.36			
V <sub>IX</sub>	Cross Point Voltage of Differential Clock Pair		(V <sub>DDQ</sub> /2) - 0.2		(V <sub>DDQ</sub> /2) + 0.2	
I <sub>OH</sub>	High-Level Output Current				-16	mA
I <sub>OL</sub>	Low-Level Output Current				16	
T <sub>A</sub>	Operating Free-Air Temperature		0		70	°C

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## DC Electrical Characteristics - DDRI/DDR333 (PC1600, PC2100, PC2700)

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 2.5 \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5 \pm 0.2\text{V}$ ; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	$V_{DDQ}$	MIN	TYP	MAX	UNITS
$V_{IK}$		$I_I = -18\text{mA}$	2.3V			-1.2	V
$V_{OH}$		$I_{OH} = -100\mu\text{A}$	2.3V-2.7V	$V_{DDQ} - 0.2$			
		$I_{OH} = -8\text{mA}$	2.3V	1.95			
$V_{OL}$		$I_{OL} = 100\mu\text{A}$	2.3V-2.7V			0.2	
		$I_{OL} = 8\text{mA}$	2.3V			0.35	
$I_I$	All Inputs	$V_I = V_{DD}$ or GND	2.7V			$\pm 5$	$\mu\text{A}$
$I_{DD}$	Standby (Static)	RESET# = GND	2.7V			0.01	$\mu\text{A}$
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , RESET# = $V_{DD}$			TBD		
$I_{DDD}$	Dynamic operating (clock only)	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and CLK# switching 50% duty cycle.	2.7V			TBD	$\mu/\text{clock MHz}$
	Dynamic Operating (per each data input)	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle		$I_O = 0$			TBD
$r_{OH}$	Output High	$I_{OH} = -16\text{mA}$	2.3V-2.7V	7	13.5	20	$\Omega$
$r_{OL}$	Output Low	$I_{OL} = 16\text{mA}$	2.3V-2.7V	7	13	20	$\Omega$
$r_{O(D)}$	[ $r_{OH} - r_{OL}$ ] each separate bit	$I_O = 20\text{mA}$ , $T_A = 25^\circ\text{C}$	2.5V			4	$\Omega$
$C_i$	Data Inputs	$V_I = V_{REF} \pm 350\text{mV}$	2.5V	2.5		3.5	pF
	CLK and CLK#	$V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$		2.5		3.5	

Notes:

1 - Guaranteed by design, not 100% tested in production.

# ICSSSTVA16859C

## DC Electrical Characteristics - DDRI-400 (PC3200)

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 2.5 \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5 \pm 0.2\text{V}$ ; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	$V_{DDQ}$	MIN	TYP	MAX	UNITS
$V_{IK}$		$I_I = -18\text{mA}$	2.5V			-1.2	V
$V_{OH}$		$I_{OH} = -100\mu\text{A}$	2.5V-2.7V	$V_{DDQ} - 0.2$			
		$I_{OH} = -8\text{mA}$	2.7V	1.95			
$V_{OL}$		$I_{OL} = 100\mu\text{A}$	2.5V-2.7V			0.2	
		$I_{OL} = 8\text{mA}$	2.5V			0.35	
$I_I$	All Inputs	$V_I = V_{DD}$ or GND	2.7V			$\pm 5$	$\mu\text{A}$
$I_{DD}$	Standby (Static)	RESET# = GND	2.7V			0.01	$\mu\text{A}$
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , RESET# = $V_{DD}$			TBD		
$I_{DDD}$	Dynamic operating (clock only)	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and CLK# switching 50% duty cycle.	2.7V		TBD		$\mu/\text{clock MHz}$
	Dynamic Operating (per each data input)	RESET# = $V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle		$I_O = 0$		TBD	
$r_{OH}$	Output High	$I_{OH} = -16\text{mA}$	2.5V-2.7V	7	13.5	20	$\Omega$
$r_{OL}$	Output Low	$I_{OL} = 16\text{mA}$	2.5V-2.7V	7	13	20	$\Omega$
$r_{O(D)}$	[ $r_{OH} - r_{OL}$ ] each separate bit	$I_O = 20\text{mA}$ , $T_A = 25^\circ\text{C}$	2.6V			4	$\Omega$
$C_i$	Data Inputs	$V_I = V_{REF} \pm 350\text{mV}$	2.6V	2.5		3.5	pF
	CLK and CLK#	$V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$		2.5		3.5	

Notes:

1 - Guaranteed by design, not 100% tested in production.

## Timing Requirements<sup>1</sup>

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		V <sub>DDQ</sub> = 2.5V ± 0.2V		UNITS
			MIN	MAX	
f <sub>clock</sub>	Clock frequency			270	MHz
t <sub>SL</sub>	Output slew rate		1	4	V/ns
t <sub>S</sub>	Setup time, fast slew rate <sup>2 &amp; 4</sup>	Data before CLK↑, CLK#↓	0.4		ns
	Setup time, slow slew rate <sup>3 &amp; 4</sup>		0.6		ns
T <sub>h</sub>	Hold time, fast slew rate <sup>2 &amp; 4</sup>	Data after CLK↑, CLK#↓	0.4		ns
	Hold time, slow slew rate <sup>3 &amp; 4</sup>		0.5		ns

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
  - 2 - For data signal input slew rate of ≥ 1V/ns.
  - 3 - For data signal input slew rate of ≥ 0.5V/ns and < 1V/ns.
  - 4 - CLK, CLK# signals input slew rate of ≥ 1V/ns.

## Switching Characteristics - DDRI/DDR333 (PC1600, PC2100, PC2700)

(over recommended operating free-air temperature range, unless otherwise noted) (see Figure 1)

SYMBOL	From (Input)	To (Output)	V <sub>DD</sub> = 2.5V ± 0.2V			UNITS
			MIN	TYP	MAX	
f <sub>max</sub>			210			MHz
t <sub>PD</sub>	CLK, CLK# (TSSOP)	Q	1.6	2.1	2.6	ns
	CLK, CLK# (VFQFN[MLF2])	Q	1.6	2.1	2.6	ns
t <sub>phi</sub>	RESET#	Q			3.5	ns

## Switching Characteristics - DDRI-400 (PC3200)

(over recommended operating free-air temperature range, unless otherwise noted) (see Figure 1)

SYMBOL	From (Input)	To (Output)	V <sub>DD</sub> = 2.6V ± 0.1V			UNITS
			MIN	TYP	MAX	
f <sub>max</sub>			210			MHz
t <sub>PD</sub>	(VFQFN[MLF2])	Q	1.1		1.65	ns
t <sub>PDSS</sub>		Q			1.9	ns
t <sub>PD</sub>	CLK, CLK# (TSSOP)	Q	1.1	1.6	1.85	ns
t <sub>phi</sub>	RESET#	Q			3.5	ns

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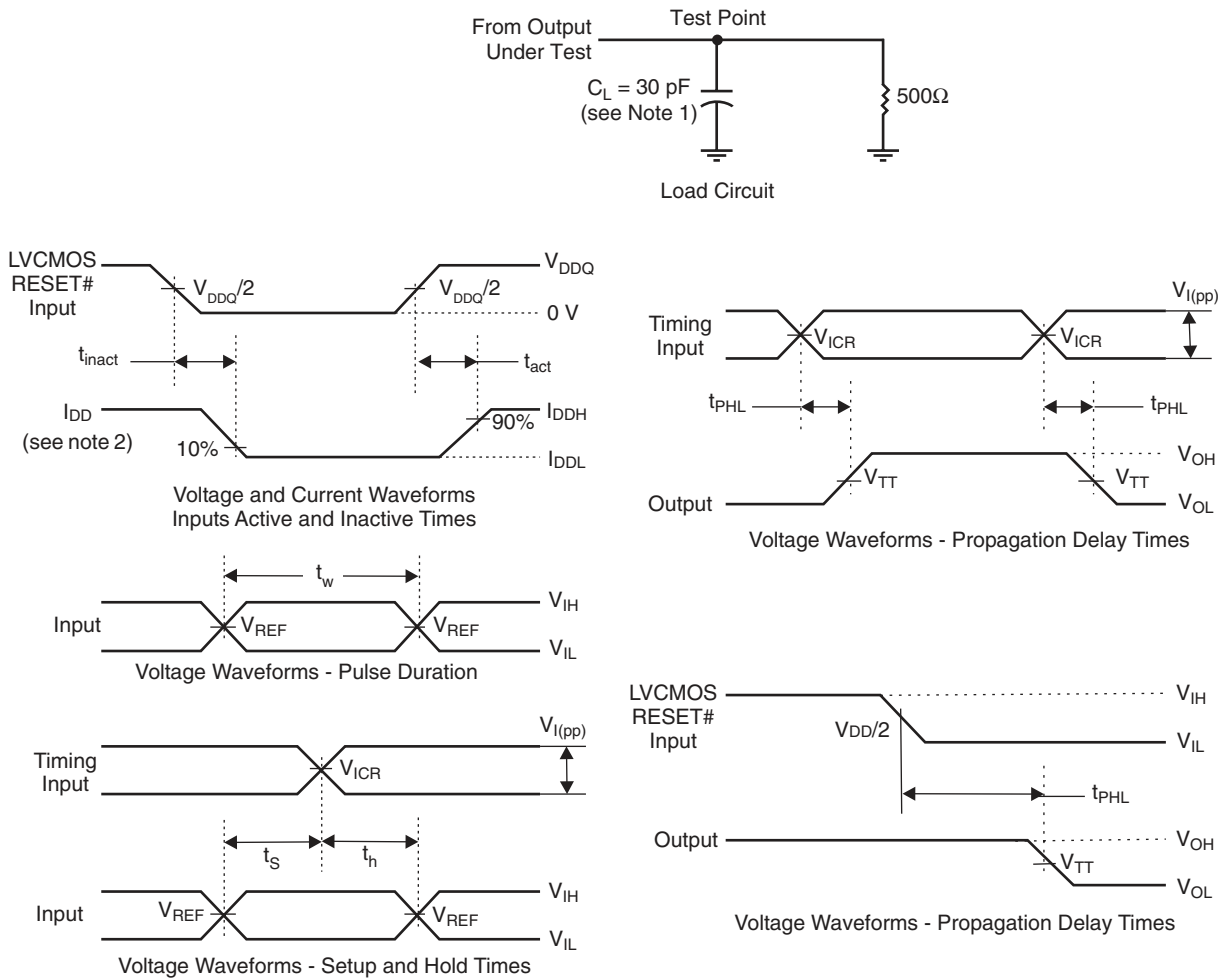
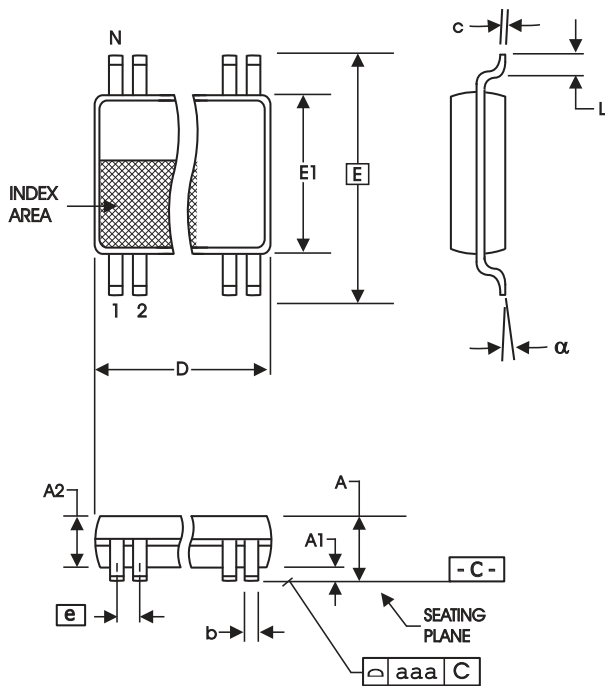


Figure 1 - Parameter Measurement Information ( $V_{DDQ} = 2.5V \pm 0.2V$ )

- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DDQ}$  or GND, and  $I_O = 0$  mA.
  3. All input pulses are supplied by generators having the following characteristics: PRR @ 10 MHz,  $Z_o=50\Omega$ , input slew rate = 1 V/ns  $\pm 20\%$  (unless otherwise specified).
  4. The outputs are measured one at a time with one transition per measurement.
  5.  $V_{TT} = V_{REF} = V_{DDQ}/2$
  6.  $V_{IH} = V_{REF} + 310mV$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DDQ}$  for LVC MOS input.
  7.  $V_{IL} = V_{REF} - 310mV$  (AC voltage levels) for differential inputs.  $V_{IL} = GND$  for LVC MOS input.
  8.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$





**6.10 mm. Body, 0.50 mm. pitch TSSOP**  
**(240 mil) (0.020 mil)**

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	.004

### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

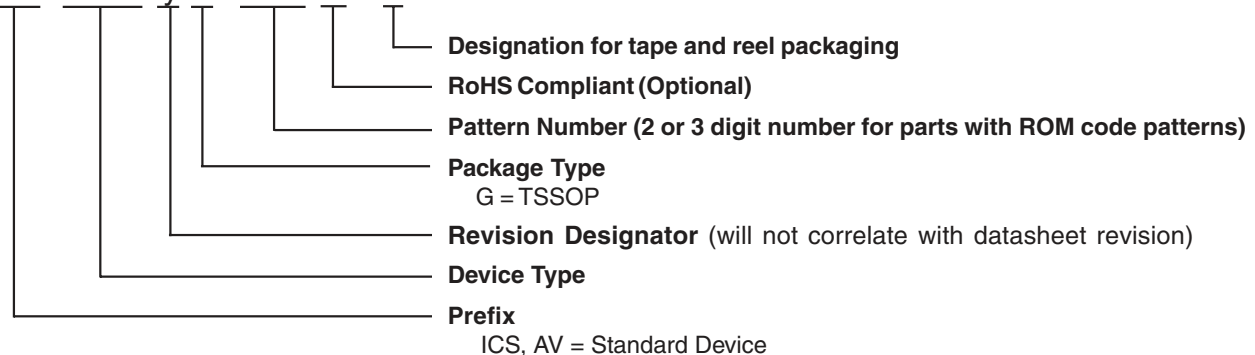
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## Ordering Information

### ICSSSTVA16859CGLF-T

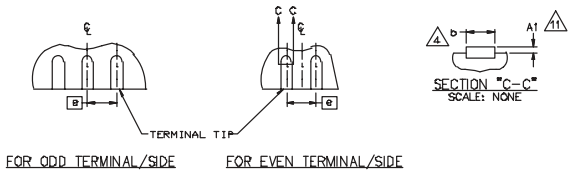
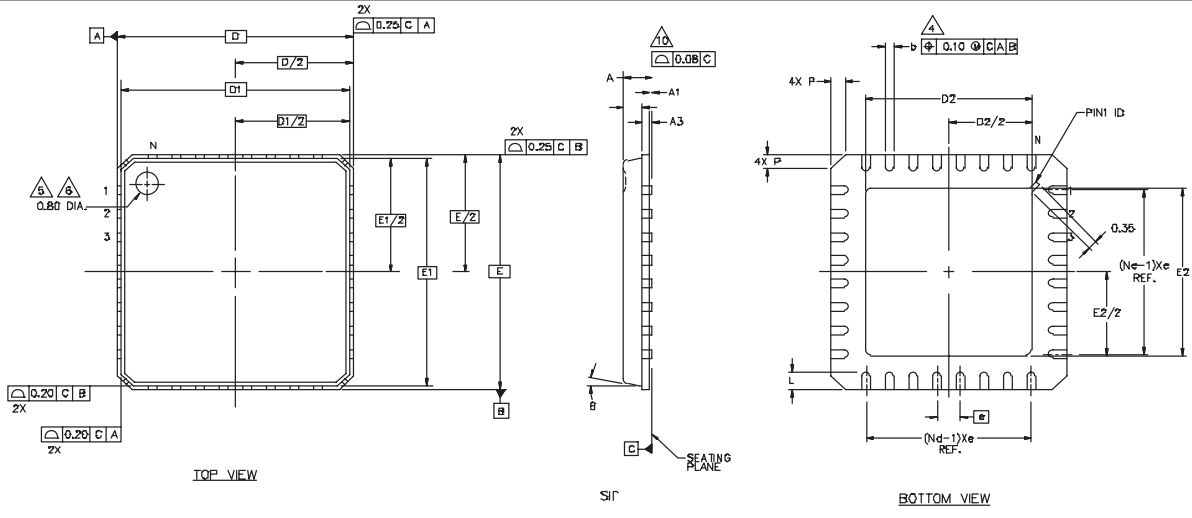
Example:

**ICS XXXX y G - PPP LF - T**



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# ICSSSTVA16859C



## 56 pin MLF2

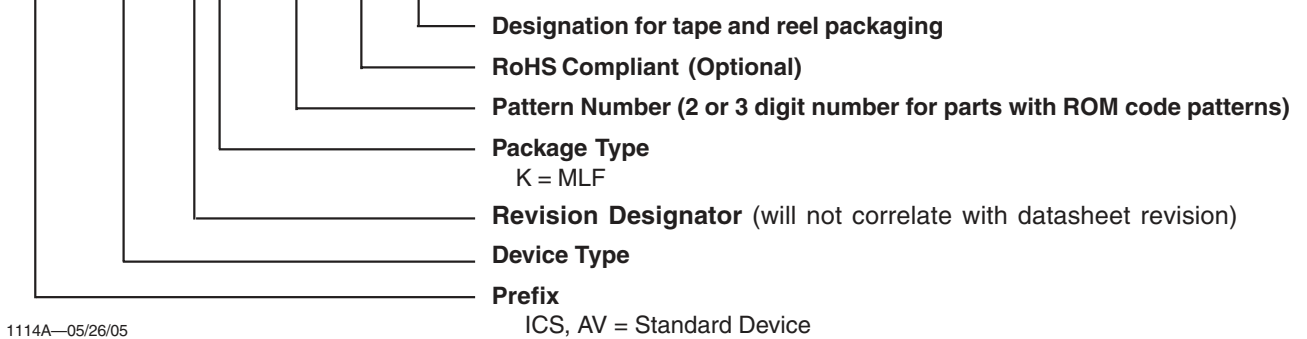
Symbol	Common Dimensions		
A	-	0.85	1.00
A1	0.00	0.01	0.05
A2	-	0.65	0.80
A3	0.20 BSC		
D	8.00 BSC		
D1	7.75 BSC		
E	8.00 BSC		
E1	7.75 BSC		
Θ			12
P	0.24	0.42	0.60
R	0.13	0.17	0.23
<b>Pitch Variation D</b>			
e	0.50 BSC		
N	56		
Nd	14		
Ne	14		
L	0.30	0.40	0.50
b	0.18	0.23	0.30
Q	0.00	0.20	0.45
D2	4.35	4.50	4.65
E2	5.05	5.20	5.35

## Ordering Information

ICSSSTVA16859CKLF-T

Example:

ICS XXXX y K - PPP LF - T



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