LOW SKEW, 1-TO-10, DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL FANOUT BUFFER

ICS853111-02

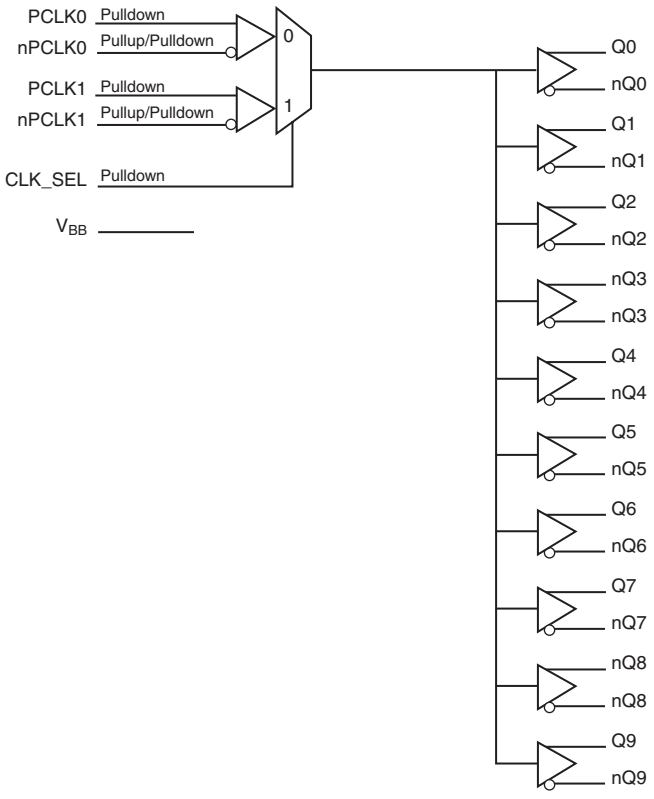
General Description

The ICS853111-02 is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS853111-02 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853111-02 ideal for those clock distribution applications demanding well defined performance and repeatability.

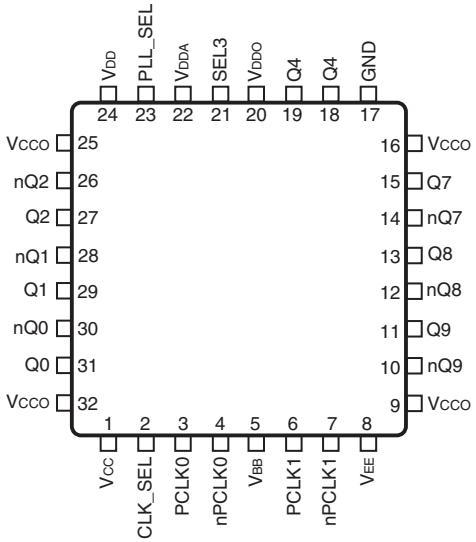
Features

- Ten differential 2.5V, 3.3V LVPECL/ECL outputs
- Two selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 3.2GHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 25ps (typical)
- Part-to-part skew: 85ps (typical)
- Propagation delay: 680ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS853111-02

32-Lead TSSOP, E-Pad
7mm x 7mm x 1mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Positive supply pin.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1/nPCLK1 inputs. When LOW, selects PCLK0/nPCLK0 inputs. LVTTL / LVCMOS interface levels.
3	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
5	V_{BB}	Output		Bias voltage.
6	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
8	V_{EE}	Power		Negative supply pin.
9, 16, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL/ECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL/ECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL/ECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

Function Tables

Table 3A. Clock Input Function Table

Inputs		Outputs			
PCLK0 or PCLK1	**nPCLK0 or nPCLK1**	**Q0:Q9**	**nQ0:nQ9**	**Input to Output Mode**	**Polarity**
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Table 3B. Control Input Function Table

Inputs	
CLK_SEL	**Selected Source**
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
V_{BB} Sink//Source, I_{BB}	± 0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	49.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				85	mA

Table 4B. DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.295	2.33	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage (Single-ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-200			-200			-200			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V

.**Table 4C. LVPECL DC Characteristics,** V_{CC} = 2.5V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.495	1.53	1.565	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage (Single-ended)		1.275		1.56	1.275		1.56	1.275		-0.8	V
V_{IL}	Input Low Voltage (Single-ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-200			-200			-200			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V.

Table 4D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -3.8V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.005	-0.97	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage (Single-ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage (Single-ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.486		-1.386	-1.486		-1.386	-1.486		-1.386	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2		0	V_{EE}+1.2		0	V_{EE}+1.2		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1 nPCLK0, nPCLK1	-200			-200			-200			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V

AC Electrical Characteristics

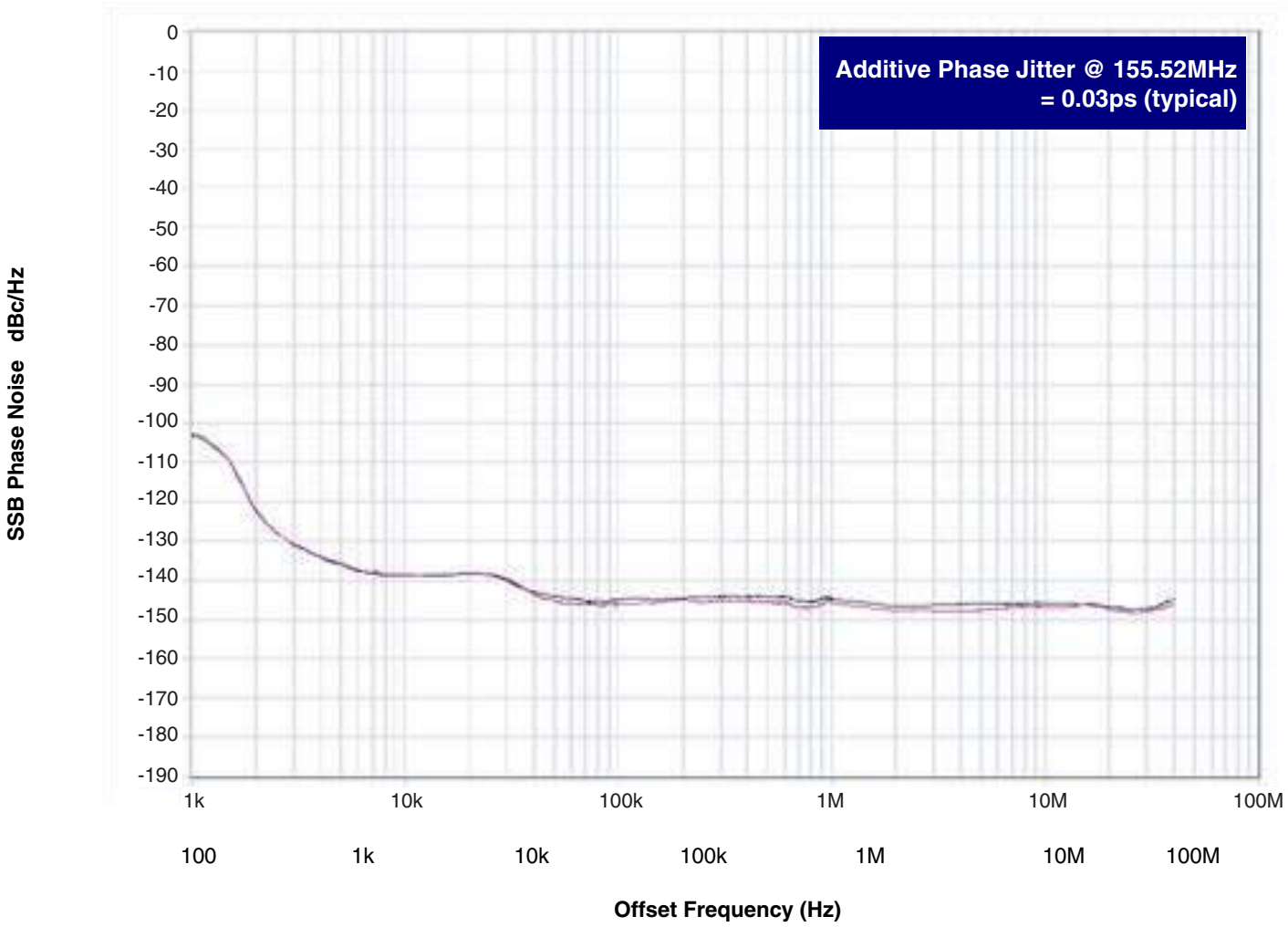
Table 5. AC Characteristics, V_{CC} = -3.8V to -2.375V or , V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency				3.2		3.2				3.2	GHz
t_{PD}	Propagation Delay; NOTE 1		600	680	750	650	725	790	690	790	890	ps
*t*sk(o)	Output Skew; NOTE 2, 4			25	37		25	37		25	37	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			85	225		85	225		85	225	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jjitter Section			0.03			0.03			0.03		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	60	200	325	100	200	280	130	200	270	ps

All parameters are measured at f ≤ 1GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

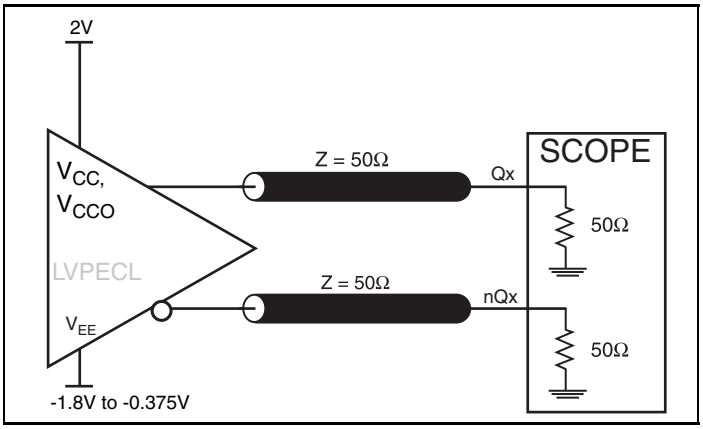
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

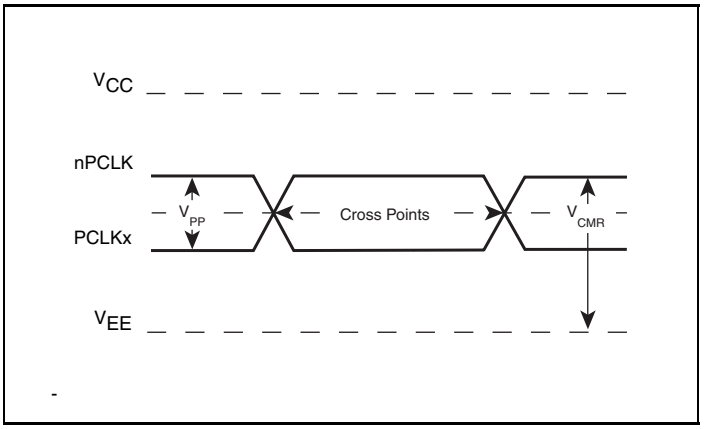


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

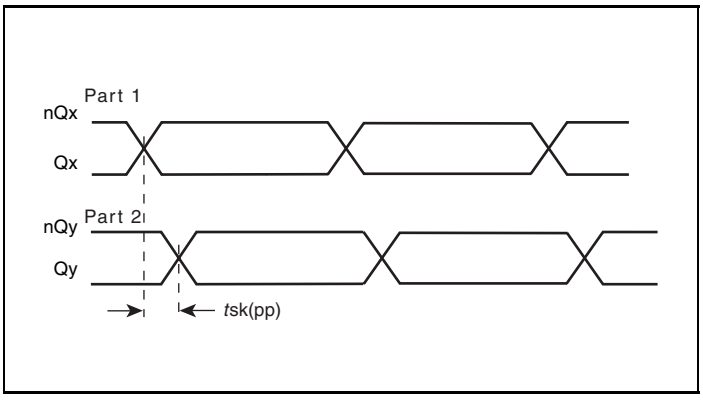
Parameter Measurement Information



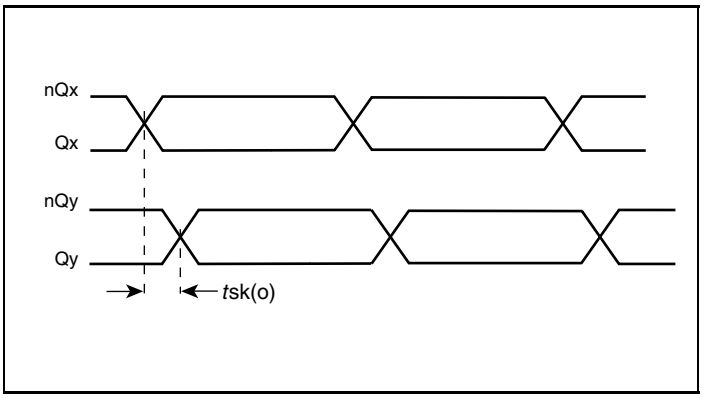
LVPECL Output Load AC Test Circuit



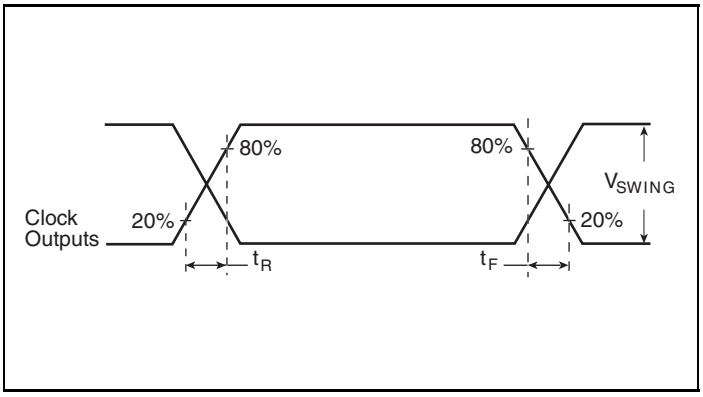
Differential Input Level



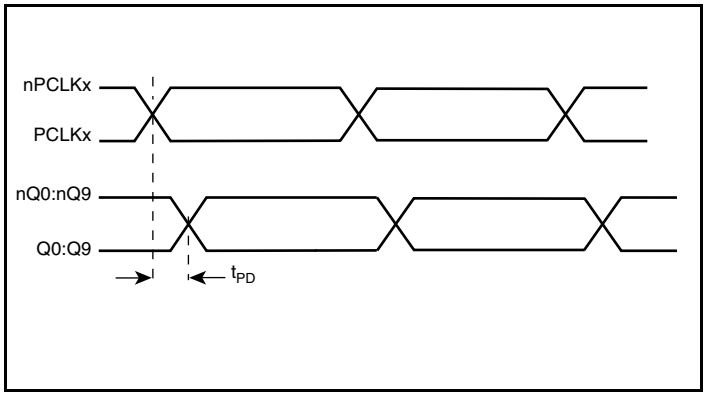
Part-to-Part Skew



Output Skew



Output Rise/Fall Time



Propagation Delay

Application Information

Wiring the Differential Input to Accept Single-ended LVCMOS Levels

Figure 1A shows an example of the differential input that can be wired to accept single-ended LVCMOS levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be loacted as close as possible to the input pin.

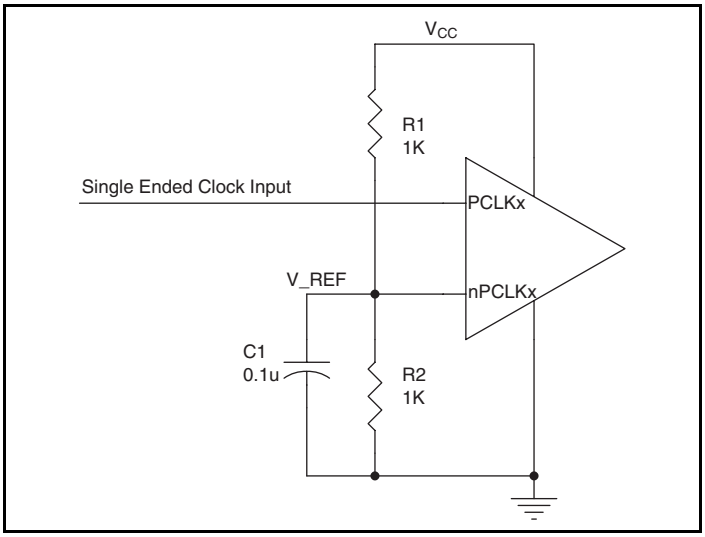


Figure 1A. Single-Ended LVCMOS Signal Driving Differential Input

Wiring the Differential Input to Accept Single-ended LVPECL Levels

Figure 2 shows an example of the differential input that can be wired to accept single-ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be loacted as close as possible to the input pin.

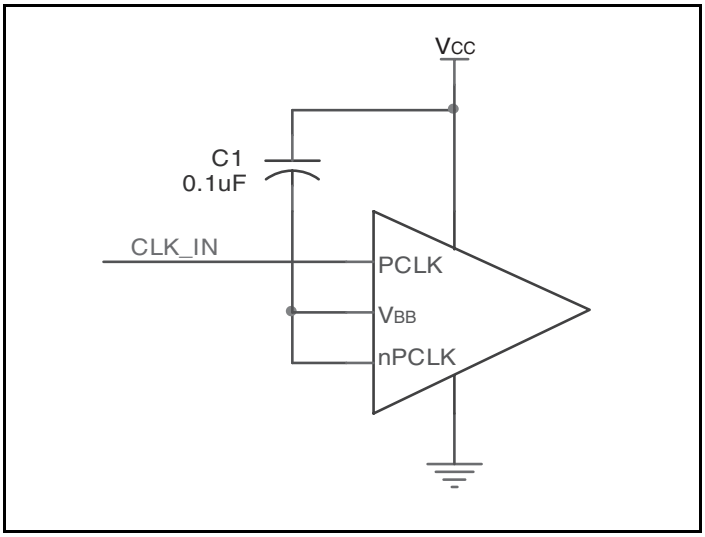


Figure 2. Single-Ended LVPECL Signal Driving Differential Input

LVPECL Clock Input Interface (with VBB)

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

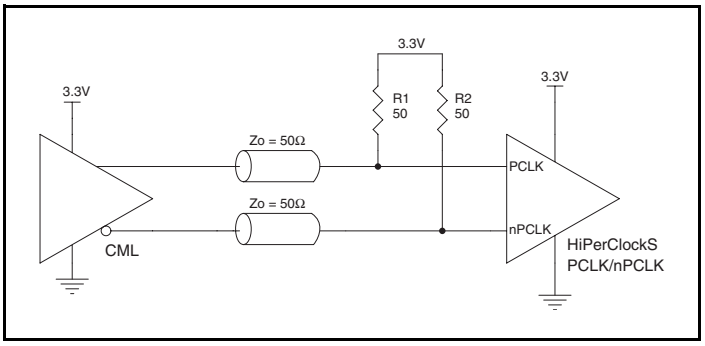


Figure 3A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver

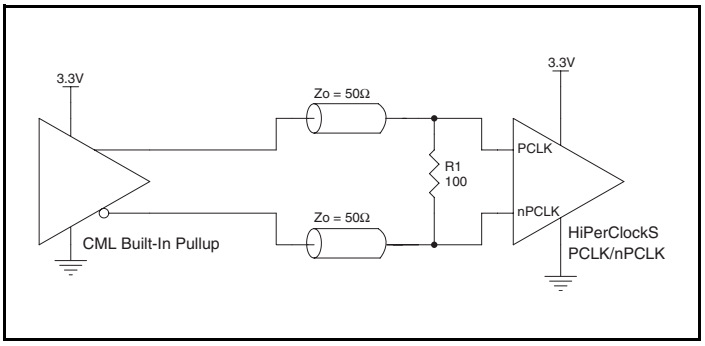


Figure 3B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

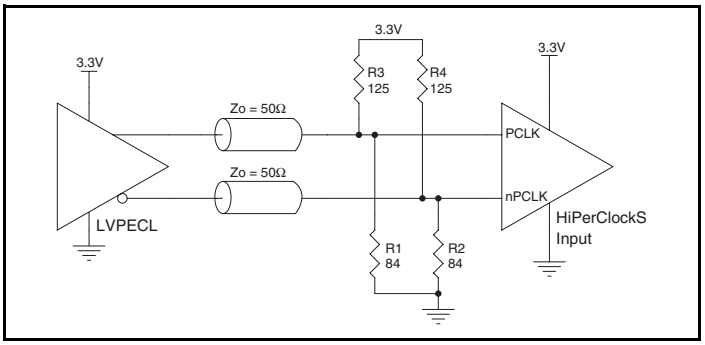


Figure 3C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

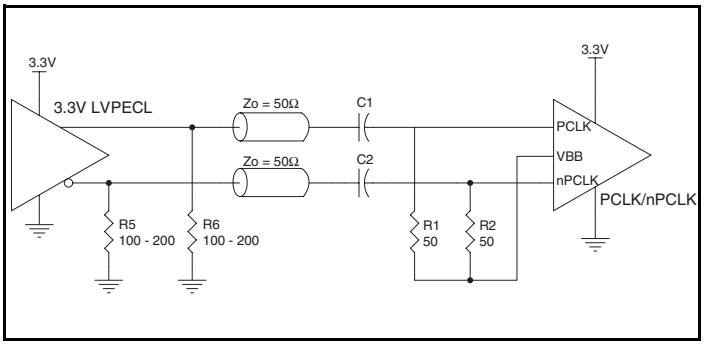


Figure 3D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

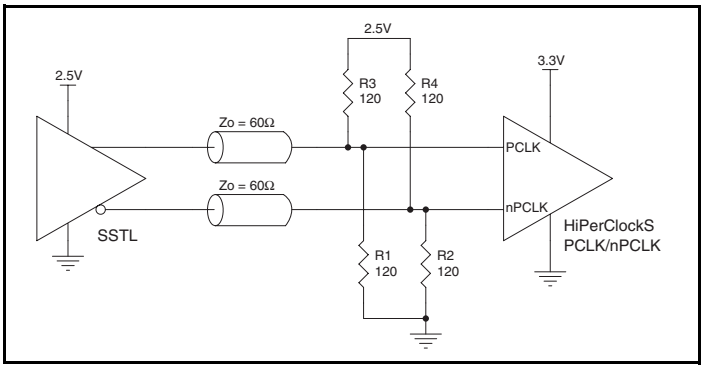


Figure 3E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

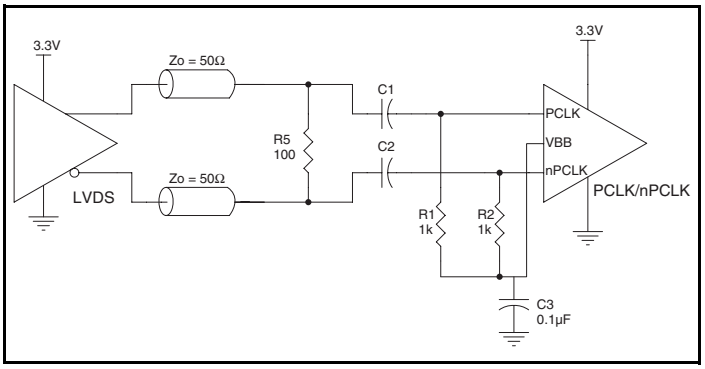


Figure 3F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground. For applications

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

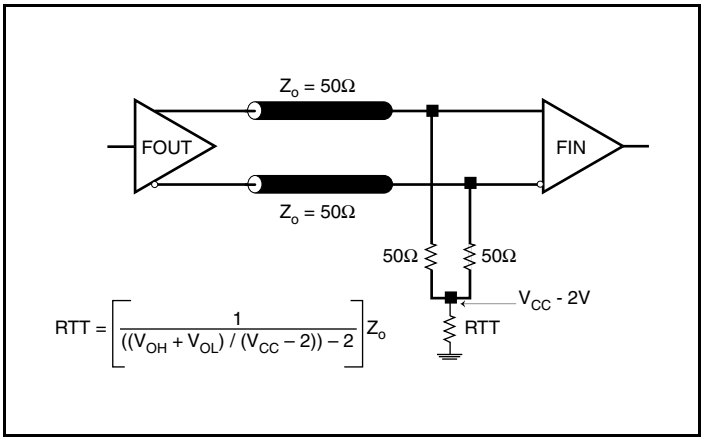


Figure 4A. 3.3V LVPECL Output Termination

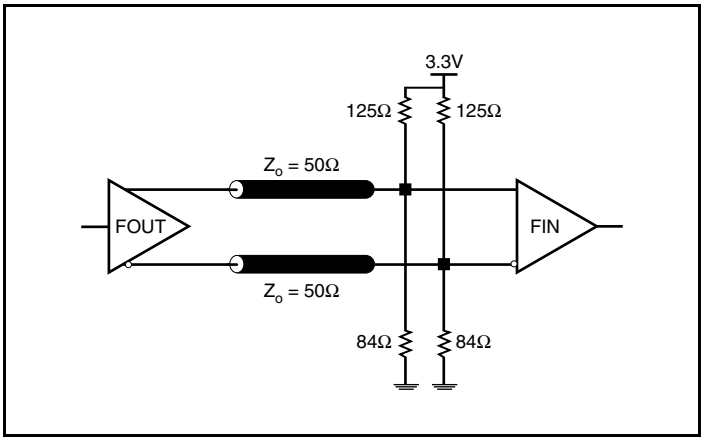


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

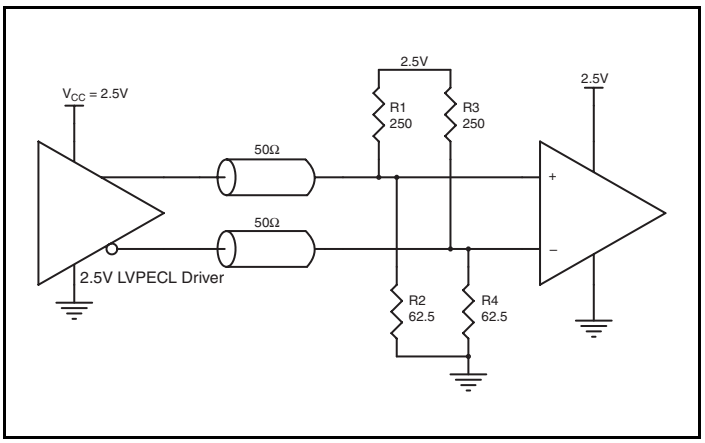


Figure 5A. 2.5V LVPECL Driver Termination Example

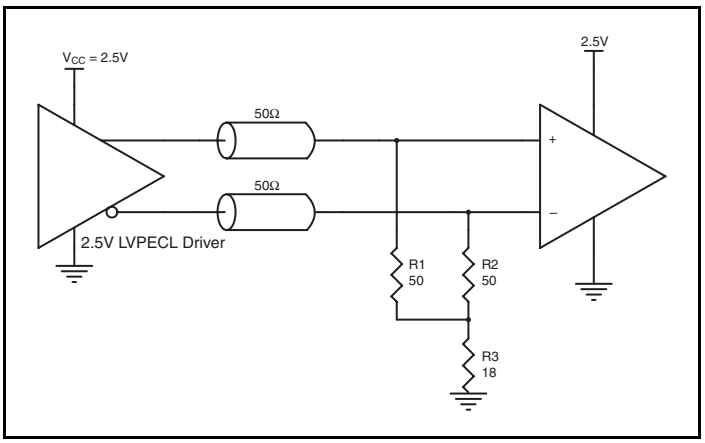


Figure 5B. 2.5V LVPECL Driver Termination Example

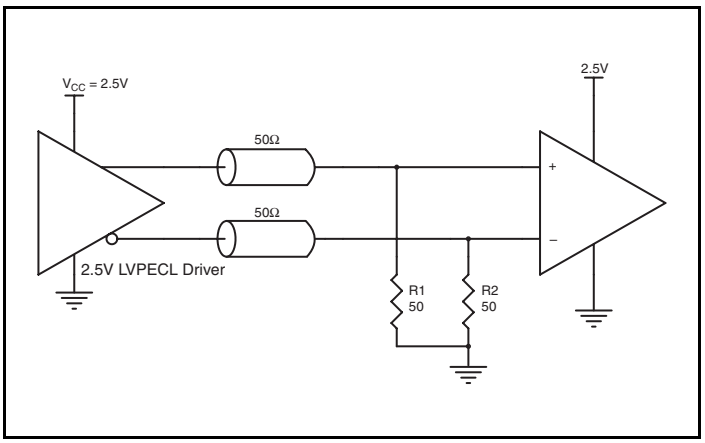


Figure 5C. 2.5V LVPECL Driver Termination Example

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

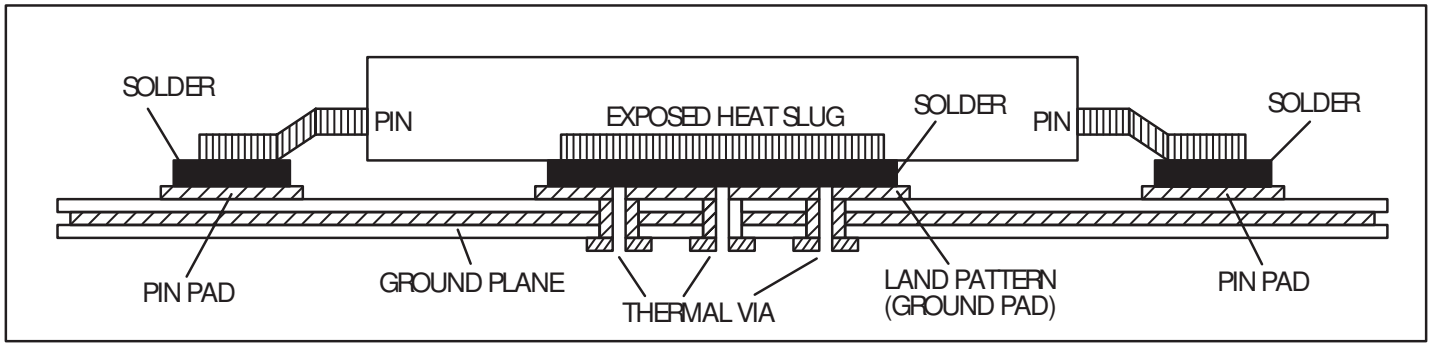


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Example

This application note provides a general design guide using ICS853111-02 LVPECL buffer. *Figure 7* shows a schematic example of the ICS853111-02 LVPECL clock buffer. In this example, the input is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK0/nPCLK0 input.

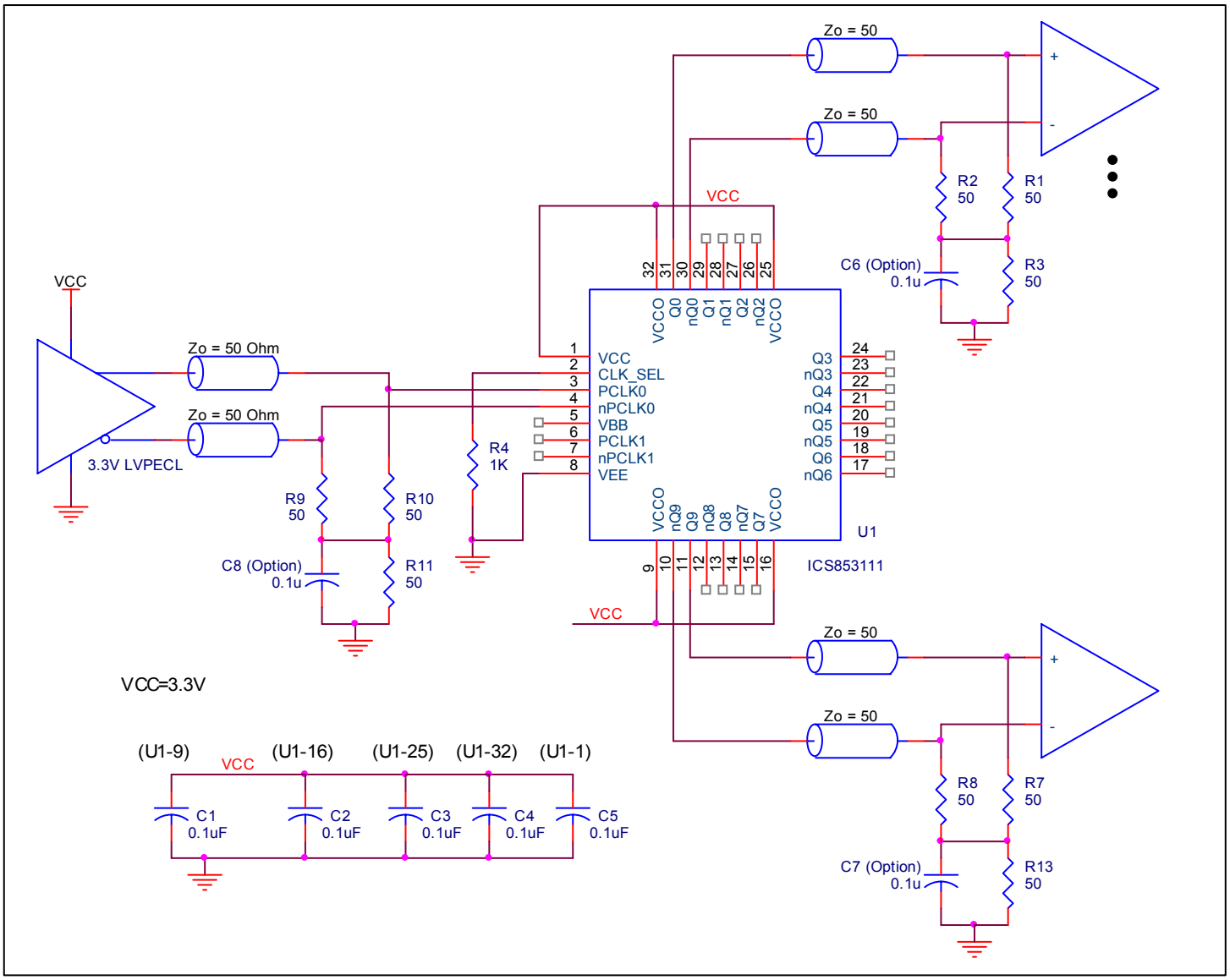


Figure 7. ICS853111-02 Example LVPECL Clock Output Buffer Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853111-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853111-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 85mA = **323mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is10 * 30.94mW = **309.4mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 323mW + 309.4mW = **632.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.632W * 49.5°C/W = 116.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead TQFP, E-Pad Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	69.3°C/W	57.8°C/W	52.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.8°C/W	41.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

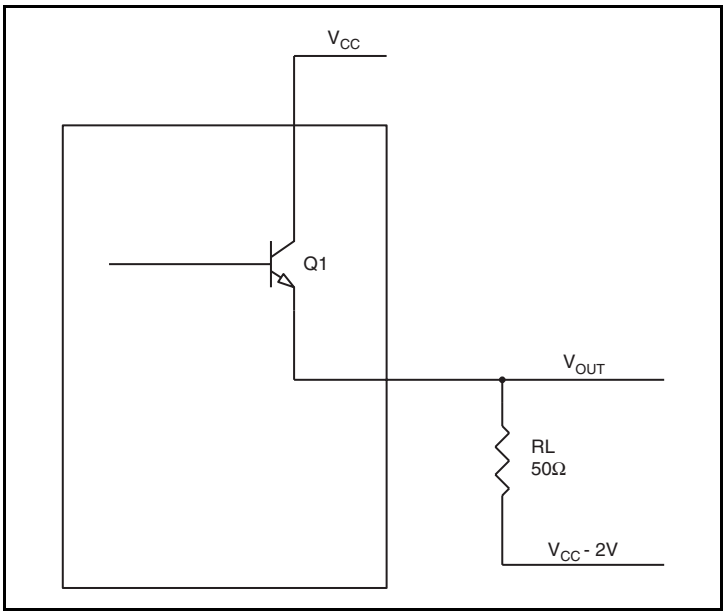


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.935V**
  $(V_{CC\_MAX} – V_{OH\_MAX})$ = **0.935V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.67V**
  $(V_{CC\_MAX} – V_{OL\_MAX})$ = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.935V)/50Ω] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{COC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.67V)/50Ω] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	69.3°C/W	57.8°C/W	52.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.8°C/W	41.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS853111-02 is: 1340
Pin compatible with MC100EP111 and MC100LVEP111

Package Outline and Package Dimensions

Package Outline - G Suffix for 32 Lead TQFP, E-Pad

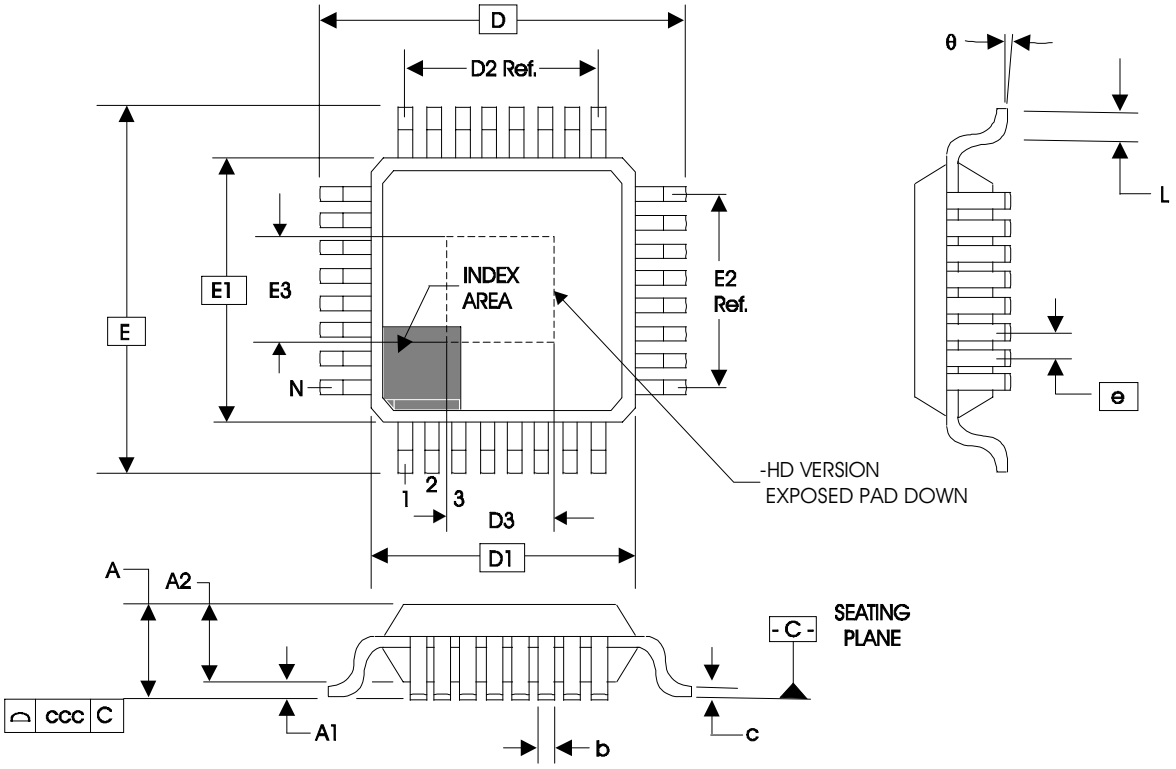


Table 8. Package Dimensions 32 Lead TQFP, E-Pad

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.40
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
D3 & E3	3.0		4.0
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853111AY-02	ICS853111A02	32 Lead TQFP, E-Pad	Tube	-40°C to 85°C
ICS853111AY-02T	ICS853111A02	32 Lead TQFP, E-Pad	1000 Tape & Reel	-40°C to 85°C
ICS853111AY-02LF	ICS853111A02L	“Lead-Free” 32 Lead TQFP, E-Pad	Tube	-40°C to 85°C
ICS853111AY-02LFT	ICS853111A02L	“Lead-Free” 32 Lead TQFP, E-Pad	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		10	Added Recommendations for Unused Input and Output Pins.	1/10/06
	T9	17	Ordering Information Table - added Lead-Free marking.	
B	T4B	5	3.3V LVPECL DC Characteristics - changed I_{IH} max. from 150µA to 200µA. Changed I_{IL} min. from -150µA to -200µA.	2/13/08
	T4C	5	2.5V LVPECL DC Characteristics - changed I_{IH} max. from 150µA to 200µA. Changed I_{IL} min. from -150µA to -200µA.	
	T4D	6	ECL DC Characteristics - changed I_{IH} max. from 150µA to 200µA. Changed I_{IL} min. from -150µA to -200µA.	
		11	Updated LVPECL Clock Input Interface Section.	
		14	Updated EPAD Thermal Release Path Section.	
		16	Power Considerations - updated Junction Temperature equation with worst case thermal resistance of 49.5°C/W.	

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia
Integrated Device Technology
IDT (S) Pte. Ltd.
1 Kallang Sector, #07-01/06
Kolam Ayer Industrial Park
Singapore 349276
+65 67443356
Fax: +65 67441764

Japan
NIPPON IDT KK
Sanbancho Tokyu, Bld. 7F,
8-1 Sanbancho
Chiyoda-ku, Tokyo 102-0075
+81 3 3221 9822
Fax: +81 3 3221 9824

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 37885
idteurope@idt.com

www.IDT.com