

Product Summary

BV _{DSS}	R _{DS(ON)}	I _D T _c = +25°C
-60V	50mΩ @ V _{GS} = -10V	-26A
	70mΩ @ V _{GS} = -4.5V	-22A

Description and Applications

This new generation 60V P-channel enhancement mode MOSFET is designed to minimize R_{DS(ON)} yet maintain superior switching performance. This device is ideal for use in notebook battery power managements and load switches.

- Notebook battery power managements
- DC-DC converters
- Load switches

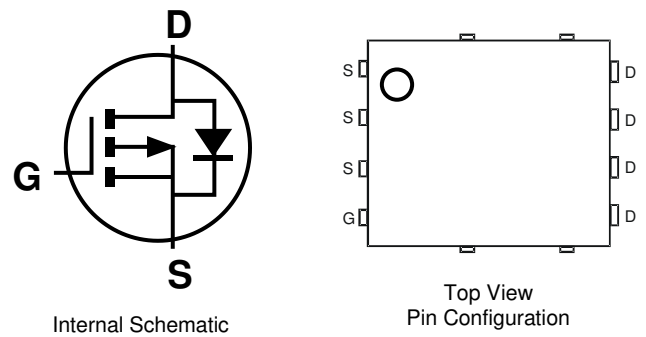
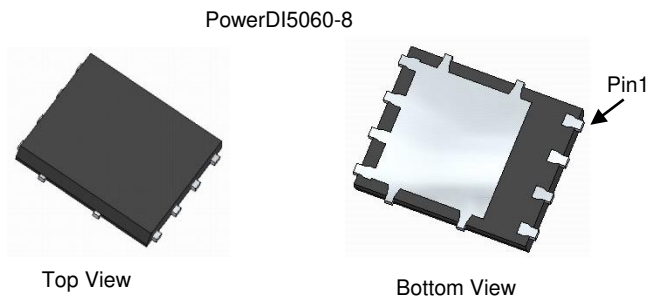
Features and Benefits

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**

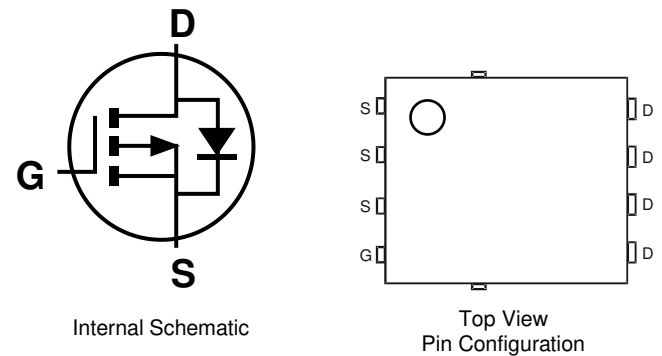
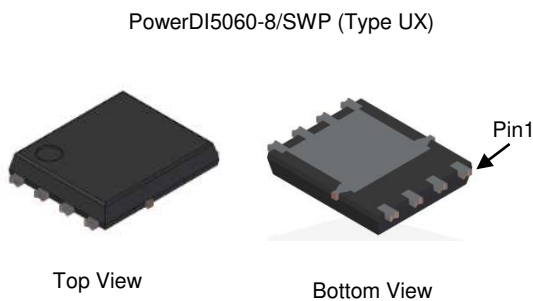
Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, “Green” Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 [Ⓔ]
- Weight: 0.097 grams (Approximate)

Site 1:



Site 2:



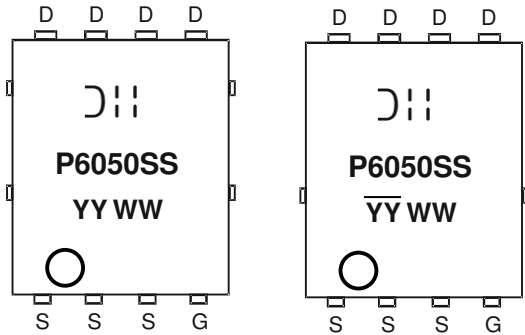
- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP6050SPS-13	PowerDI5060-8	2500	Tape & Reel
DMP6050SPS-13	PowerDI5060-8/SWP (Type UX)	2500	Tape & Reel

Note: 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



= Manufacturer's Marking
 P6050SS = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Last Two Digits of Year (ex: 23 = 2023)
 WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-60	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = -10V	Steady State	T _A = +25°C	I _D	-5.7	A
		T _A = +70°C		-4.5	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	-45	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	-2.4	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I _{SM}	-45	A
Avalanche Current (Note 8) L = 0.1mH			I _{AS}	-25	A
Repetitive Avalanche Energy (Note 8) L = 0.1mH			E _{AS}	32	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	1.3	W
Thermal Resistance, Junction to Ambient @ T _A = +25°C (Note 5)	R _{θJA}	95	°C/W
Power Dissipation (Note 6)	P _D	2.4	W
Thermal Resistance, Junction to Ambient @ T _A = +25°C (Note 6)	R _{θJA}	52	°C/W
Thermal Resistance, Junction to Case @ T _C = +25°C (Note 7)	R _{θJC}	2.4	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	-60	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	μA	V _{DS} = -60V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	-1.0	—	-3.0	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	43	50	mΩ	V _{GS} = -10V, I _D = -5A
		—	53	70		V _{GS} = -4.5V, I _D = -4A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C _{iss}	—	2163	—	pF	V _{DS} = -30V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	88	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	58	—	pF	
Gate Resistance	R _g	—	13	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = -10V)	Q _g	—	30	—	nC	V _{DS} = -30V, I _D = -5A
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	14	—	nC	
Gate-Source Charge	Q _{gs}	—	5	—	nC	
Gate-Drain Charge	Q _{gd}	—	4.6	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	4.7	—	ns	V _{GS} = -10V, V _{DS} = -30V, R _G = 3Ω, I _D = -5A
Turn-On Rise Time	t _R	—	2.7	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	73	—	ns	
Turn-Off Fall Time	t _F	—	25	—	ns	
Body Diode Reverse Recovery Time	t _{RR}	—	18	—	ns	I _F = -5A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{RR}	—	12	—	nC	I _F = -5A, di/dt = 100A/μs

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

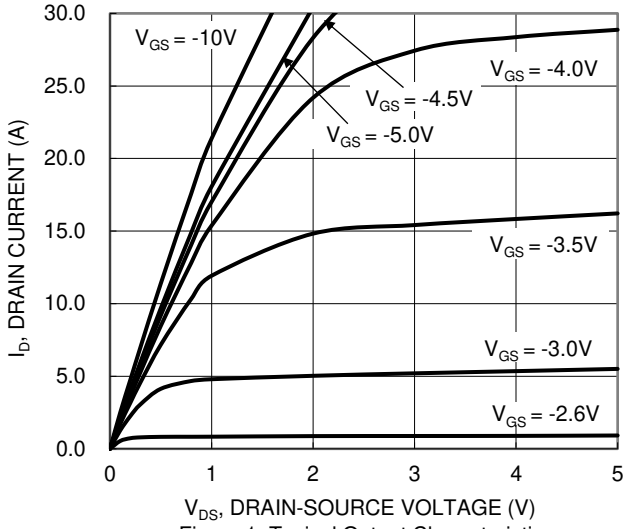


Figure 1. Typical Output Characteristic

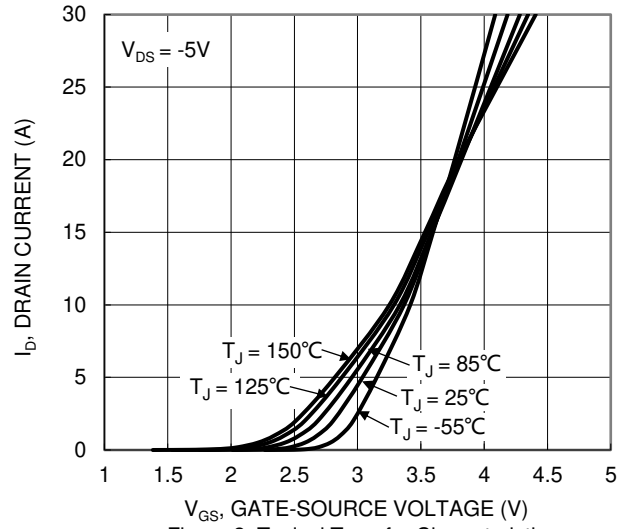


Figure 2. Typical Transfer Characteristic

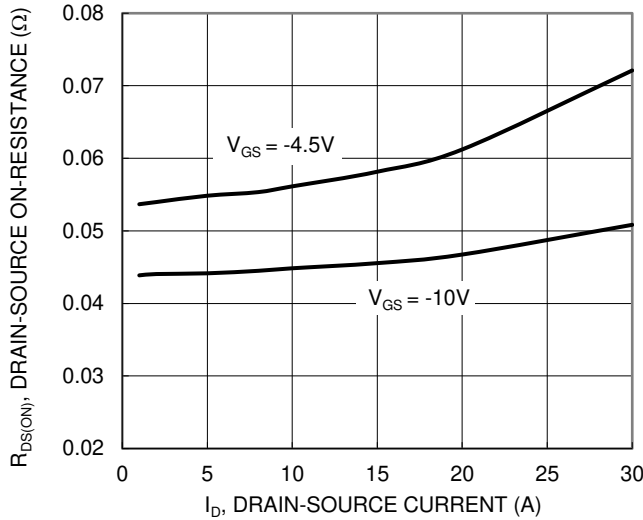


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

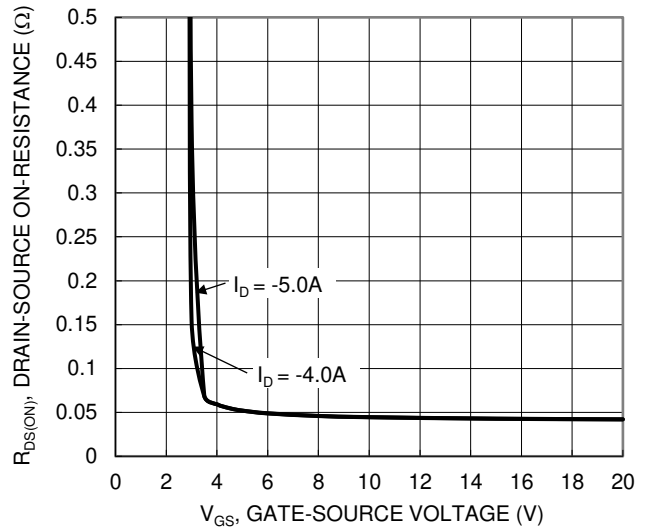


Figure 4. Typical Transfer Characteristic

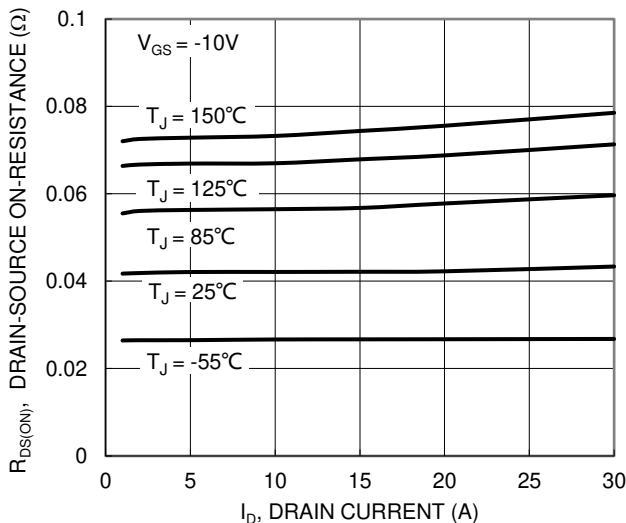


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

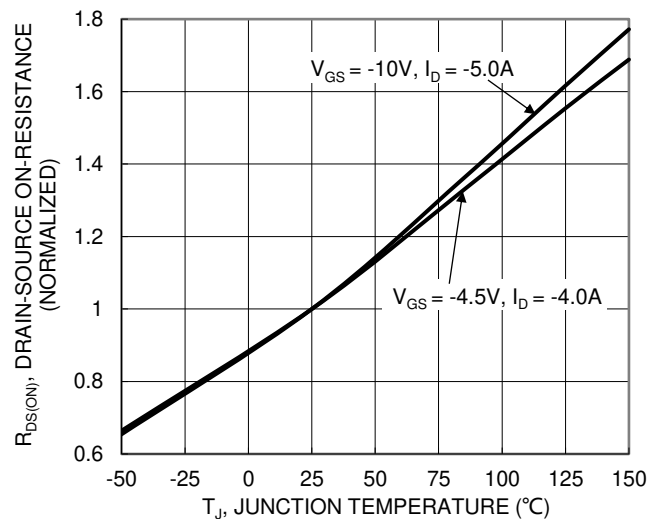


Figure 6. On-Resistance Variation with Junction Temperature

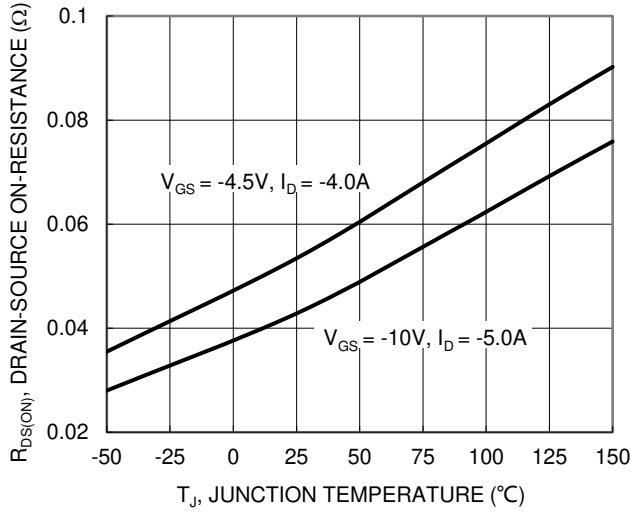


Figure 7. On-Resistance Variation with Junction Temperature

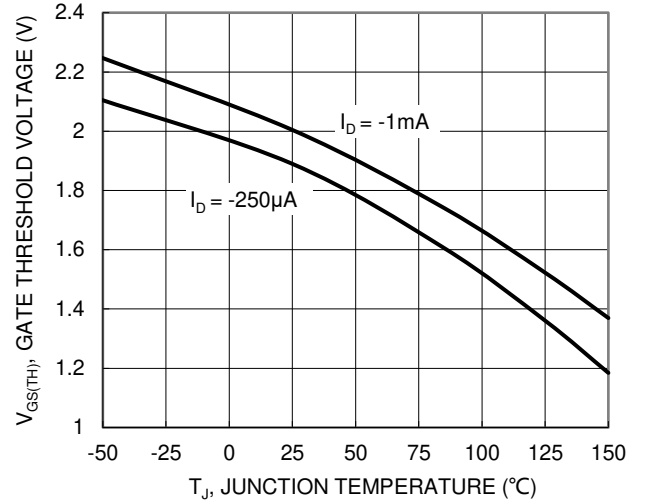


Figure 8. Gate Threshold Variation vs. Junction Temperature

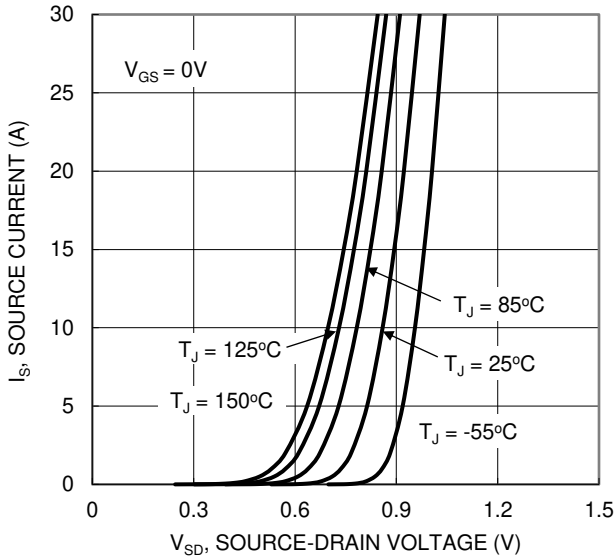


Figure 9. Diode Forward Voltage vs. Current

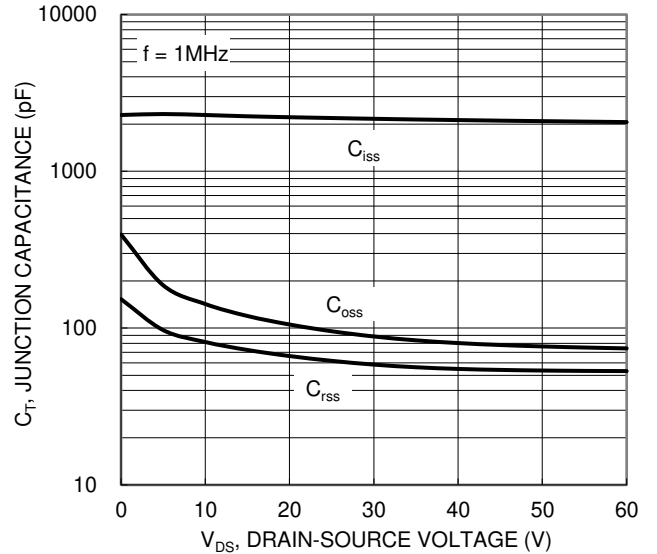


Figure 10. Typical Junction Capacitance

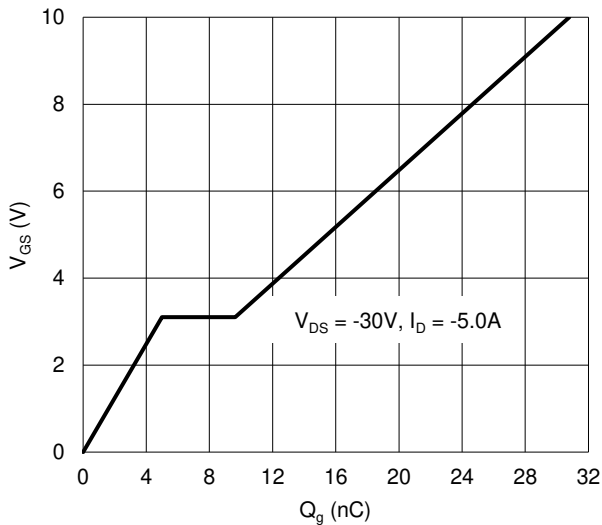


Figure 11. Gate Charge

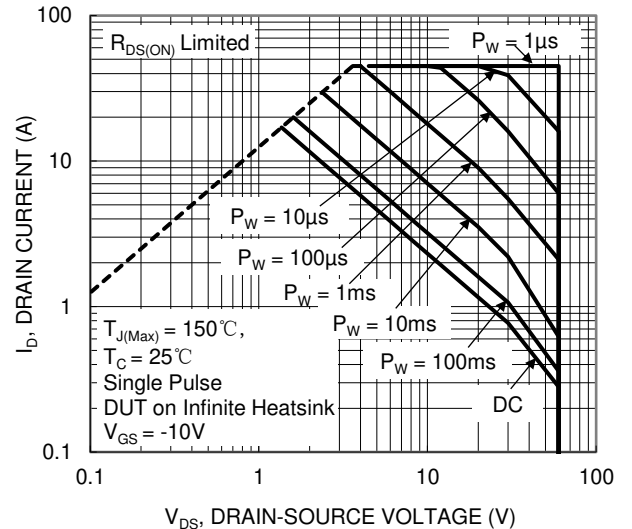


Figure 12. SOA, Safe Operation Area

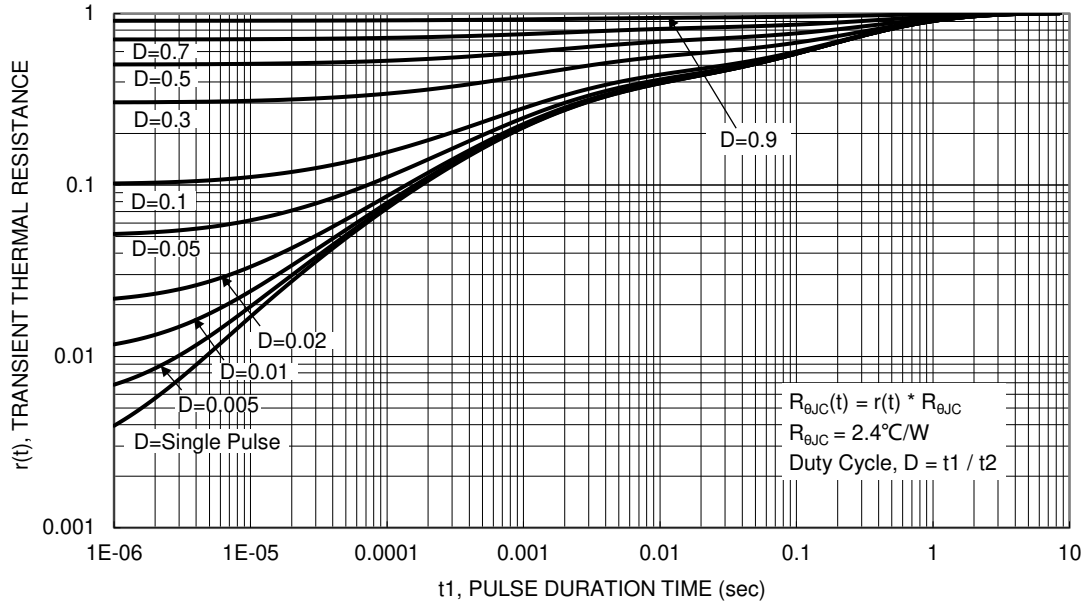


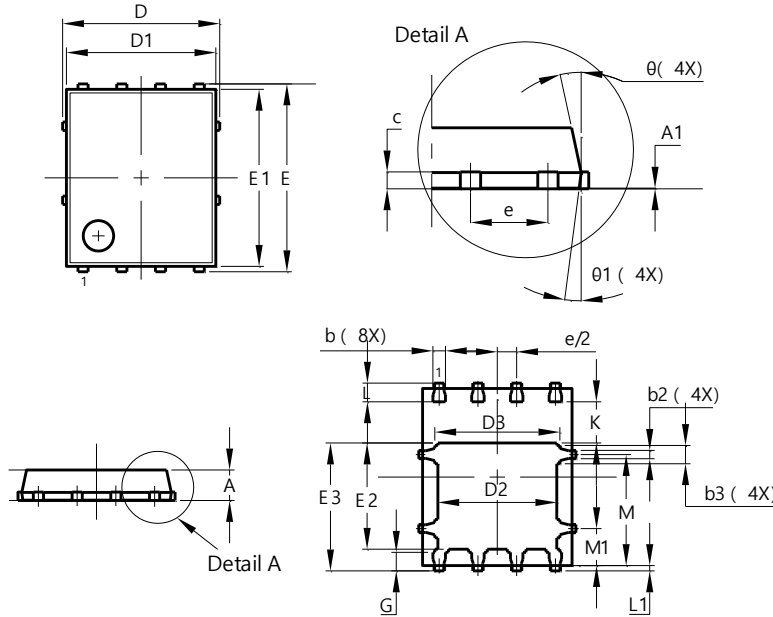
Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

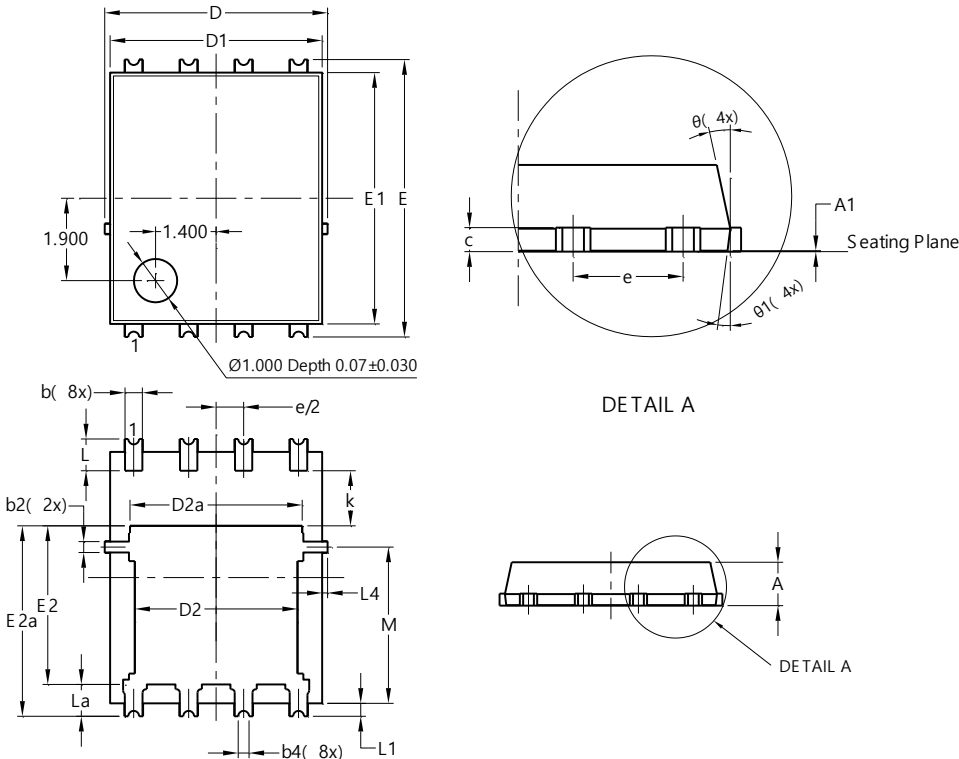
PowerDI5060-8



PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
theta	10°	12°	11°
theta1	6°	8°	7°
All Dimensions in mm			

Site 2:

PowerDI5060-8/SWP (Type UX)



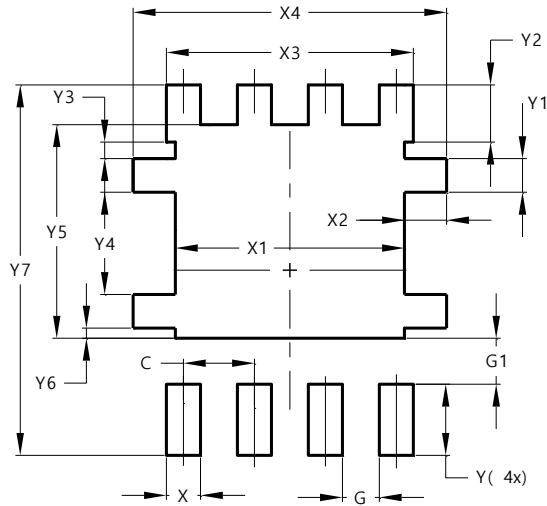
PowerDI5060-8/SWP (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
theta	10°	12°	11°
theta1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

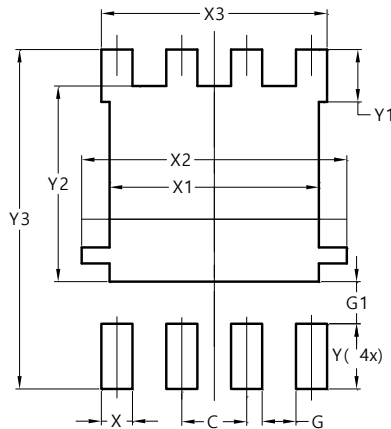
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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