TPS206x-Q1 Current-Limited Power-Distribution Switches

1 Features

- Qualified for Automotive Applications
- 70-mΩ High-Side MOSFET
- 1-A Continuous Current
- Thermal and Short-Circuit Protection
- Accurate Current Limit (1.1-A Minimum, 2.1-A Maximum)
- Operating Range: 2.7 V to 5.5 V
- 0.6-ms Typical Rise Time
- Undervoltage Lockout
- Deglitched Fault Report ($\overline{OC}$)
- No $\overline{OC}$ Glitch During Power Up
- 1-μA Maximum Standby Supply Current
- Bidirectional Switch
- Built-in Soft Start
- UL Recognized Under File No. E166910
- Ambient Temperature Range: –40°C to 125°C

2 Applications

- Power Distribution and Switching
- Heavy Capacitive Loads
- Short-Circuit Protections

3 Description

The TPS206x-Q1 power-distribution switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

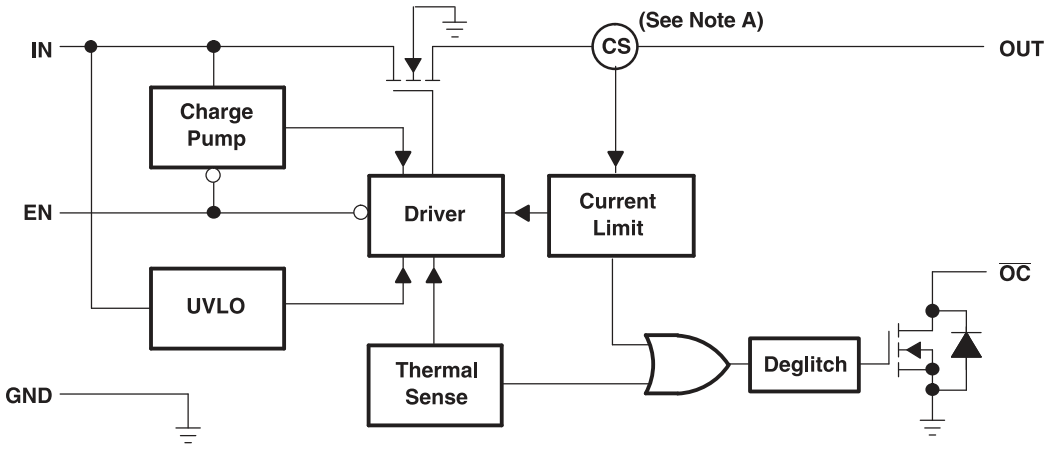
When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$x) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5 A (typically).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS206x-Q1	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS2065-Q1 Functional Block Diagram



A. Current sense

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2012) to Revision C — **Page**

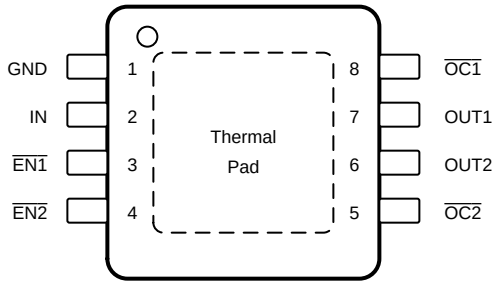
- Added *ESD Ratings* table, *Feature Description* section, *Thermal Information* table, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Current Limit max from 1.9 A at T_A = 25°C to 2.1 A across full T_A range in *Features* ... 1
- Changed *UL Listed* to *UL Recognized Under* in *Features* ... 1
- Removed the *General Switch Catalog* image from the front page ... 1
- Removed *Ordering Information* table, see POA at the end of the document ... 3
- Changed pin 4 name from *EN or* $\overline{EN}$ to *EN* under the TPS2065-Q1 pinout to reflect the correct pin name for that specific part instead of the EN and $\overline{EN}$ options from the TPS206x family ... 4

Changes from Revision A (November 2011) to Revision B — **Page**

- Changed Pin Out drawing to include EN. ... 1
- Added "or EN" to *Electrical Characteristics* table. ... 5

5 Pin Configuration and Functions

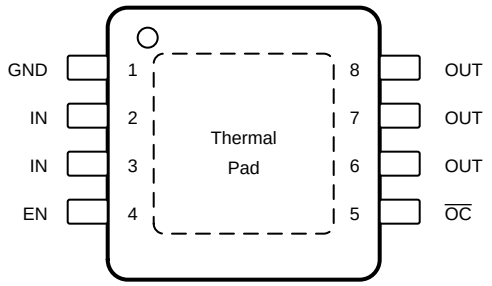
TPS2062-Q1 DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions: TPS2062-Q1

PINS		TYPE	DESCRIPTION
NAME	NO.		
$\overline{EN1}$	3	I	Enable input, logic low (active low) turns on power switch IN-OUT1
$\overline{EN2}$	4	I	Enable input, logic low (active low) turns on power switch IN-OUT2
GND	1	GND	Ground
IN	2	PWR	Supply Input voltage
$\overline{OC1}$	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	O	Power-switch output, IN-OUT1
OUT2	6	O	Power-switch output, IN-OUT2
Thermal Pad	—	GND	Internally connected to GND; used to heat-sink the part to the circuit board ground plane, also calledPowerPAD™ or exposed thermal pad. Must be connected to GND pin.

TPS2065-Q1 DGN Package
8-Pin HVSSOP
Top View



Pin Functions: TPS2065-Q1

PINS		TYPE	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input, logic high (active high) turns on power switch IN-OUT
GND	1	GND	Ground
IN	2, 3	PWR	Supply Input voltage
$\overline{OC}$	5	O	Overcurrent, open-drain output, active low, IN-OUT
OUT	6, 7, 8	O	Power-switch output, IN-OUT
Thermal Pad	—	GND	Internally connected to GND; used to heat-sink the part to the circuit board ground plane, also called PowerPAD™ or exposed thermal pad. Must be connected to GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$(2)	–0.3	6	V
Output voltage(2), $V_{O(OUTx)}$	–0.3	6	V
Input voltage, $V_{I(\overline{ENx})}$	–0.3	6	V
Voltage, $V_{I(\overline{OCx})}$	–0.3	6	V
Continuous output current, $I_{O(OUTx)}$	Internally limited		
Continuous total power dissipation	See *Dissipation Ratings*		
Operating virtual junction temperature range, T_J	–40	150	°C
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM)	±100	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	1	A
Ambient temperature, T_A	–40	125	°C
Operating virtual junction temperature, T_J	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS2062-Q1 DGN (MSOP-PowerPAD) 8 PINS	TPS2065-Q1 DGN (MSOP-PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65	57.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	38.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.9	38.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.7	10.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(\overline{ENx})}$ = 0 V for TPS2062-Q1 or $V_{I(EN)}$ = 5.5 V for TPS2065-Q1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(ON)}$	Static drain-source ON-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 1 A, –40°C ≤ T_A ≤ 125°C			70	135	mΩ
	Static drain-source ON-state resistance, 2.7-V operation(2)	$V_{I(IN)}$ = 2.7 V, I_O = 1 A, –40°C ≤ T_A ≤ 125°C			75	150	mΩ
t_r	Rise time, output	C_L = 1 µF, R_L= 5 Ω, T_A = 25°C	$V_{I(IN)}$ = 5.5 V		0.6	1.5	ms
			$V_{I(IN)}$ = 2.7 V		0.4	1	
t_f	Fall time, output	C_L = 1 µF, R_L= 5 Ω, T_A = 25°C	$V_{I(IN)}$ = 5.5 V	0.05		0.5	ms
			$V_{I(IN)}$ = 2.7 V	0.05		0.5	
ENABLE INPUT $\overline{EN}$ OR EN							
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V		2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V				0.8	
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V		–1		1	µA
t_{ON}	Turnon time	C_L = 100 µF, R_L= 5 Ω				3	ms
t_{off}	Turnoff time	C_L = 100 µF, R_L= 5 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit output current(1)	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short-circuit	T_A = 25°C	1.1	1.5	1.9	A
			–40°C ≤ T_A ≤ 125°C	1.1	1.5	2.1	
I_{OC_TRIP}	Overcurrent trip threshold	$V_{I(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT		1.6	2.3	2.9	A

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design.

Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(\overline{ENx})}$ = 0 V for TPS2062-Q1 or $V_{I(EN)}$ = 5.5 V for TPS2065-Q1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
SUPPLY CURRENT (TPS2062-Q1)						
Supply current, low-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V	T_A = 25°C		0.5	1	µA
		–40°C ≤ T_A ≤ 125°C		0.5	5	
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V	T_A = 25°C		50	70	µA
		–40°C ≤ T_A ≤ 125°C		50	90	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V	–40°C ≤ T_A ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, IN = ground	T_A = 25°C		0.2		µA
SUPPLY CURRENT (TPS2065-Q1)						
Supply current, low-level output	No load on OUT, $V_{I(EN)}$ = 0 V	T_A = 25°C		0.5	1	µA
		–40°C ≤ T_A ≤ 125°C		0.5	5	
Supply current, high-level output	No load on OUT, $V_{I(EN)}$ = 5.5 V	T_A = 25°C		43	60	µA
		–40°C ≤ T_A ≤ 125°C		43	70	
Leakage current	OUT connected to ground, $V_{I(EN)}$ = 0 V	–40°C ≤ T_A ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, IN = ground	T_A = 25°C		0		µA
UNDERVOLTAGE LOCKOUT						
Low-level input voltage, IN			2		2.5	V
Hysteresis, IN	T_A = 25°C			75		mV
OVERCURRENT $\overline{OC1}$ AND $\overline{OC2}$						
Output low voltage, $V_{OL(OCx)}$	$I_{O(\overline{OCx})}$ = 5 mA				0.4	V
Off-state current	$V_{O(\overline{OCx})}$ = 5 V or 3.3 V				1	µA
$\overline{OC}$ deglitch[2]	$\overline{OCx}$ assertion or deassertion		4	8	15	ms
THERMAL SHUTDOWN[3]						
Thermal shutdown threshold			135			°C
Recovery from thermal shutdown			125			°C
Hysteresis				10		°C

(3) The thermal shutdown only reacts under overcurrent conditions.

6.6 Dissipation Ratings

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DGN-8	2.14 W	17.123 mW/°C	428 mW

6.7 Typical Characteristics

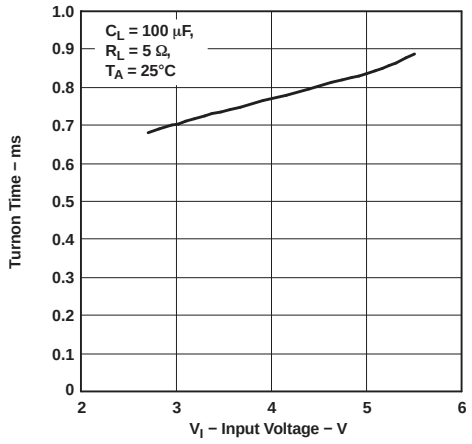


Figure 1. Turnon Time vs Input Voltage

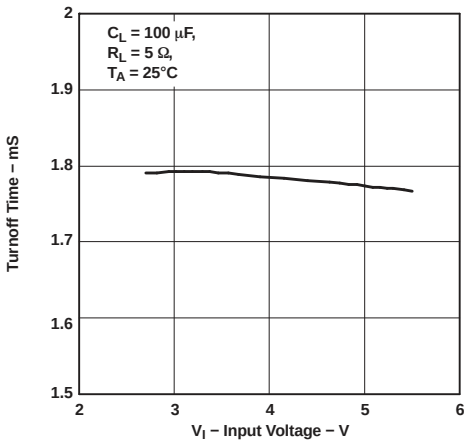


Figure 2. Turnoff Time vs Input Voltage

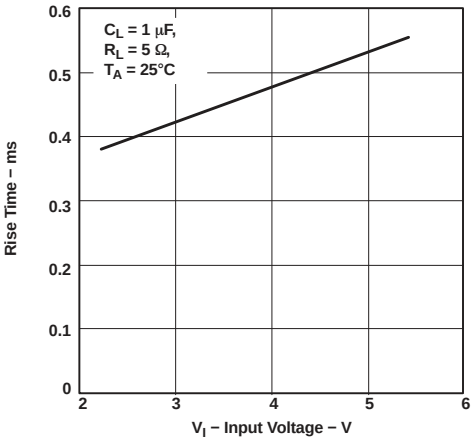


Figure 3. Rise Time vs Input Voltage

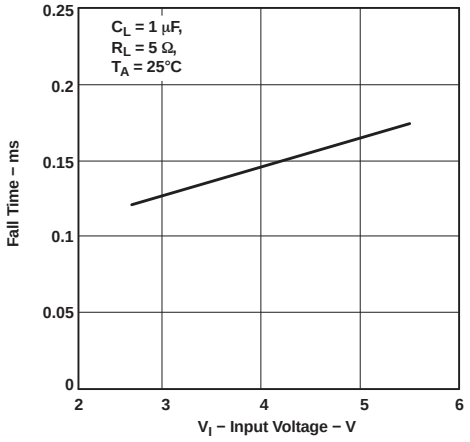


Figure 4. Fall Time vs Input Voltage

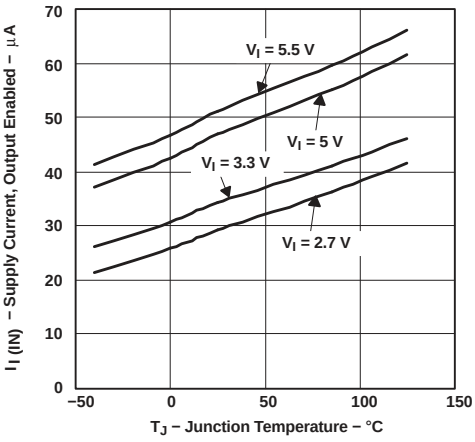


Figure 5. TPS2062-Q1 Supply Current, Output Enabled vs Junction Temperature

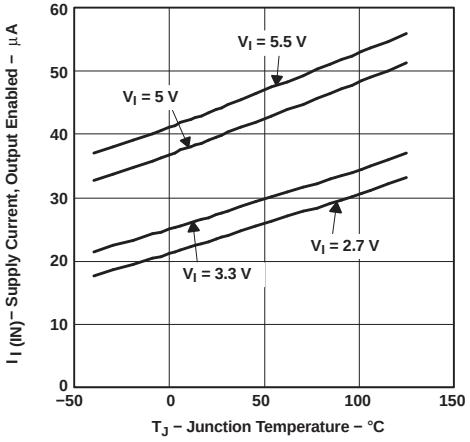


Figure 6. TPS2065-Q1 Supply Current, Output Enabled vs Junction Temperature

Typical Characteristics (continued)

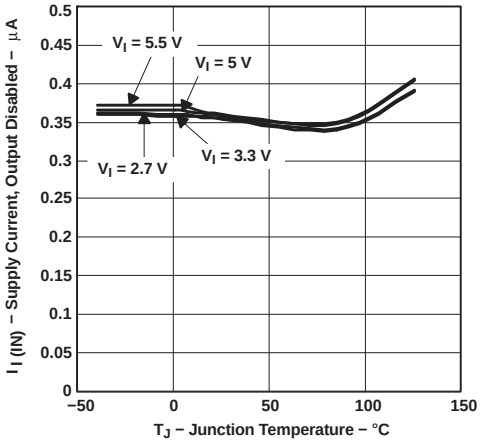


Figure 7. TPS2062-Q1 Supply Current, Output Disabled vs Junction Temperature

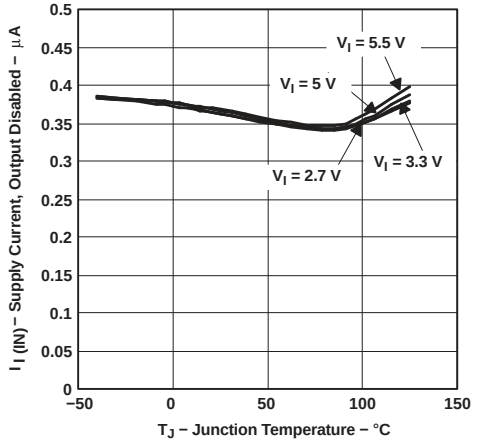


Figure 8. TPS2065-Q1 Supply Current, Output Disabled vs Junction Temperature

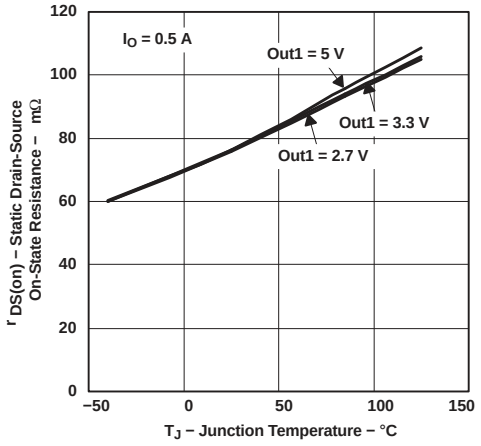


Figure 9. Static Drain-Source ON-State Resistance vs Junction Temperature

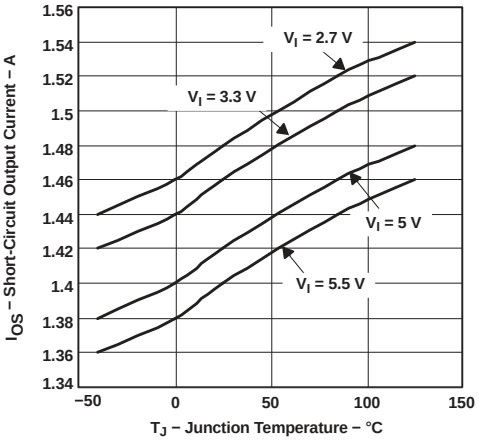


Figure 10. Short-Circuit Output Current vs Junction Temperature

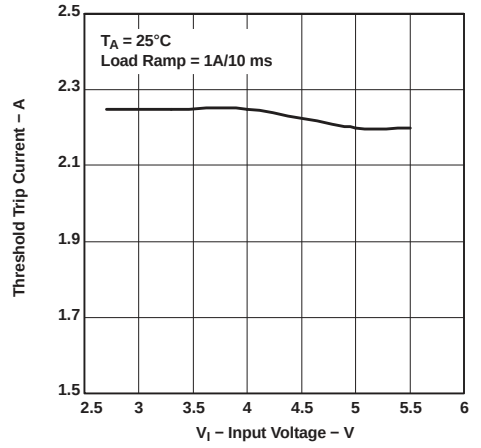


Figure 11. Threshold Trip Current vs Input Voltage

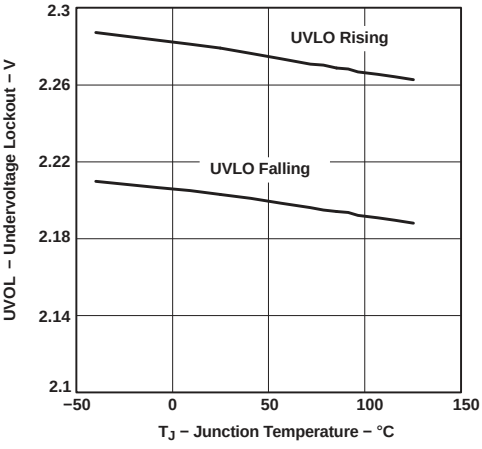


Figure 12. Undervoltage Lockout vs Junction Temperature

Typical Characteristics (continued)

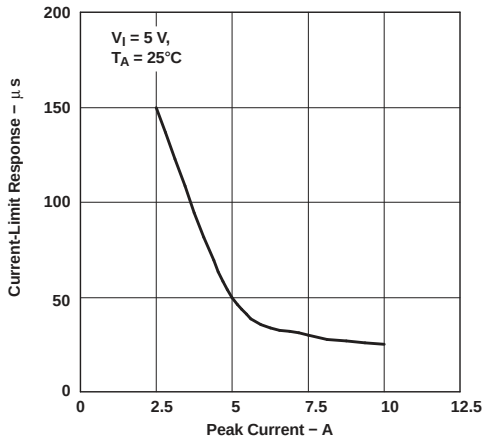


Figure 13. Current-Limit Response vs Peak Current

7 Parameter Measurement Information

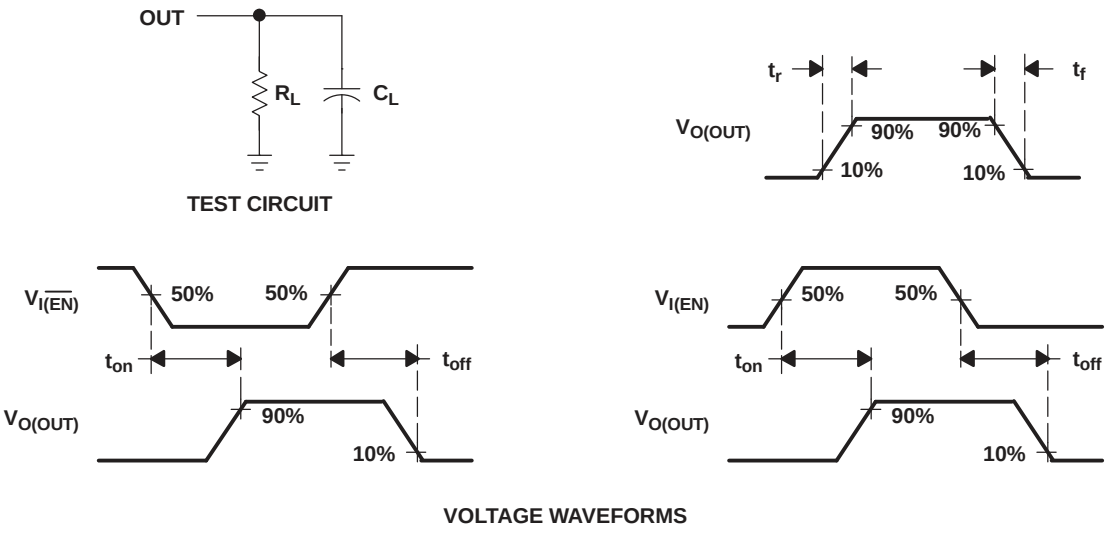


Figure 14. Test Circuit and Voltage Waveforms

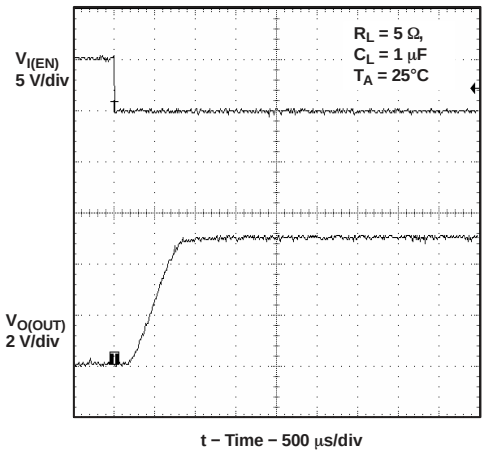


Figure 15. Turnon Delay and Rise Time With 1-µF Load

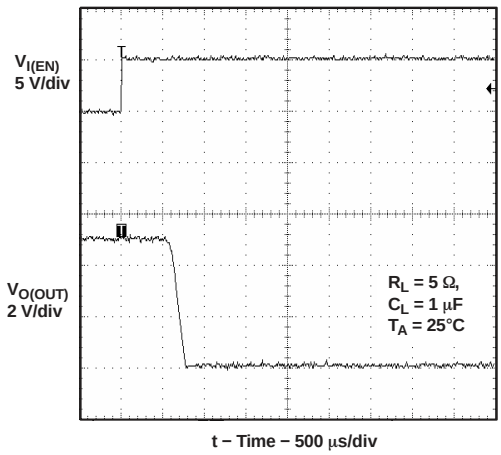


Figure 16. Turnoff Delay and Fall Time With 1-µF Load

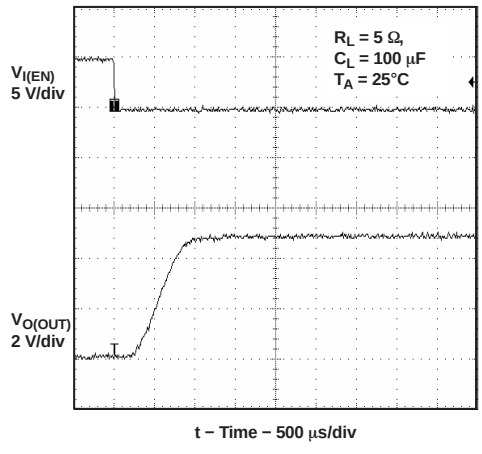


Figure 17. Turnon Delay and Rise Time With 100-µF Load

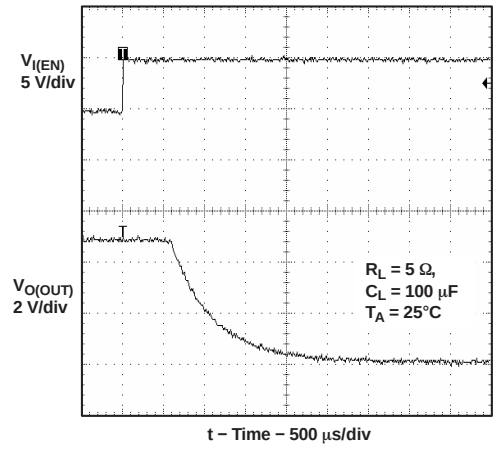


Figure 18. Turnoff Delay and Fall Time With 100-µF Load

Parameter Measurement Information (continued)

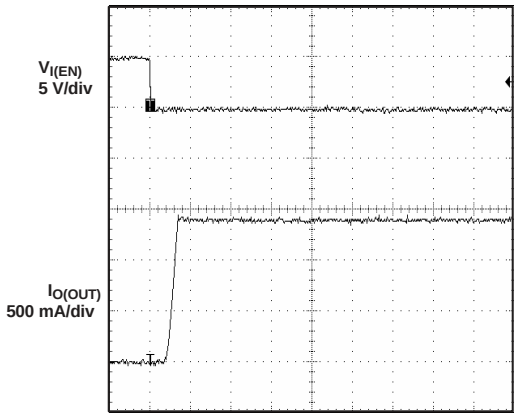


Figure 19. Short-Circuit Current, Device Enabled Into Short

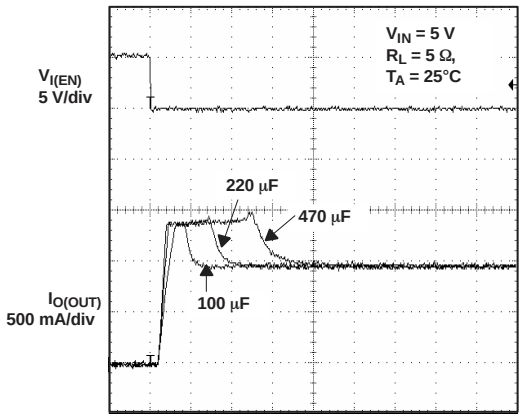


Figure 20. Inrush Current With Different Load Capacitance

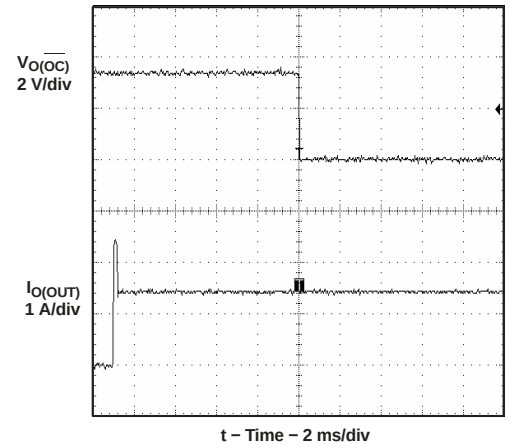


Figure 21. 2-Ω Load Connected to Enabled Device

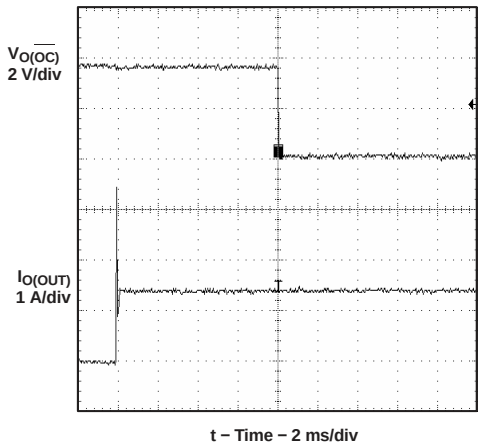


Figure 22. 1-Ω Load Connected to Enabled Device

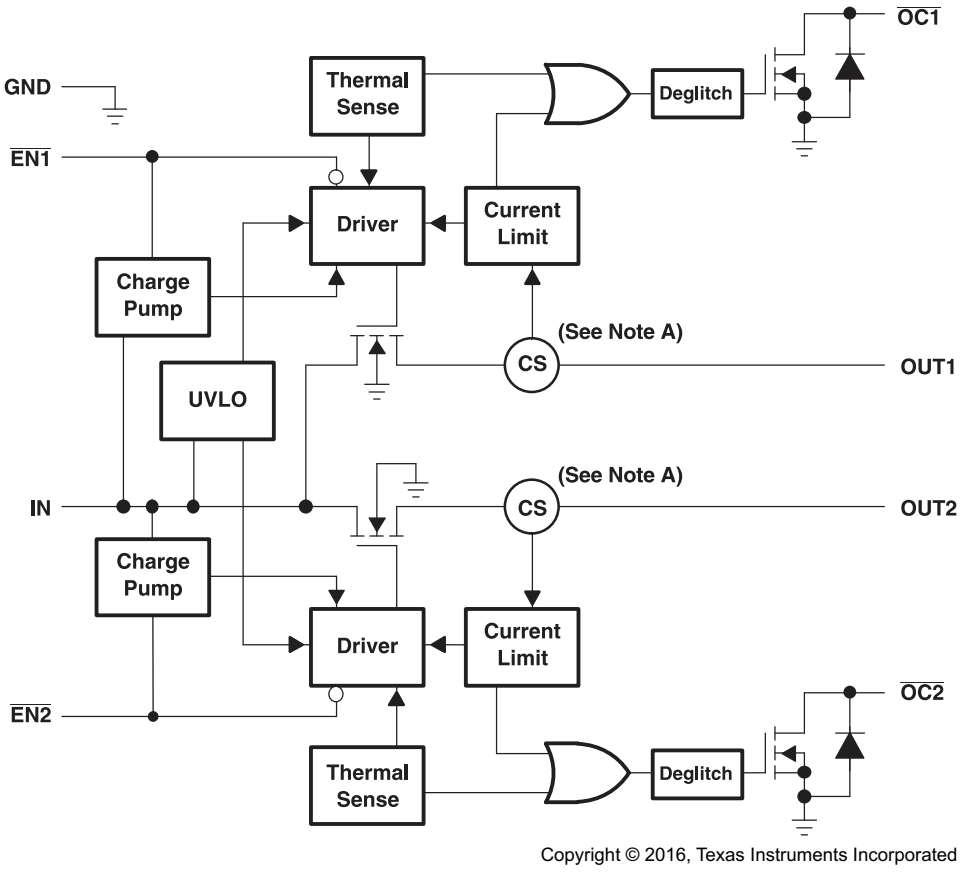
8 Detailed Description

8.1 Overview

The TPS206x-Q1 power-distribution switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently (10°C hysteresis, typical). Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5 A typically.

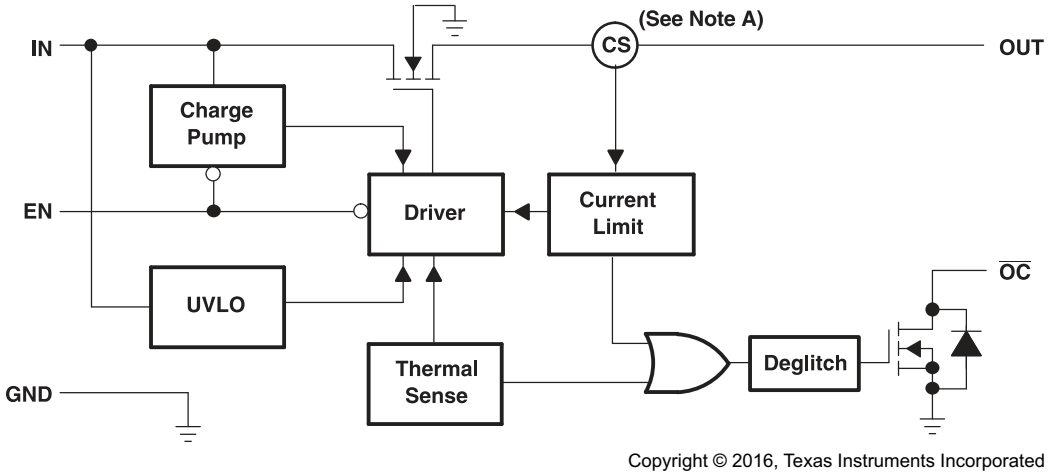
8.2 Functional Block Diagrams



A. Current sense

Figure 23. Functional Block Diagram – TPS2062-Q1

Functional Block Diagrams (continued)



A. Current sense

Figure 24. Functional Block Diagram – TPS2065-Q1

8.3 Feature Description

8.3.1 Power Switch

The power switch is an N-channel MOSFET with a low ON-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1 A.

8.3.2 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

8.3.3 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver controls the rise and fall times of the output voltage.

8.3.4 Enable ($\overline{ENx}$ for TPS2062-Q1) and (EN for TPS2065-Q1)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μA when a logic high is present on $\overline{ENx}$ or a logic low is present on EN. A logic low input on $\overline{ENx}$ or logic high on EN restores bias to the drive and control circuits and turns the switch ON. The enable input is compatible with both TTL and CMOS logic levels.

8.3.5 Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

Feature Description (continued)

8.3.6 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

8.3.7 Thermal Sense

The TPS2065-Q1 and TPS2062-Q1 implement a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the junction temperature rises to approximately 140°C, the internal thermal-sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10°C, the switch turns back ON. The switch continues to cycle OFF and ON until the fault is removed. The open-drain fault reporting output ($\overline{OC}x$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

8.3.8 Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

8.4 Device Functional Modes

The device has two functional modes of operation controlled by EN or $\overline{EN}x$. When there is a logic high on EN or a logic low on $\overline{EN}x$, the device is in the normal mode of operation and the power switch is ON. When EN is logic low or $\overline{EN}x$ is logic high, the device is in a low power mode where the power switch is off and the supply current is reduced to less than 1 μA.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 5). The TPS206x-Q1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2065-Q1 and TPS2062-Q1 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

9.1.2 $\overline{OC}$ Response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS2065-Q1 and TPS2062-Q1 are designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

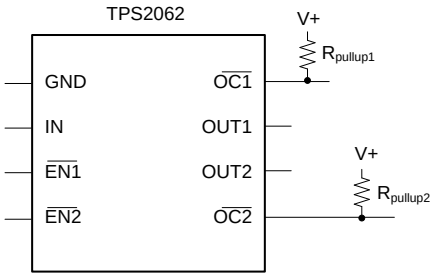


Figure 25. Typical Circuit for the $\overline{OC}$ Pin

Application Information (continued)

9.1.3 Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the OFF state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned ON until the power supply has reached at least 2 V, even if the switch is enabled. When the power supply returns, for example on cable reinsertion, the power switch is turned ON with a controlled rise time to reduce EMI and voltage overshoots.

9.1.4 Universal Serial Bus (USB) Applications

A typical application of the TPS206x-Q1 is for power distribution in USB applications. The universal serial bus (USB) interface is a 12-Mbps, or 1.5-Mbps, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts or self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS2065-Q1 and TPS2062-Q1 have higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

NOTE

The USB interface and standards are continually being updated and expanded. Check the applicability of this product to the specific USB standard for which it is used.

9.1.5 Host, Self-Powered (SPH), and Bus-Powered Hubs (BPH)

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 26). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

Application Information (continued)

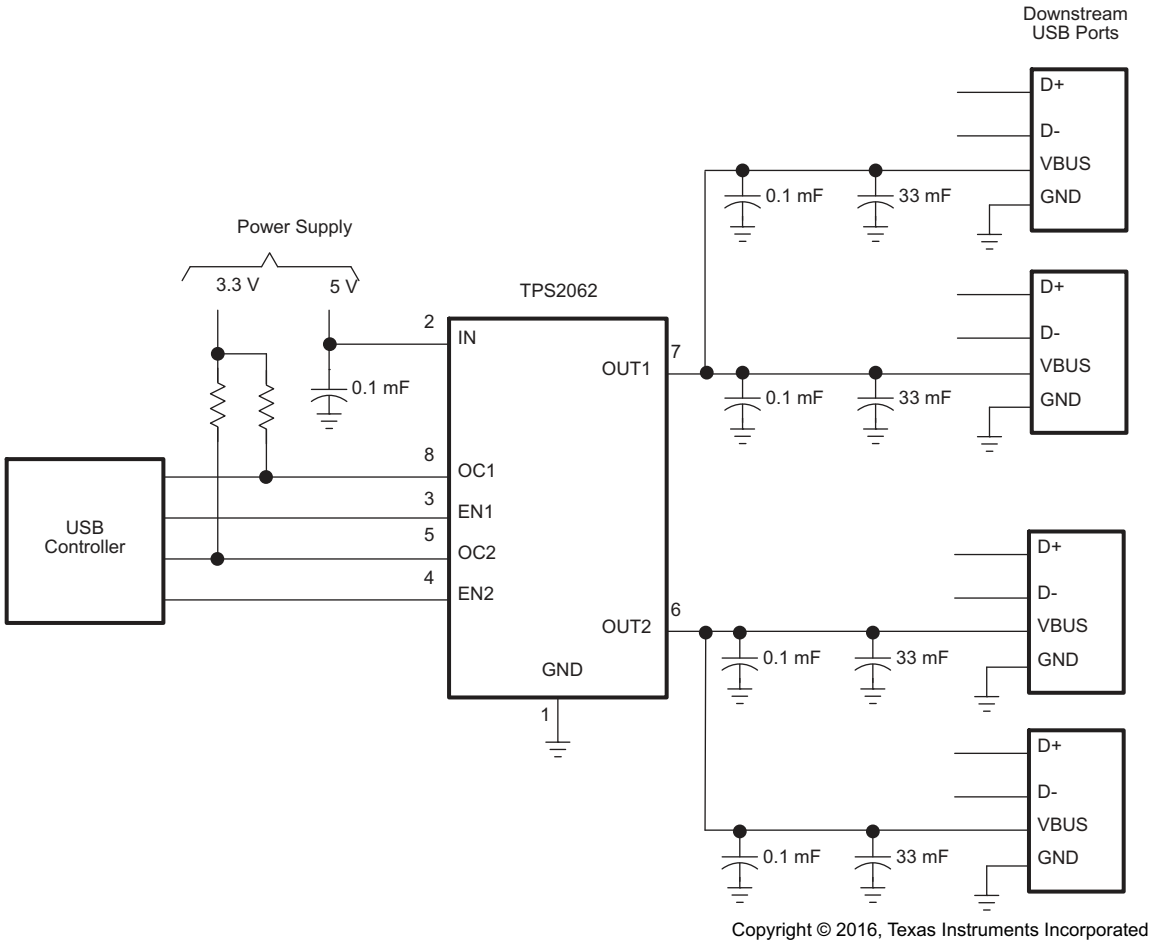


Figure 26. Typical Four-Port USB Host or Self-Powered Hub

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

9.1.6 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 27). With TPS2065-Q1 and TPS2062-Q1, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

Application Information (continued)

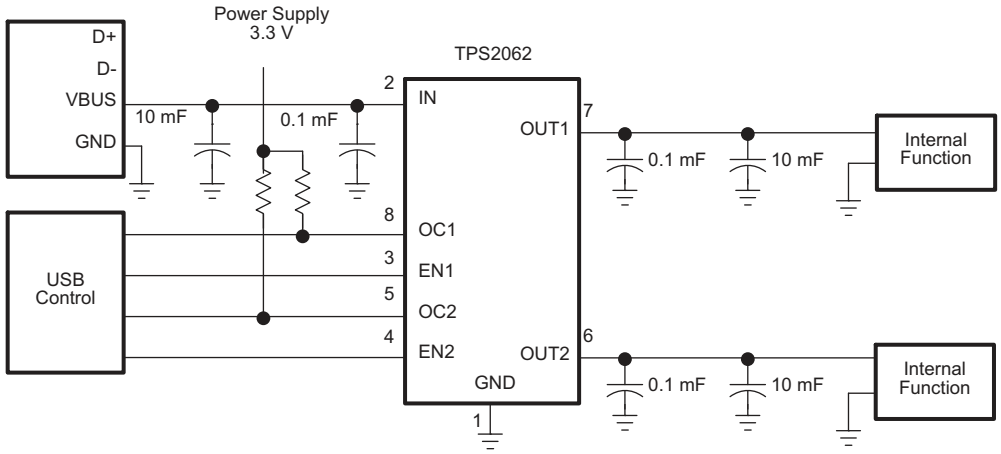


Figure 27. High-Power Bus-Powered Function

9.1.7 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts or SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- BPHs must:
  - Enable or disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2065-Q1 and TPS2062-Q1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 28).

Application Information (continued)

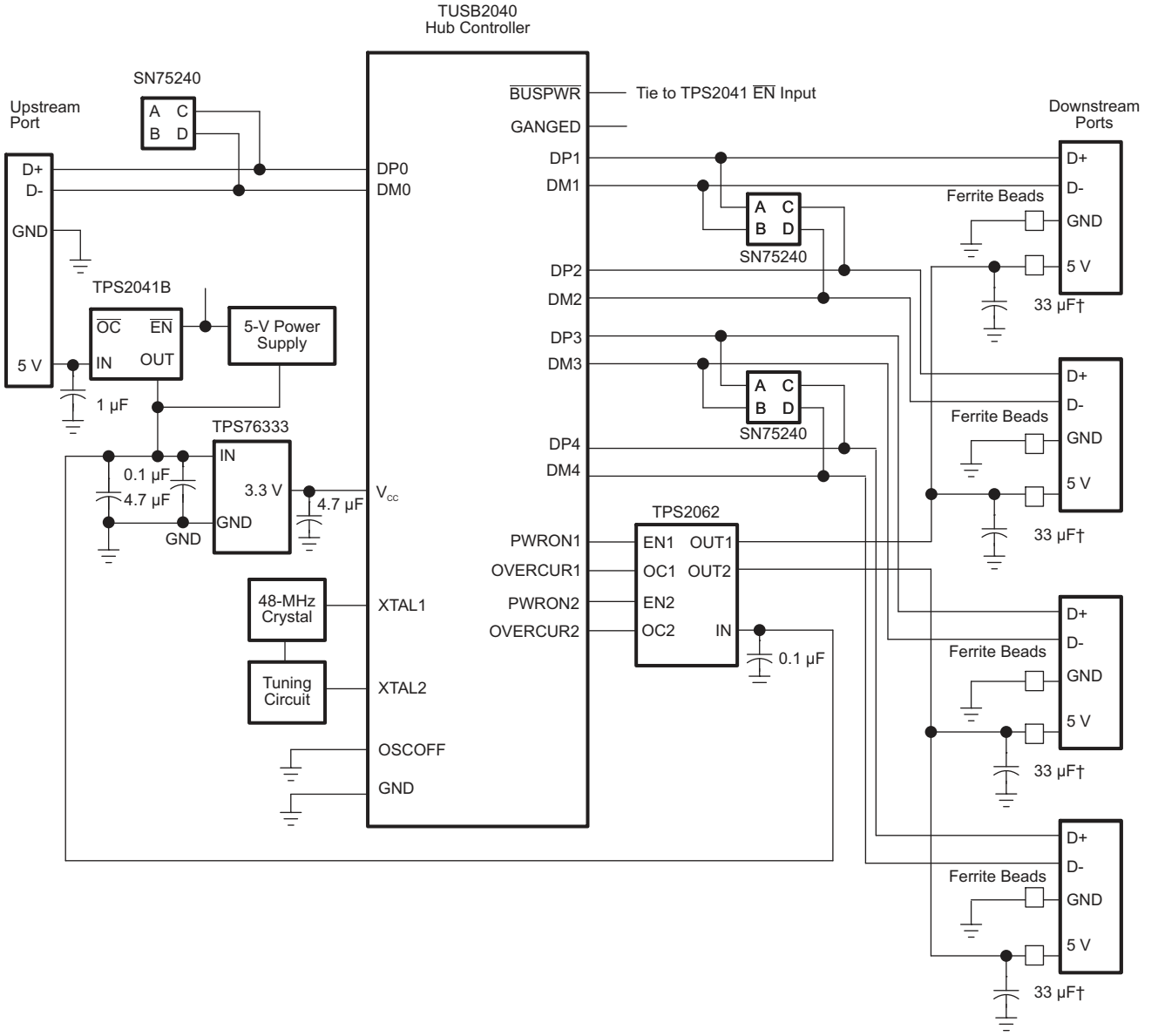


Figure 28. Hybrid Self- and Bus-Powered Hub Implementation

9.1.8 Generic Hot-Plug Applications

In many applications, it may be necessary to remove modules or PCBs while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2065-Q1 and TPS2062-Q1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2065-Q1 and TPS2062-Q1 ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

Application Information (continued)

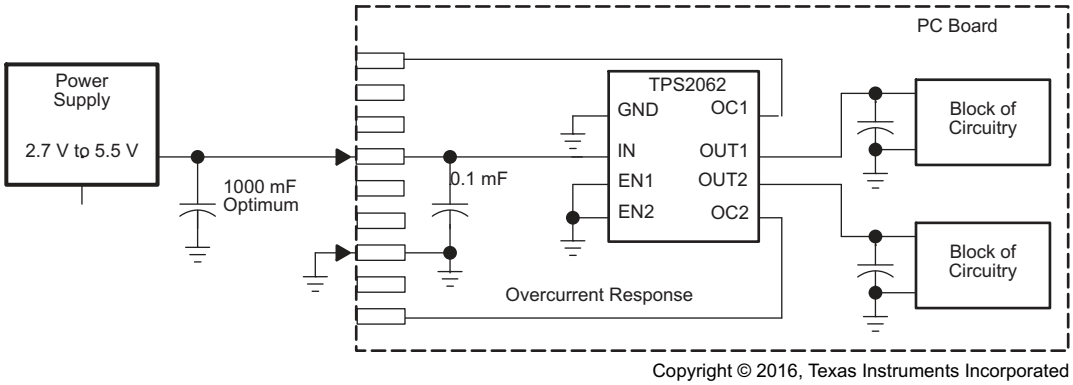


Figure 29. Typical Hot-Plug Implementation

By placing the TPS2065-Q1 and TPS2062-Q1 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

9.2 Typical Application

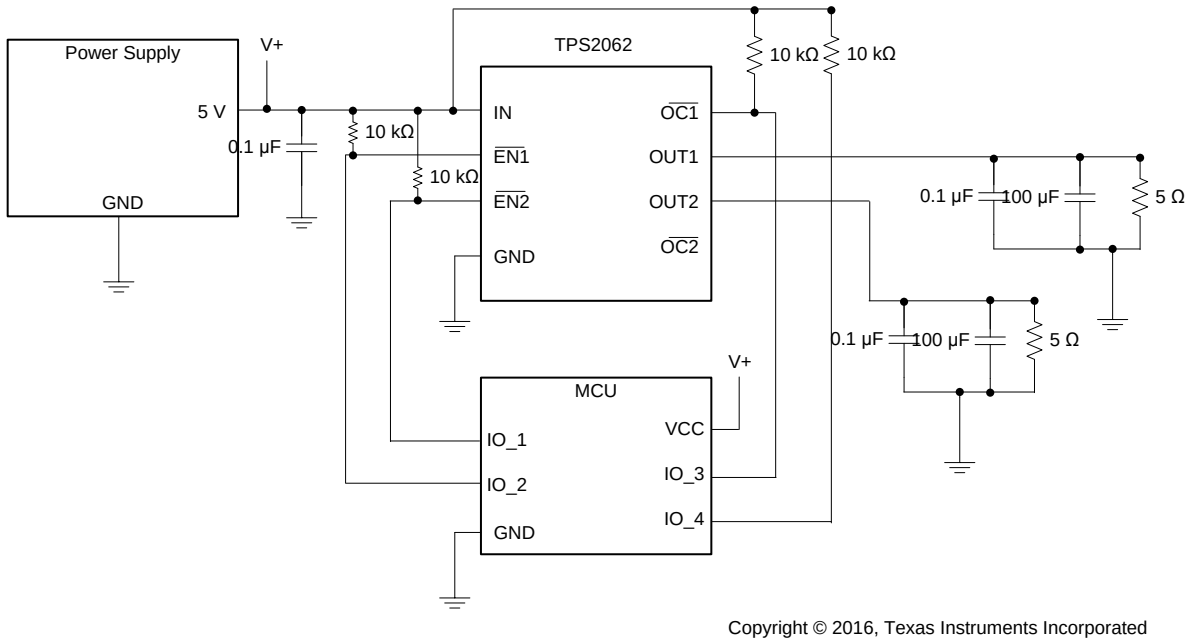


Figure 30. Typical Application Diagram

9.2.1 Design Requirements

The application requires distribution of 5 V to two seperate loads. The power supply can provide up to 4.5 A. In the case of a short circuit or overcurrent fault with a load, the supply to the other load must not be impacted. The load is equivalent to 5 Ω.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The two channel current-limited switch, TPS2062-Q1 is used. Each switch provides a current limit maximum of 2.1 A from the 5-V supply in the case of a short circuit. Each channel is independently controlled through its $\overline{EN}x$ and has a corresponding $\overline{OC}x$ flag to alert the controller in the system of the overcurrent in the channel. This allows the other channel to independetly function in case of a short and the channel with the short to be disabled by the controller if the fault persists to ensure that the device does not have a thermal shut down. Take care to use proper thermal design of the PCB and application is made following the guidelines in *Layout* to help avoid potential thermal shut down.

A 0.1-μF capacitor was used as close as possible to IN to filter high frequencies on switching. A 0.1-μF capacitor was also used as close as possible to OUTx to filter high frequencies on switching and a 100-μF capacitor is used on each OUTx as bulk capacitance for each load. This application is shown in Figure 30.

9.2.3 Application Curves

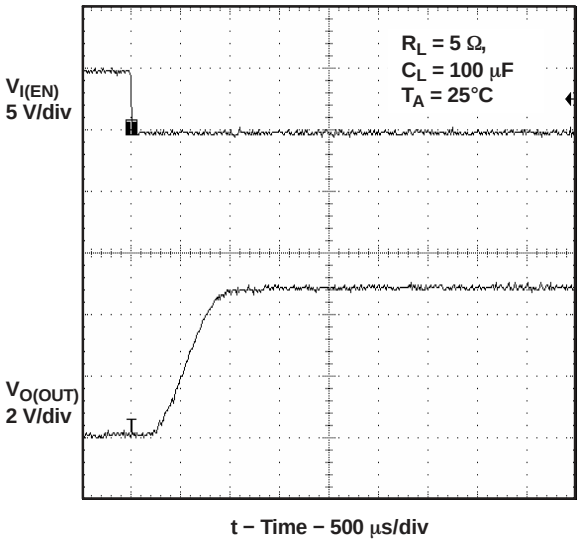


Figure 31. Turnon Delay and Rise Time With 100 μF and 5-Ω Load

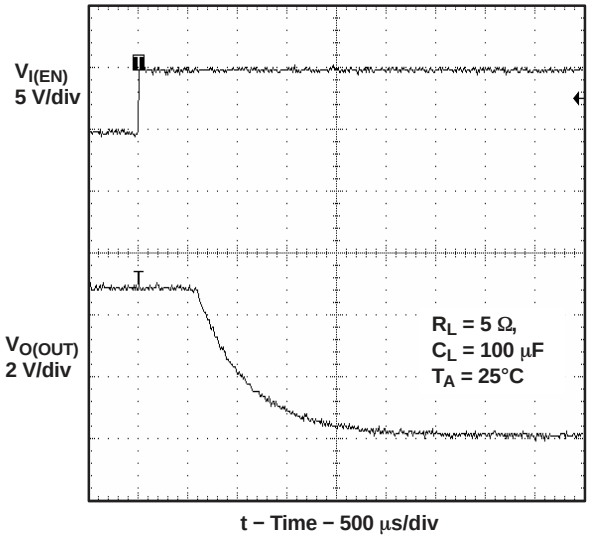


Figure 32. Turnoff Delay and Rise Time With 100 μF and 5-Ω Load

10 Power Supply Recommendations

TI recommends using a 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device. TI recommends placing a high-value electrolytic capacitor on the output pin(s) when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

11 Layout

11.1 Layout Guidelines

- Place the filter and bypass capacitor between IN and GND as close as possible ensuring a low-impedance trace for IN and a low-impedance trace and via path from GND to ground plane.
- Place the output filter capacitor as close as possible to OUT between OUT and GND. Place the higher-value electrolytic bypass capacitor between OUT and GND. The bypass capacitor is recommended when large transient currents are expected on the output. The OUT trace must be low-impedance to the load.
- Place the pullup resistor for $\overline{OCx}$ between the pullup voltage source and $\overline{OCx}$.

11.2 Layout Examples

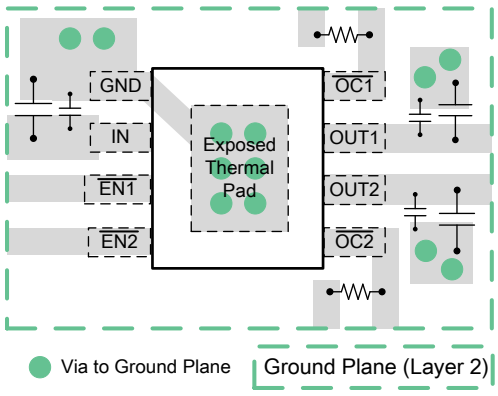


Figure 33. Layout Example for TPS2062-Q1

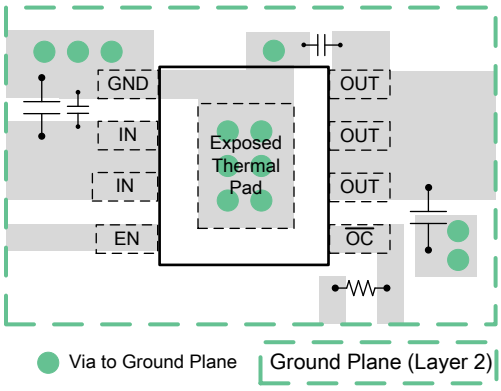


Figure 34. Layout Example for TPS2065-Q1

11.3 Thermal Considerations

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS2065-Q1 and TPS2062-Q1 implement a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises above a minimum of 135°C due to overcurrent conditions, the internal thermal-sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal-sense circuit, and after the device has cooled approximately 10°C, the switch turns back ON. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low, with a 10-ms deglitch) when an overtemperature shutdown or overcurrent occurs.

11.4 Power Dissipation and Junction Temperature

The low ON-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(ON)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(ON)}$ from Figure 9. Using this value, the power dissipation per switch can be calculated using Equation 1:

$$P_D = r_{DS(ON)} \times I^2 \quad (1)$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

The thermal resistance, $R_{\theta JA}$ = 1 / (DERATING FACTOR), where DERATING FACTOR is obtained from *Dissipation Ratings*. Thermal resistance is a strong function of the printed-circuit board construction, and the copper trace area connecting the integrated circuit.

Finally, calculate the junction temperature with Equation 2:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- T_A= Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used. (2)

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

See the TPS2065-Q1 product tools folder on TI.com for a PSpice model and evaluation module.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2062-Q1	Click here	Click here	Click here	Click here	Click here
TPS2065-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2062QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSOQ	Samples
TPS2065QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTLQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

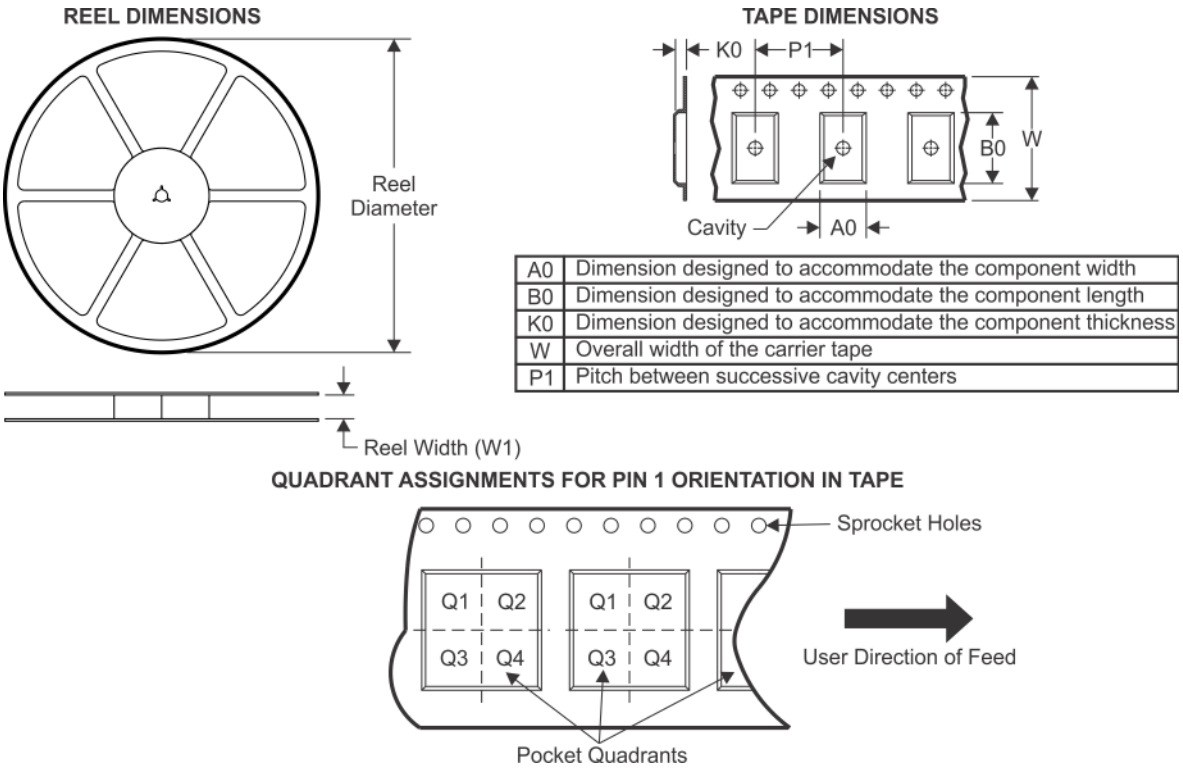
OTHER QUALIFIED VERSIONS OF TPS2062-Q1, TPS2065-Q1 :

- Catalog: TPS2062, TPS2065

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

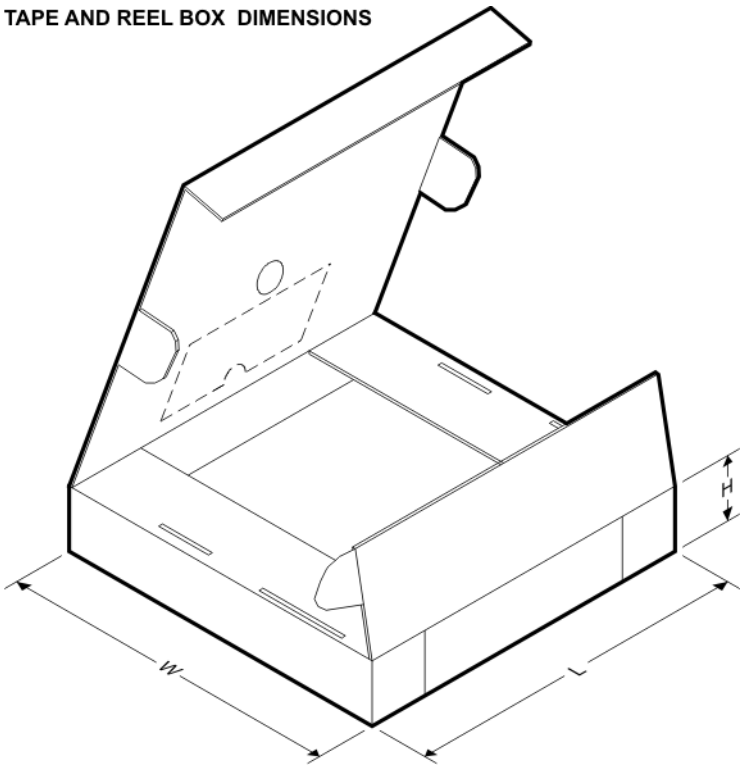


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2062QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2065QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2062QDGNRQ1	HVSSOP	DGN	8	2500	370.0	355.0	55.0
TPS2065QDGNRQ1	HVSSOP	DGN	8	2500	370.0	355.0	55.0

GENERIC PACKAGE VIEW

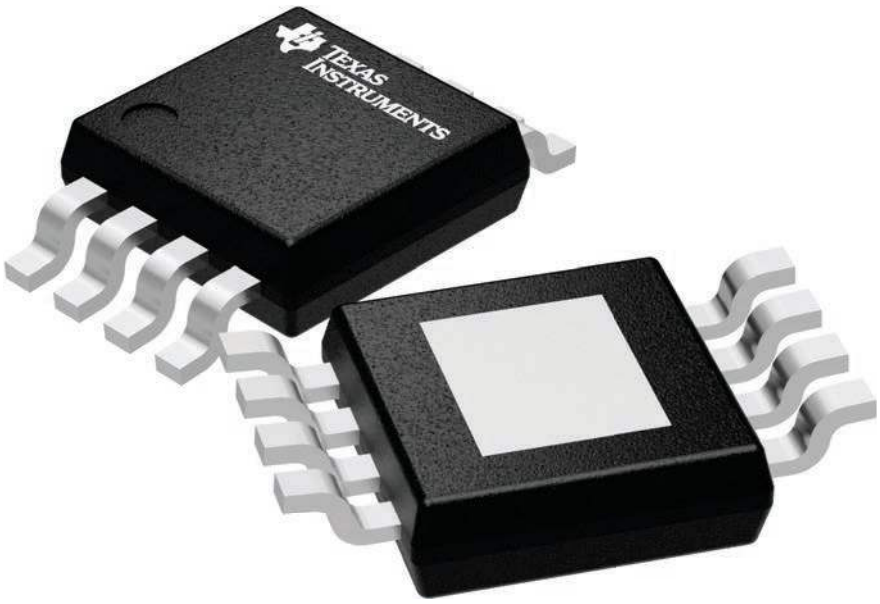
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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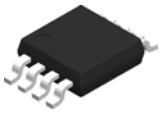
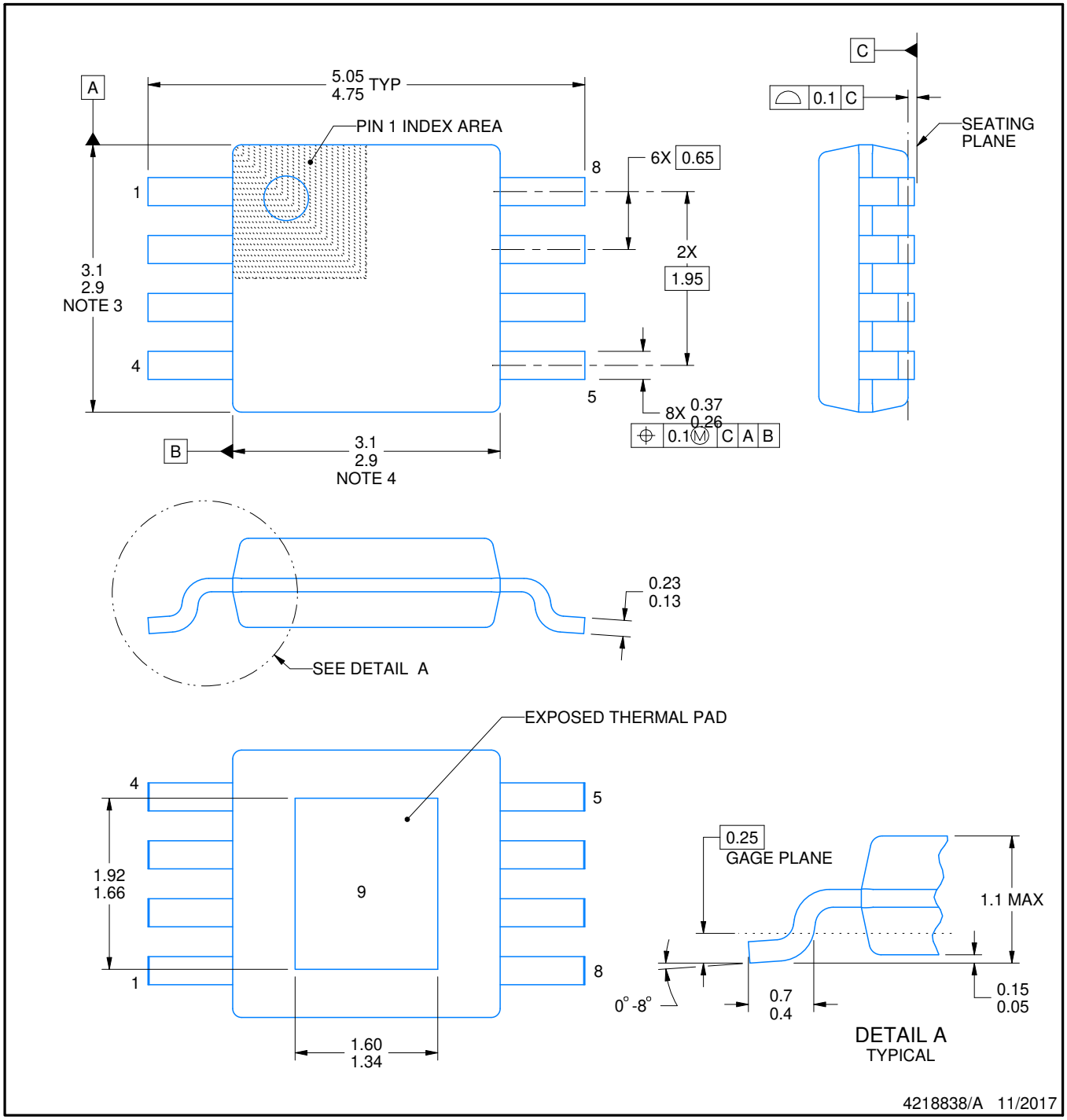
PACKAGE OUTLINE

DGN0008C



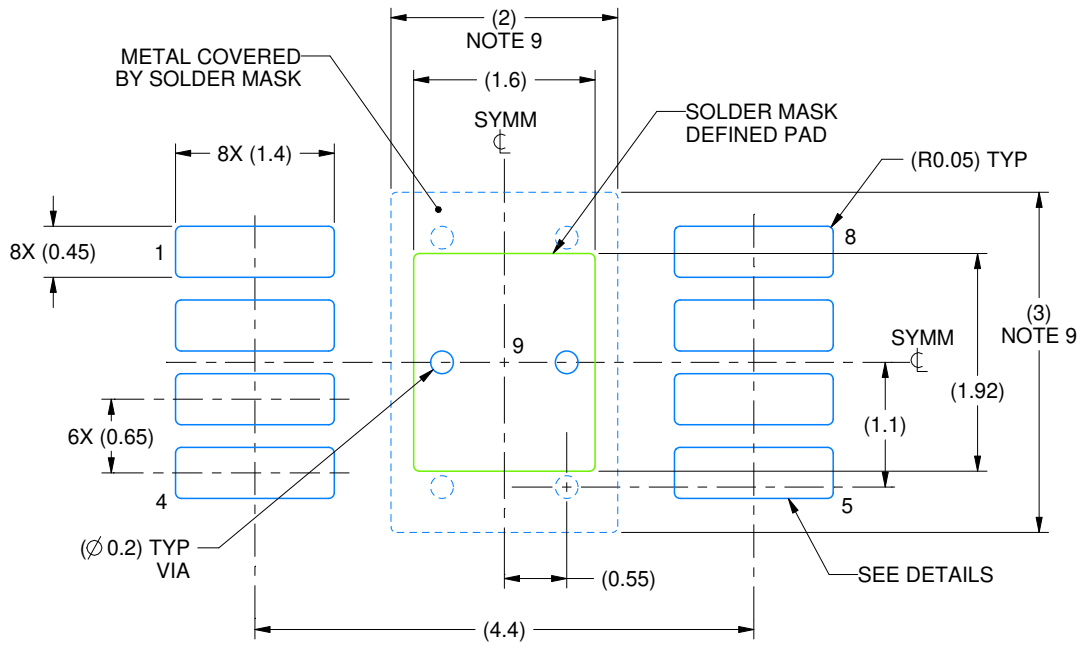
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

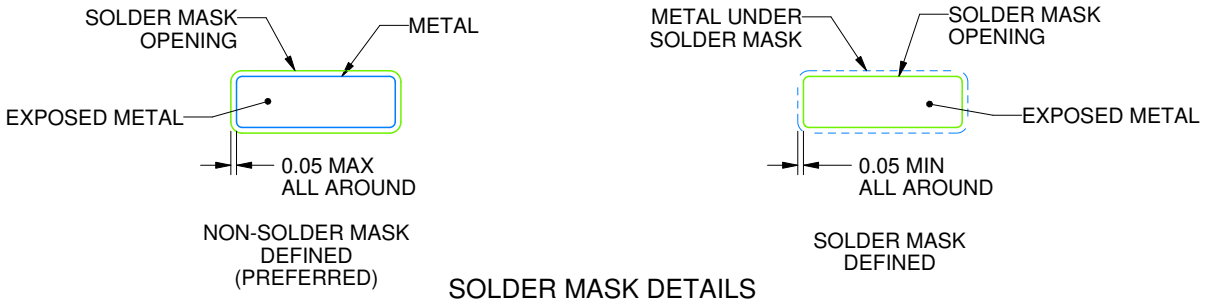


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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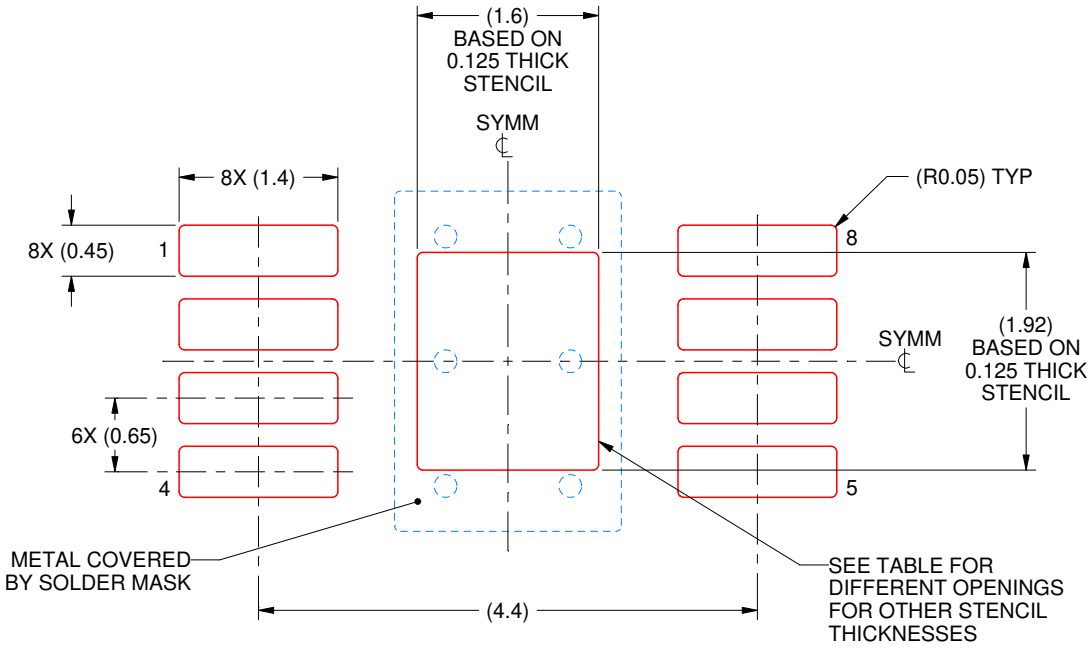
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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