BUF-03

HIGH-SPEED VOLTAGE FOLLOWER/BUFFER

Precision Monolithics Inc.

FEATURES

- **Very High Slew Rate** ..... **220V/μs Min**
- **Wide Bandwidth** **63MHz**
- **Load Drive Current** ..... **70mA Peak**
- **Easily Drives Large Capacitive Loads Without Oscillation**
- **High Input Resistance** ..... **$5 \times 10^{11}\Omega$**
- **Low Output Resistance** **2Ω**
- **Very Low Bias Current (Warmed-Up)** ..... **400pA Max**
- **Low Offset Voltage** ..... **6mV Max**
- **Unity Gain** **0.997V/V**
- **Excellent Gain Linearity** **0.015%**
- **Available in Die Form**

ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

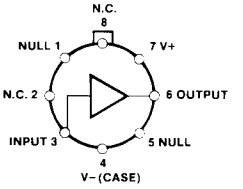
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

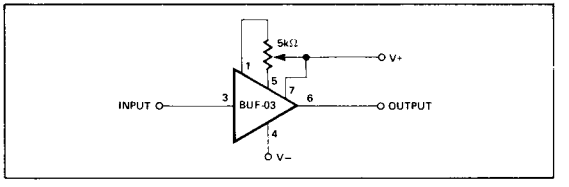
Applications for which the BUF-03 is well-suited include high-speed line drivers, isolation amplifiers for driving reactive loads, and high-speed sample-hold circuits.

PIN CONNECTIONS

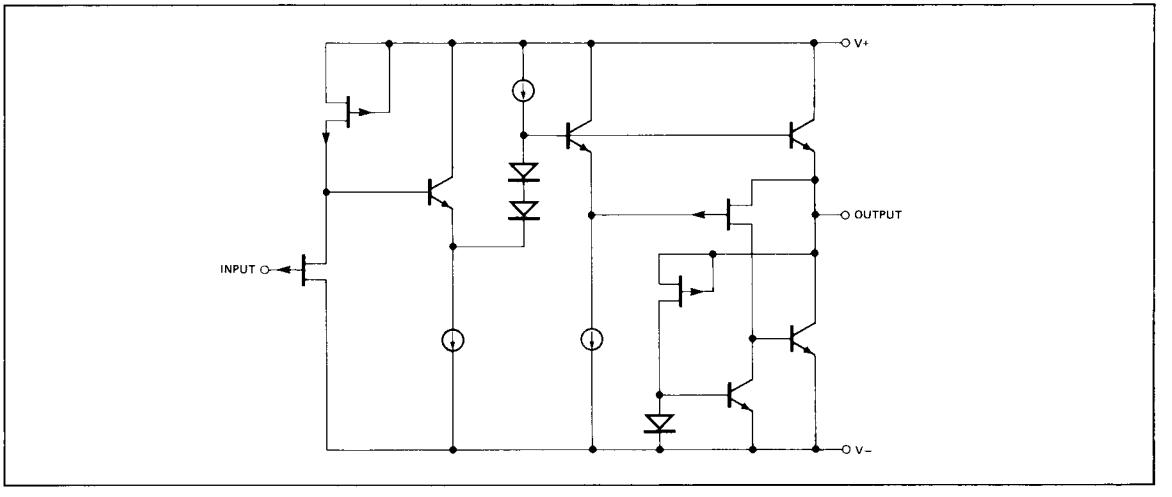


TO-99 (J-Suffix)

OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (P_d)
In Still Air Without Heat Sink (Note 1) 1.00W
Input Voltage (Note 2) ..... ±18V
Continuous Output Current (Note 3) 70mA
Peak Output Current (Note 3) 100mA
Short Circuit Protection (Note 3) ..... Indefinite (Note 4)
Maximum Junction Temperature (T_j) ..... 175°C
Storage Temperature Range ..... −65°C to +175°C
Operating Temperature Range (Note 5)
..... −55°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Dice Junction Temperature (T_j) ..... −65°C to +175°C
Thermal Resistance θ_{JA} (Note 1) ..... 150°C/W
Thermal Resistance θ_{JC} (Note 1) ..... **18°C/W**

NOTES:
1. Based on MIL-STD-38510 published thermal resistance specification for 8 lead can-case outline C.
2. When $V_{CC} < \pm 18V$, the maximum input voltage is equal to the supply voltage.
3. The maximum P_d or T_j are not to be exceeded.
4. At 80mA.
5. When operating at $T_A > +25°C$, heat sinking is required to insure $T_{jMAX} = +175°C$ specification is not exceeded using the equation $T_{jMAX} = T_A + (P_d \times \theta J_{CMAX} + \theta_{SA})$ where θ_{SA} = sink to ambient thermal resistance. PMI recommends using either the Thermalloy 2227 or 1101 or equivalent when operating up to $T_A = +125°C$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 0\Omega$, $T_A = T_j = 25°C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A/E MIN	BUF-03A/E TYP	BUF-03A/E MAX	BUF-03B/F MIN	BUF-03B/F TYP	BUF-03B/F MAX	UNITS
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$, $T_A = T_j = 75°C$	220	250	—	180	250	—	V/μs
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} = \leq 2V_{p-p}$	—	63	—	—	50	—	MHz
Settling Time	t_S	To 0.1%, ±10V step	—	90	—	—	100	—	ns
Capacitive Load Capability	C_{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t_d	Step Input	—	7	—	—	7	—	ns
Rise Time	t_r	ΔV = 0.5V	—	7	—	—	7	—	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	—	350	—	—	400	—	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	—	50	—	—	60	—	$nV/\sqrt{Hz}$
DC SPECIFICATIONS									
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	2	6	—	4	15	mV
Input Bias Current	I_B		—	150	400	—	180	700	pA
Input Resistance	R_{IN}		—	5×10^{11}	—	—	4×10^{11}	—	Ω
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	0.9960 0.9945 0.9925	0.9975 0.9960 0.9945	— — —	0.9940 0.9930 0.9905	0.9970 0.9950 0.9930	— — —	V/V
Nonlinearity (Note 2)	NL	$V_{IN} = \pm 10V$, $R_L \geq 2k\Omega$ (Note 3) $V_{IN} = \pm 7V$, $R_L \geq 1k\Omega$	— —	0.015 0.013	0.023 0.023	— —	0.017 0.015	0.03 0.03	%F.S.
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to $20k\Omega$ (Note 2) $R_L \geq 2k\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I_{SY}	No Load	—	19	25	—	19	25	mA
Peak Load Current	$I_{L,PK}$		—	70	—	—	70	—	mA
Output Resistance	R_O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	—	±80	—	—	±80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	±11.5	—	—	±11.5	—	V

NOTES:
1. Electrical parameters are pulse tested on automated test equipment. Total test time at each temperature is limited to less than one second maximum to keep T_j approximately equal to T_A.
2. Parameters specified with $R_S \leq 20k\Omega$ are tested at $R_S = 0\Omega$. Limits in test program are adjusted to take into account worst case voltage offset induced by $R_S = 20k\Omega$, i.e., I_B max × $20k\Omega$.
3. Nonlinearity is computed using linear regression techniques with data from five points (e.g., −10V, −5V, 0V, +5V, +10V for ±10V full-scale linearity; −7V, −3.5V, 0V, +3.5V, and +7V for ±7V full-scale linearity).

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, $T_A = T_j$, unless otherwise noted. (Note 1)

			BUF-03A			BUF-03B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	—	220	—	—	220	—	V/μs
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2)	—	50	100	—	90	170	μV/°C
Input Bias Current	I_B	$T_A = +125°C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	2.24	mV/V
Supply Current	I_{SY}	$T_A = +125°C$	—	18	24	—	18	24	mA

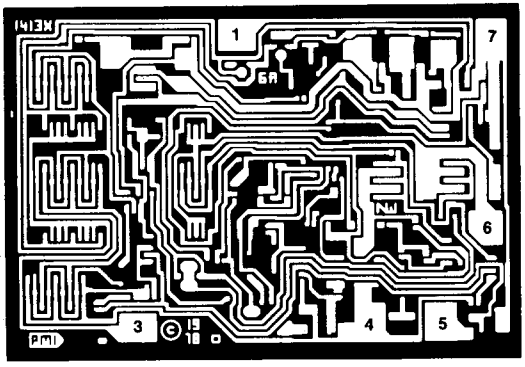
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, $T_A = T_j$, unless otherwise noted.

			BUF-03E			BUF-03F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \geq 2k\Omega$	—	240	—	—	240	—	V/μs
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2	—	40	90	—	80	150	μV/°C
Input Bias Current	I_B	$T_A = +70°C$	—	1.5	5	—	1.8	8	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70°C$	—	19	25	—	19	25	mA

NOTES:

1. In order to operate the device at an ambient temperature of +125°C, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of +175°C. The chip temperature of +165°C is achieved by reducing the case-to-ambient thermal resistance to 30°C/W (e.g., Thermalloy 2227).
2. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.071 × 0.049 inch, 3479 sq. mils
(1.80 × 1.24 mm, 2.23 sq. mm)

1. NULL
3. INPUT
4. NEGATIVE SUPPLY
5. NULL
6. OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	25	25	mA MAX

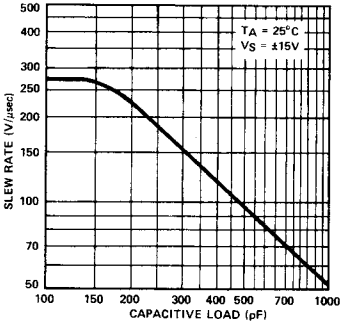
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

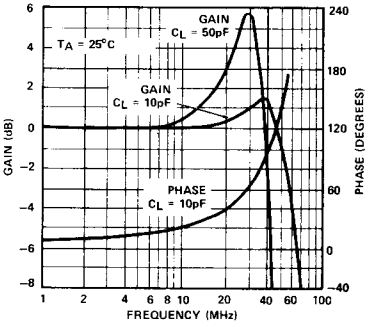
PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	180	V/μs
Peak Load Current	$I_{L\cdot PK}$		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	±80	±80	mV
Input Voltage Range (Reduced Accuracy)	IVR		±11.5	±11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V_{p\text{-}p}$, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{p\text{-}p}$	63	55	MHz
Settling Time	t_S	To 0.1%, ±10V step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d	Step Input	7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	50	60	$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

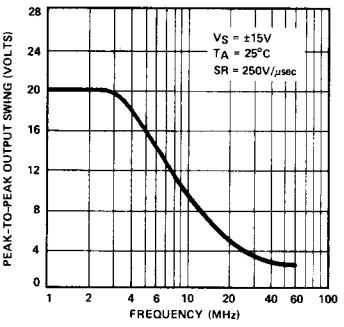
SLEW RATE vs CAPACITIVE LOAD



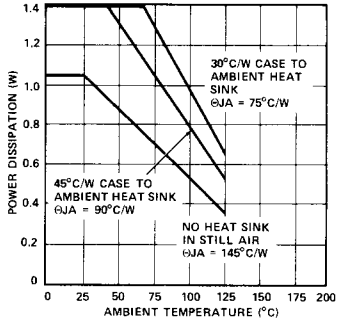
GAIN AND PHASE RESPONSE vs FREQUENCY



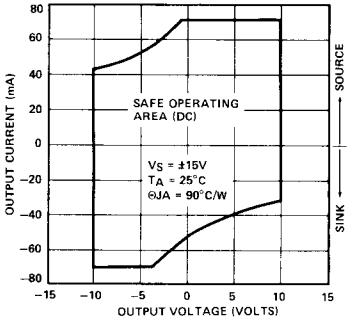
LARGE-SIGNAL FREQUENCY RESPONSE



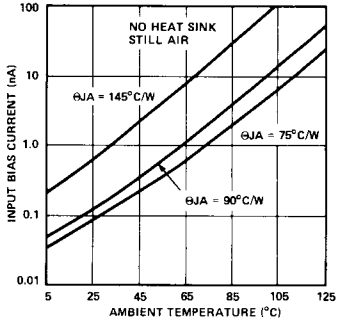
MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



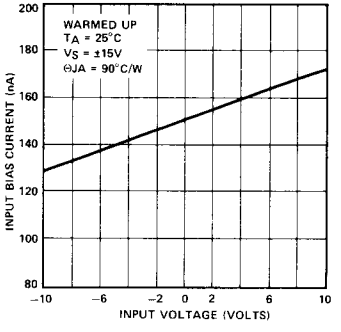
OUTPUT CURRENT vs OUTPUT VOLTAGE



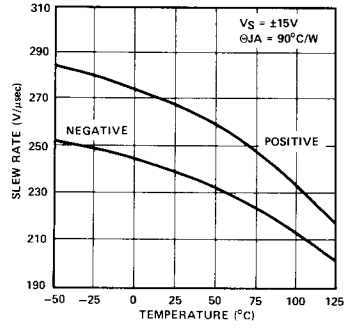
INPUT BIAS CURRENT vs TEMPERATURE (WARMED-UP)



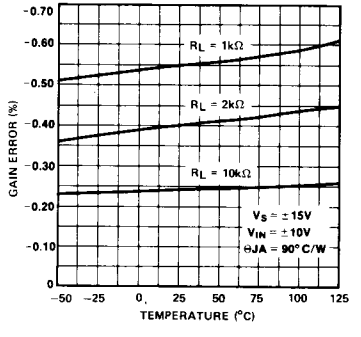
INPUT BIAS CURRENT vs INPUT VOLTAGE



SLEW RATE vs TEMPERATURE

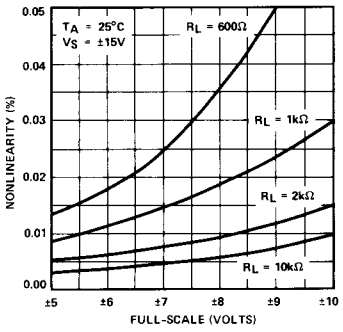


GAIN ERROR vs TEMPERATURE

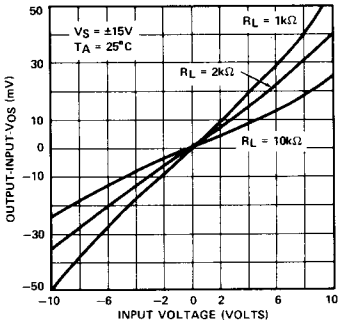


TYPICAL PERFORMANCE CHARACTERISTICS

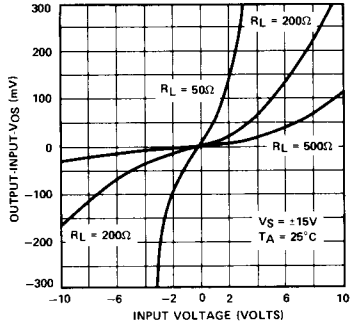
NONLINEARITY vs FULL-SCALE VOLTAGE



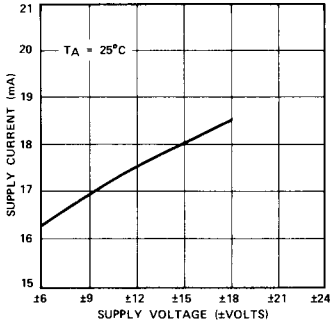
GAIN ERROR vs INPUT VOLTAGE



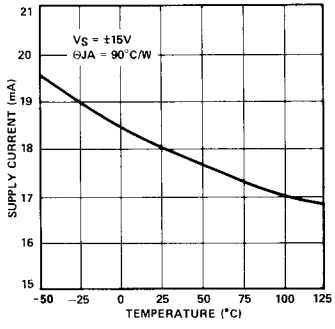
GAIN ERROR vs INPUT VOLTAGE



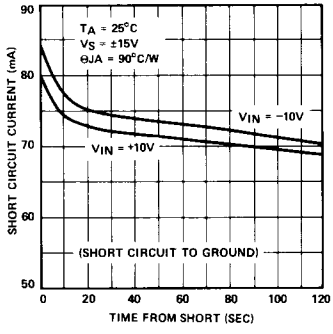
SUPPLY CURRENT vs SUPPLY VOLTAGE



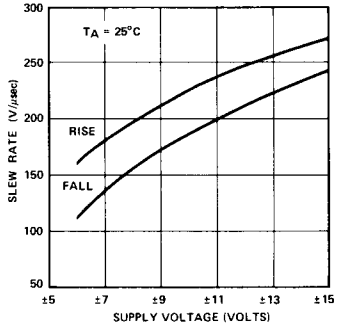
SUPPLY CURRENT vs TEMPERATURE



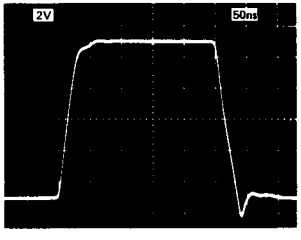
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



SLEW RATE vs SUPPLY VOLTAGE



SLEW RATE



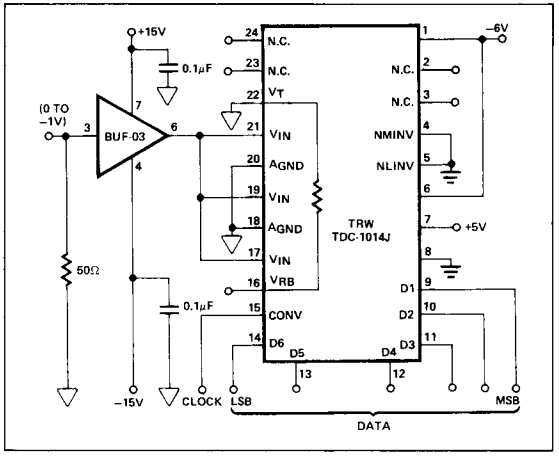
5 OPERATIONAL AMPLIFIERS/BUFFERS

APPLICATIONS INFORMATION

OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at ±6V supplies ±2V signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical 540mW (=30V×18mA) to 195mW (=12V×16.2mA) at ±6V. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH-SPEED 6-BIT A/D BUFFER



HIGH-SPEED SAMPLE/HOLD AMPLIFIER