

# **Operational Amplifiers**

# **High Speed Operational Amplifiers**

# BA3472YF-LB

# **General Description**

This is the product guarantees long time support in Industrial market.

BA3474YF integrates two independent Op-amps on a single chip. These Op-Amps can operate from +3V to +36V (single power supply) with a high slew rate  $(10V/\mu s)$  and high-gain bandwidth (4MHz) characteristics.

#### **Features**

- Long Time Support a Product for Industrial Applications
- High Slew Rate
- Single or dual power supply operation
- Wide operating supply voltage
- High open-loop voltage gain
- Common-mode Input Voltage Range includes ground level, allowing direct ground sensing
- Wide output voltage range

#### Packages SOP8

W(Typ) x D(Typ) x H(Max) 5.00mm x 6.20mm x 1.71mm

# **Key Specifications**

■ Wide Operating Supply Voltage:

Single supply
Dual supply

■ Wide Temperature Range:

Input Offset Voltage:

Low Input Offset Current:

Low Input Bias Current:

+3.0V to +36.0V

±1.5V to ±18.0V

-40°C to +125°C

10mV (Max)

6nA (Typ)

100nA (Typ)

■ Wide Output Voltage Range:

VEE+0.3V to VCC-1.0V(Typ) (VCC-VEE=30V)

■ Slew Rate: 10V/µs(Typ)
■ Gain Band Width: 4MHz(Typ)

# **Application**

- Industrial Equipment
- Current sense application
- Buffer application amplifier
- Active filter

# Simplified schematic

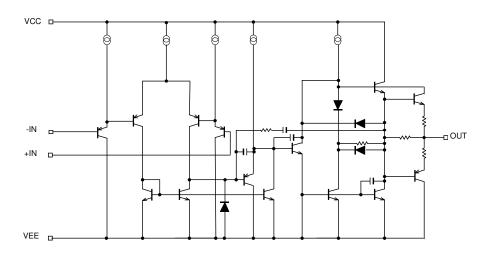
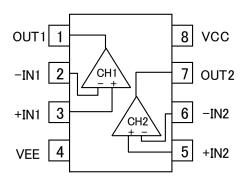


Figure 1. Simplified schematic (one channel only)

# Pin Configuration(TOP VIEW)

SOP8



Pin No.	Symbol				
1	OUT1				
2	-IN1				
3	+IN1				
4	VEE				
5	+IN2				
6	-IN2				
7	OUT2				
8	VCC				

**Ordering Information** 

В	Α	3	4	7	2	Υ	F	-	LB H2	
Part N BA34	Numbei 72YF	ſ				Pack F	age : SOP8		Product class LB for Industrial a Packaging and fo H2: Embossed ta (SOP8)	rming specification

Line-up

Topr	Pa	ckage	Orderable Part Number
-40°C to +125°C	SOP8	Reel of 250	BA3472YF-LBH2

**Absolute Maximum Ratings** (T<sub>A</sub>=25°C)

Parameter	Symbol		Ratings	Unit		
Supply Voltage	VCC-VEE		+36	V		
Power dissipation	P <sub>D</sub>	SOP8	1.075 <sup>(Note 1,2)</sup>	W		
Differential Input Voltage (Note 3)	Vı	D	+36	V		
Input Common-mode Voltage Range	V <sub>ICM</sub>		V <sub>ICM</sub>		(VEE-0.3) to VEE+36	V
Input Current <sup>(Note 4)</sup>	l <sub>1</sub>		-10	mA		
Operating Supply Voltage	Vo	pr	+3.0V to +36.0V (±1.5V to ±18.0V)	V		
Operating Temperature	T <sub>opr</sub>		-40 to +125	°C		
Storage Temperature	$T_{stg}$		T <sub>stg</sub>		-55 to +150	°C
Maximum Junction Temperature	$T_{Jmax}$		+150	°C		

<sup>(</sup>Note 1) To use at temperature above T<sub>A</sub>=25°C reduce 8.6mW/°C.

The input current can be set to less than the rated current by adding a limiting resistor.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

<sup>(</sup>Note 2) Mounted on a FR4 glass epoxy 4 layers PCB 70mm×70mm×1.6mm (occupied copper area: 70mm×70mm).

The voltage difference between inverting input and non-inverting input is the differential input voltage.

Then input terminal voltage is set to more than VEE.

<sup>(</sup>Note 4) An excessive input current will flow when input voltages of less than VEE-0.6V are applied.

# **Electrical Characteristics**

OBA3472YF-LB (Unless otherwise specified VCC=+15V, VEE=-15V)

JBA34/2YF-LB (Unless of		Temperature	, , , , , , ,	Limits	,	119		Compliti - :-		
Parameter	Symbol	range	Min.	Тур.	Max.	Unit		Condition		
(Note 5)			-	-	10	.,	Vicm=0V,			
Input Offset Voltage (Note 5)	Vio	full range	-	-	10	mV	VCC=5V VEE=0V	Vicm=0V OUT=VCC/2		
Input Offset Current (Note 5)	lio	25°C	-	6	75	nA	Vicm=0V,	OUT-0V		
input Onset Guirent	110	full range	-	-	100	1173	VICITI-OV,	001-01		
Input Bias Current (Note 6)	lb	25°C	-	100	150	nA	Vicm=0V,	OUT-0V		
mpat Blad Garront	10	full range	-	-	200		V10111-0 V,			
Supply Current	ICC	25°C	-	4	5	mA	RL=∞			
опры оптент	100	full range	-	-	5.5	ША	TILESS			
		25°C	3.7	4	-		VCC=5V	RL=2kΩ		
		full range	3.5	-	-		VEE=0V	TIL=ZN12		
Maximum Output Voltage(High)	VOH	25°C	13.7	14	-	V	BI =10k0			
		full range	13.5	-	-		RL=10kΩ			
		25°C	13.5	-	-		RL=2kΩ			
		25°C	-	0.1	0.3		VCC=5V	RL=2kΩ		
		full range	-	-	0.6		VEE=0V	111-21/22		
Maximum Output Voltage(Low)	VOL	25°C	-	-14.7	-14.3	V	RL=10kΩ			
		full range	-	-	-14.0		TIL=TOK22			
		25°C	-	-	-13.5		RL=2kΩ			
Large Signal Voltage Gain	Av	25°C	80	100	-	dB	DI > 2k0	OUT=±10V		
Large Signal Voltage Claim	Av	full range	70	-	-	uБ	nt⊑≥ktz,	OUT=±10V		
Input Common-mode	Vicm	25°C	0	-	VCC-2.0	V	VCC=5V	OUT=VCC/2		
Voltage Range	VICITI	full range	0	-	VCC-2.6	V	VEE=0V	001=000/2		
Common-mode Rejection Ratio	CMRR	25°C	60	97	-	dB	OUT=0V			
Power Supply Rejection Ratio	PSRR	25°C	60	97	-	dB	Vicm=0V,	OUT=0V		
Output Source Current	Isource	25°C	10	30	-	mΛ	VCC=5V	IN+=1V IN-=0V		
(Note <sup>-</sup> 7)	isource	full range	10	-	-	mA	VEE=0V	OUT=0V Only 1ch is short circuit		
(Noto 7)		25°C	20	30	-		VCC=5V	IN+=0V IN-=1V		
Output Sink Current (Note 7)	Isink	full range	20	-	-	mA	VEE=0V	OUT=5V, Only 1ch is short circuit		
Gain Band Width	GBW	25°C	-	4	-	MHz		-		
Slow Pato	QD.	25°C	-	10	-	\//	Av=1, IN=	-10V to +10V,		
Slew Rate	SR	full range	5	-	-	V/µs	RL=2kΩ			
Channel Separation	CS	25°C	_	120	_	dB		-		

<sup>(</sup>Note 5) Absolute value

<sup>(</sup>Note 6) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

<sup>(</sup>Note 7) Under high temperatures, please consider the power dissipation when selecting the output current.

When the output terminal is continuously shorted the output current reduces the internal temperature by flushing.

#### **Description of Electrical Characteristics**

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

# 1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

#### 1.1 Power supply voltage (VCC-VEE)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

#### 1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.

#### 1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

#### 1.4 Power dissipation (Pd)

Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

# 2. Electrical characteristics

# 2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

#### 2.2 Input offset current (lio)

Indicates the difference of input bias current between the non-inverting and inverting terminals.

# 2.3 Input bias current (lb)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.

# 2.4 Circuit current (ICC)

Indicates the current that flows within the IC under specified no-load conditions.

# 2.5 High level output voltage/low level output voltage (VOH/VOL)

Indicates the voltage range of the output under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage while Low-level output voltage indicates the lower limit.

#### 2.6 Large signal voltage gain (Av)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

Av = (Output voltage fluctuation) / (Input offset fluctuation)

# 2.7 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC normally operates.

# 2.8 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.

CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

# 2.9 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.

PSRR= (Change of power supply voltage)/(Input offset fluctuation)

# 2.10 Output source current/ output sink current (IOH / IOL)

The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

# 2.11 Gain Band Width (GBW)

The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.

#### 2.12 Slew rate (SR)

Indicates the ratio of the change in output voltage with time when a step input signal is applied.

# 2.13 Channel separation (CS)

Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

# **Typical Performance Curves**

OBA3472YF-LB

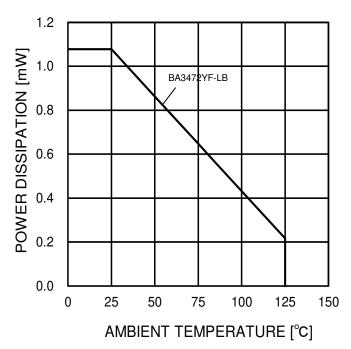


Figure 2.
Derating Curve

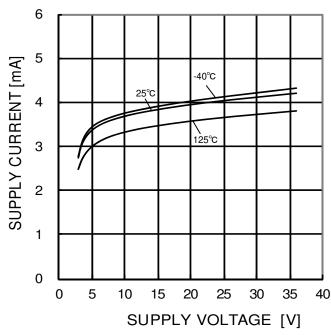


Figure 3.
Supply Current - Supply Voltage

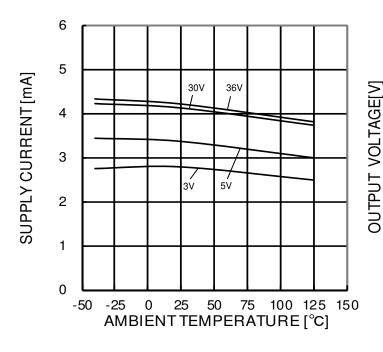


Figure 4.
Supply Current - Ambient Temperature

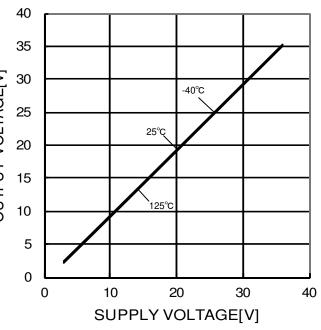


Figure 5.

Maximum Output Voltage(High)
- Supply Voltage
(RL=10k $\Omega$ )

OBA3472YF-LB

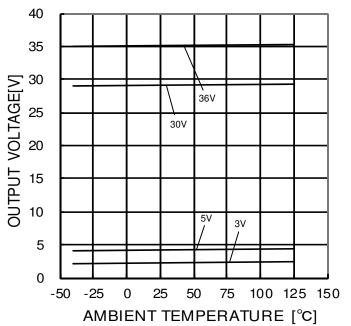


Figure 6.
Maximum Output Voltage(High)
- Ambient Temperature
(RL=10kΩ)

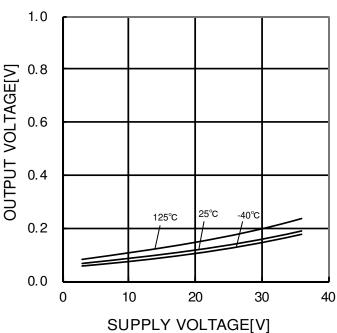


Figure 7.

Maximum Output Voltage(Low)
- Supply Voltage
(RL=10kΩ)

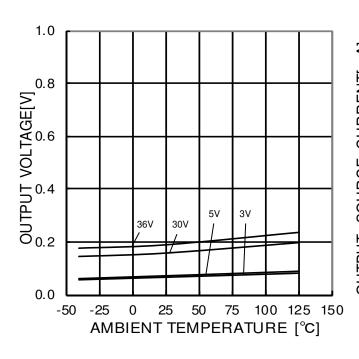


Figure 8.
Maximum Output Voltage(Low)
- Ambient Temperature
(RL=10kΩ)

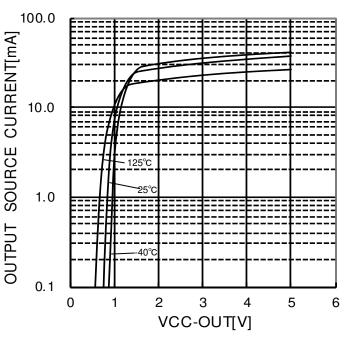


Figure 9.
Output Source Current - (VCC-OUT)
(VCC/VEE=5V/0V)

OBA3472YF-LB

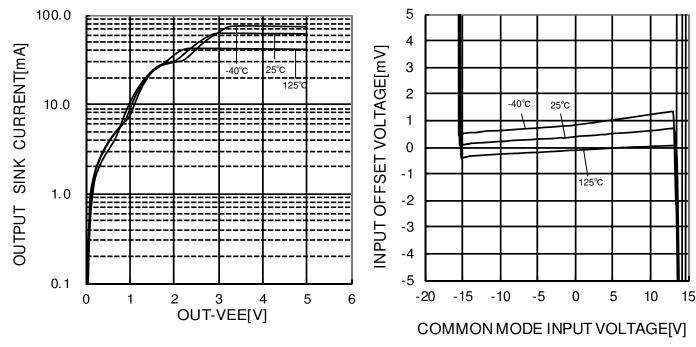


Figure 10.
Output Source Current - (OUT-VEE)
(VCC/VEE=5V/0V)

Figure 11.
Input Offset Voltage
- Common Model Input Voltage
(VCC/VEE=15V/-15V)

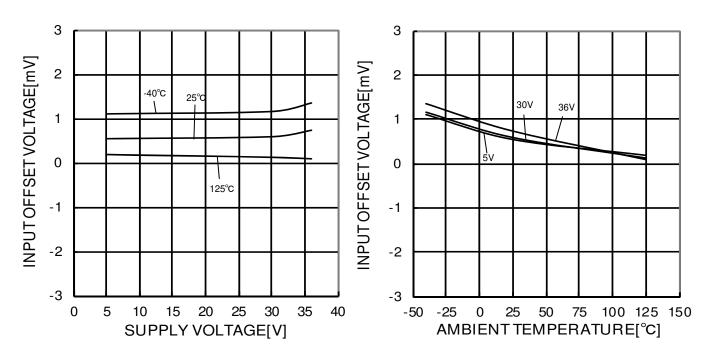
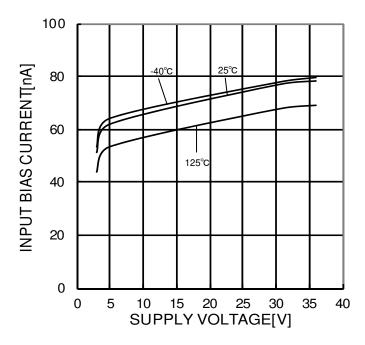


Figure 12.
Input Offset Voltage - Supply voltage

Figure 13.
Input Offset Voltage - Ambient Temperature

OBA3472YF-LB



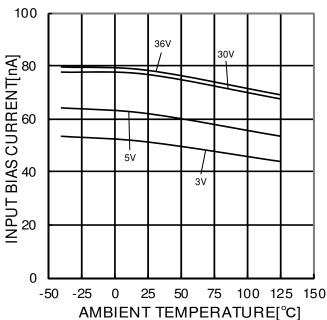


Figure 14.
Input Bias Current - Supply Voltage

Figure 15.
Input Bias Current - Ambient Temperature

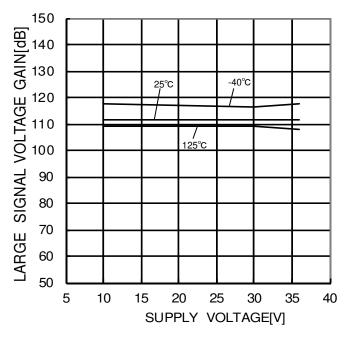


Figure 16. Large Signal Voltage Gain - Supply Voltage

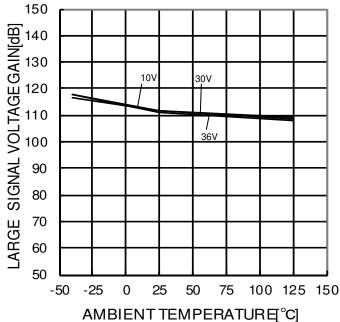


Figure 17.
Large Signal Voltage Gain
- Ambient Temperature

OBA3472YF-LB

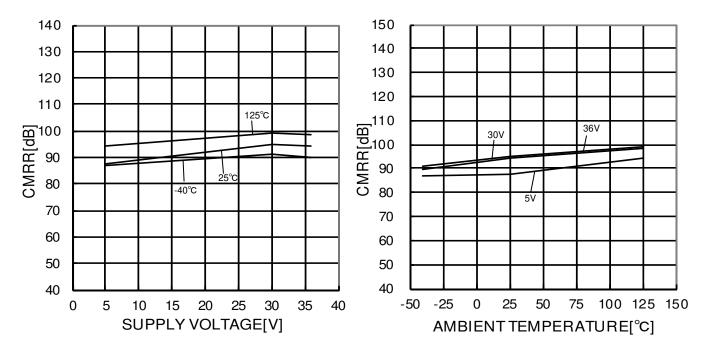


Figure 18.
Common Mode Rejection Ratio
- Supply Voltage

Figure 19.
Common Mode Rejection Ratio
- Ambient Temperature

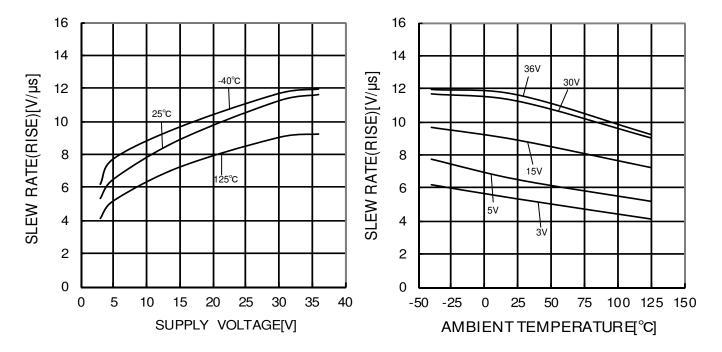
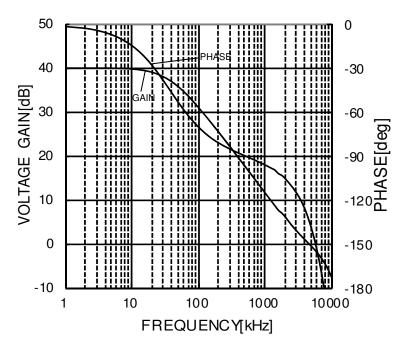


Figure 20. Slew Rate L-H - Supply Voltage  $(RL=10k\Omega)$ 

Figure 21. Slew Rate L-H Ambient Temperature  $(RL=10k\,\Omega)$ 

OBA3472YF-LB



12 10 INPUT/OUTPUT VOLTAGE[V] 8 6 OUTPUT 4 INPÚT 2 0 -2 -4 -6 -8 -10 -12 1 2 3 4 5 7 8 0 6 TIME[µs]

Figure 22.
Voltage Gain • Phase - Frequency (VCC/VEE=+15V/-15V, Av=40dB RL=2kΩ, CL=100pF, Ta=25°C)

Figure 23. Input / Output Voltage - Time (VCC/VEE=+15V/-15V, Av=0dB, RL= $2k\Omega$ , CL=100pF, Ta= $25^{\circ}C$ )

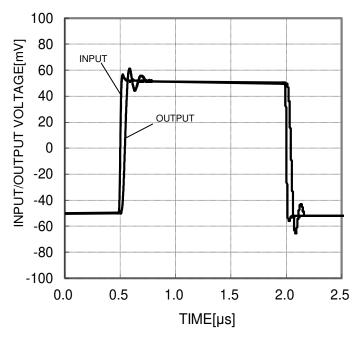


Figure 24.

Input / Output Voltage - Time (VCC/VEE=+15V/-15V, Av=0dB, RL= $2k\Omega$ , CL=100pF, Ta= $25^{\circ}C$ )

6

# Application Information NULL method condition for Test circuit1

							VCC, \	/EE, EK,	Vicm Unit: V
Parameter	VF	S1	S2	S3	VCC	VEE	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	VF2	OFF	OFF	OFF	15	-15	0	0	2
Input Pigg Current	VF3	OFF	ON	OFF	15	-15	0	0	3
Input Bias Current	VF4	ON	OFF	OFF	15				
Large Signal Voltage Cain	VF5	ON	ON	ON	15	-15	+10	0	4
Large Signal Voltage Gain	VF6 ON		ON	ON	15	-15	-10	0	4
Common-mode Rejection Ratio	VF7	ON	ON	OFF	15	-15	0	-15	5
(Input Common-mode Voltage Range)	VF8	ON	ON	OFF	15	-15	0	13	5
	VF9				2	-2	0	0	

ON

OFF

18

ON

VF10

-Calculation-

1. Input Offset Voltage (Vio)

Power Supply Rejection Ratio

$$Vio = \frac{\left| VF1 \right|}{1 + RF/RS} \quad [V]$$

2. Input Offset Current (lio)

$$lio = \frac{|VF2-VF1|}{Ri \times (1+RF/RS)} [A]$$

3. Input Bias Current (lb)

$$lb = \frac{\left| VF4 - VF3 \right|}{2 \times Ri \times (1 + RF / RS)} \quad [A]$$

4. Large Signal Voltage Gain (Av)

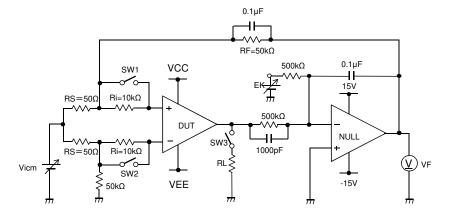
$$Av = 20 \times Log \frac{\Delta EK \times (1 + RF/RS)}{\mid VF5 - VF6 \mid} \quad [dB]$$

5. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20 \times Log \frac{\Delta Vicm \times (1 + RF/RS)}{ \mid VF8 - VF7 \mid} \quad [dB]$$

6. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20 \times Log \frac{\Delta Vcc \times (1 + RF/RS)}{\left| \ VF10 - VF9 \ \right|} \quad [dB]$$



-18

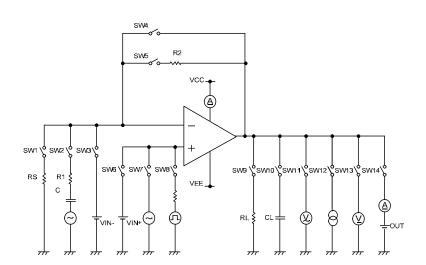
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0

Figure 25. Test circuit1 (one channel only)

# **Switch Condition for Test Circuit 2**

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage High	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Maximum Output Voltage Low	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF



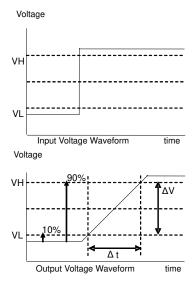


Figure 26. Test Circuit 2 (each Op-Amp)

Figure 27. Slew rate input output wave

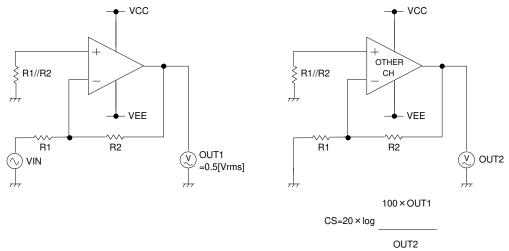


Figure 28. Test circuit 3(Channel Separation)

# **Examples of circuit**

OVoltage follower

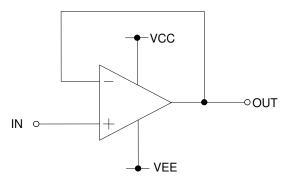


Figure 29. Voltage follower circuit

Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

OUT=IN

# OInverting amplifier

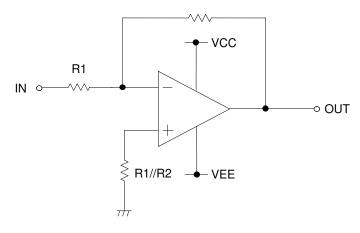


Figure 30. Inverting amplifier circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

OUT=-(R2/R1) · IN

This circuit has input impedance equal to R1.

# ONon-inverting amplifier

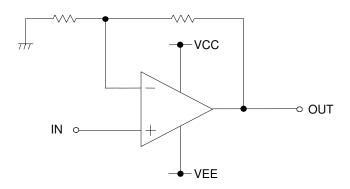


Figure 31. Non-inverting amplifier circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

OUT=(1 + R2/R1) · IN

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

# **Power Dissipation**

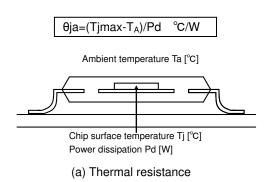
Power dissipation (total loss) indicates the power that the IC can consume at  $T_A=25^{\circ}$ C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.

Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θja°C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.

Figure 32(a) shows the model of the thermal resistance of the package. The equation below shows how to compute for the Thermal resistance ( $\theta$ <sub>ja</sub>), given the ambient temperature (T<sub>A</sub>), junction temperature (T<sub>j</sub>), and power dissipation (Pd).

$$\theta_{ia} = (T_{imax} - T_{A}) / Pd$$
 °C/W • • • • • (I)

The Derating curve in Figure 32(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance ( $\theta$ ja), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 33(c) shows an example of the derating curve for BA3472YF-LB.



Pd (max)
θja2 < θja1

θ' ja2
θ ja2

σ' ja1 θ ja1

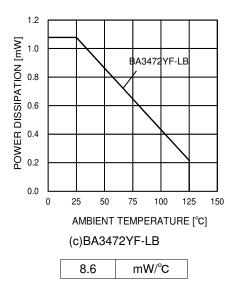
σ' ja2 η ja2

σ' ja2 η ja2 η ja2 η ja2

σ' ja2 η ja

Power dissipation of LSI [W]

Figure 32. Thermal resistance and derating curve



When using the unit above  $T_A=25^{\circ}\text{C}$ , subtract the value above per degree  $^{\circ}\text{C}$ . Mounted on a FR4 glass epoxy 4 layers PCB 70mm  $\times$  70mm  $\times$  1.6mm (occupied copper area : 70mm  $\times$  70mm).

Figure 33. Derating curve

# **Operational Notes**

#### 1) Unused circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 31, setting the non-inverting input terminal to a potential within the in-phase input voltage range (Vicm).

# 2) Input voltage

Applying VEE +36V to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

# 3) Power supply (single / dual)

The op-amp operates when the voltage supplied is between VCC and VEE. Therefore, the single supply op-amp can be used as dual supply op-amp as well.

# Connect to Vicm VEE

Figure 31
Example of application circuit for unused op-amp

# 4) Power dissipation Pd

Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics including reduced current capability due to the rise of chip temperature. Therefore, please take into consideration the power dissipation (Pd) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

# 5) Short-circuit between pins and erroneous mounting

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

# 6) Operation in a strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

#### 7) Radiation

This IC is not designed to withstand radiation.

#### 8) IC handling

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations of the electrical characteristics due to piezo resistance effects.

# 9) Board inspection

Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, make sure that the power is turned OFF before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

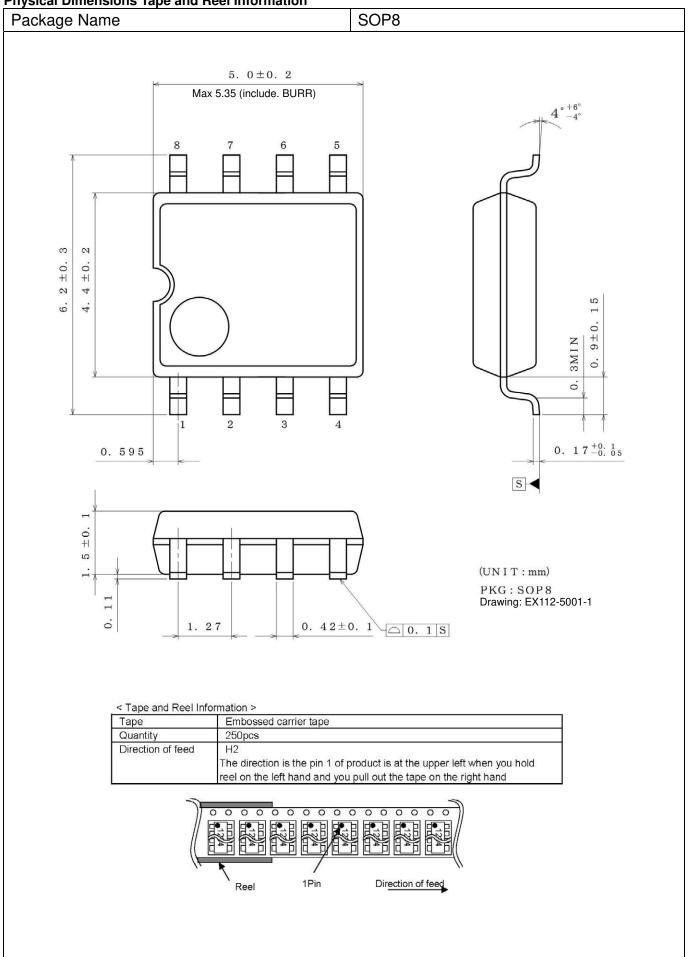
# 10) Output capacitor

If a large capacitor is connected between the output pin and GND pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VCC or VIN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 1uF between output and GND.

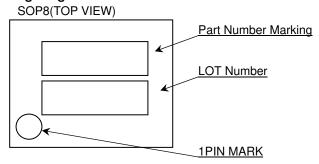
#### 11) Oscillation by output capacitor

Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these ICs.

**Physical Dimensions Tape and Reel Information** 



# **Marking Diagrams**

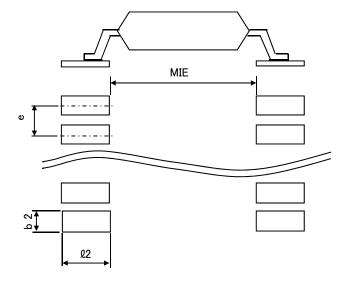


Product Name		Package Type	Marking
BA3472Y	F	SOP8	3472Y

# Land pattern data

All dimensions in mm

			7111 0	
PKG	PKG Land pitch e		Land length ≧ℓ 2	Land width b2
SOP8	1.27	4.60	1.10	0.76



**Revision History** 

Date	Revision	Changes						
16.Dec.2013	001	New Release						
30.Jan.2014	002	The feature is updated in Page1.						

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA		
CLASSIII	CL ACC III	CLASSIIb	СГАССШ		
CLASSIV	CLASSⅢ	CLASSIII	CLASSⅢ		

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  - [f] Sealing or coating our Products with resin or other coating materials
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  - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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- Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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