19-1098; Rev 2; 10/02

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX525 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX525 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and MICROWIRE™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated through the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- ♦ **Four 12-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation; 10µA Shutdown Mode**
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **Capable of Recalling Last State Prior to Shutdown**
- ♦ **SPI/QSPI and MICROWIRE Compatible**
- ♦ **Simultaneous or Independent Control of DACs through 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**

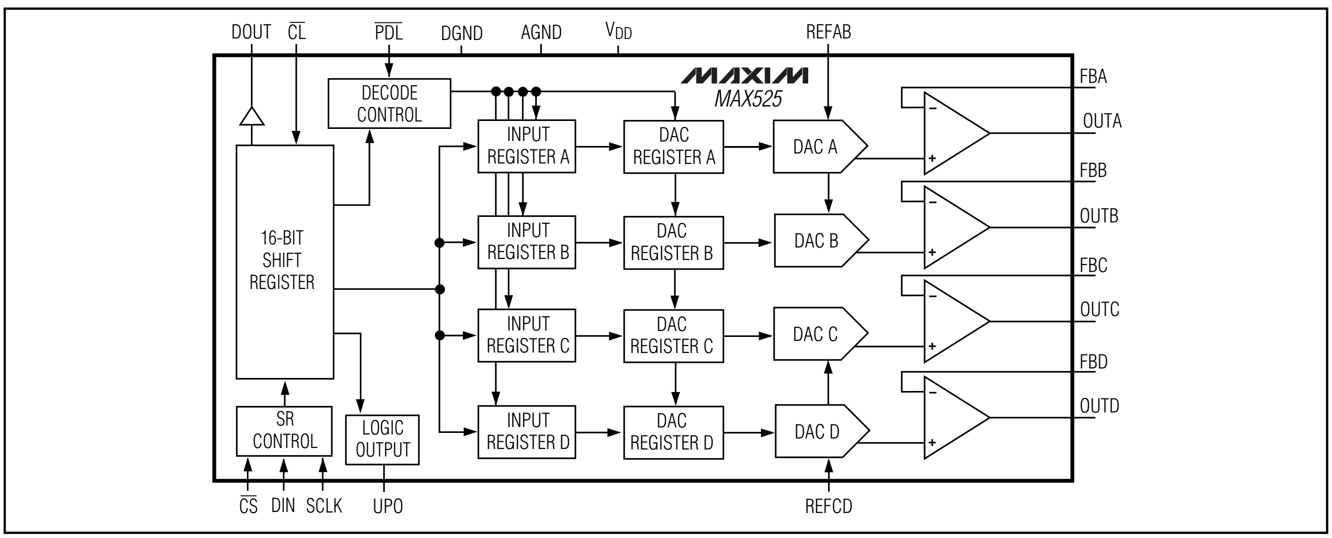
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX525ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX525BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX525ACAP	0°C to +70°C	20 SSOP	±1/2
MAX525BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued at end of data sheet.

Pin Configuration appears at end of data sheet.

Functional Diagram



Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ....-0.3V to +6V
V_{DD} to DGND ....-0.3V to +6V
AGND to DGND ....±0.3V
REFAB, REFCD to AGND ....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND ....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ....-0.3V to +6V
DOUT, UPO to DGND ....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin.....................................±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C).................889mW

Operating Temperature Ranges
MAX525_C_P ....0°C to +70°C
MAX525_E_P ....-40°C to +85°C
MAX525_MJP ....-55°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX525A		±0.25	±0.5	LSB
		MAX525B			±1.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error	GE	(Note 1)		-0.8	±2.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		100	600	µV/V
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE			-0.8	±2.0	LSB
Offset Error				±1.0	±6.0	mV
Integral Nonlinearity	INL			±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555 hex	8			kΩ
Reference Current in Shutdown				0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67V_{P-P}		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6V_{P-P} at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1V_{P-P} at 25kHz		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		12		µs
Output Voltage Swing		Rail-to-Rail® (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				15		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.85	0.98	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Accuracy is better than 1.0LSB for V_{OUT} = 6mV to V_{DD} - 60mV, guaranteed by PSR test on end points.
Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

ELECTRICAL CHARACTERISTICS (continued)

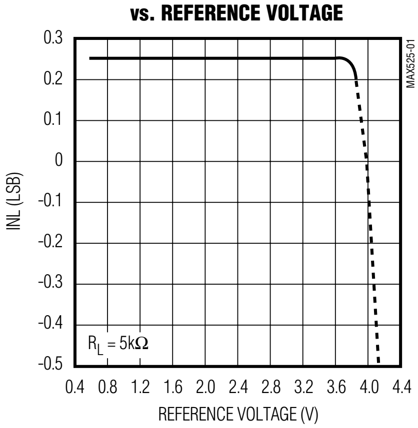
(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

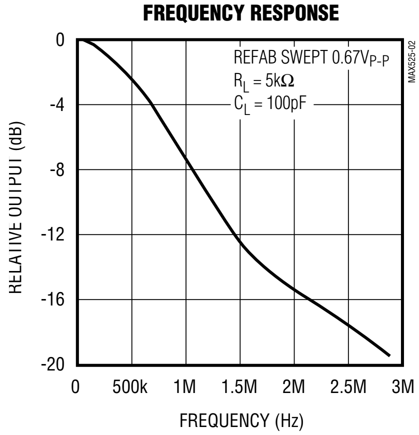
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

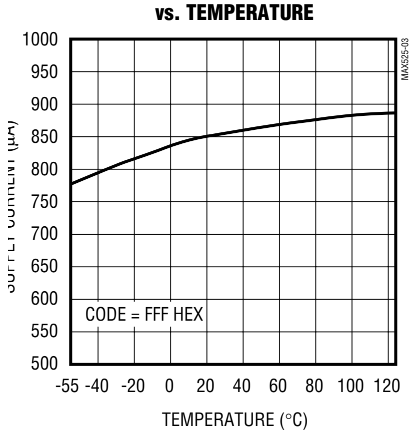
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

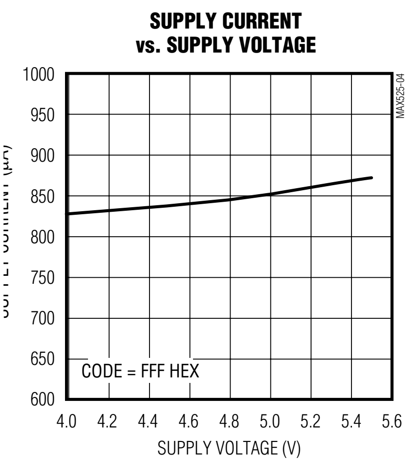


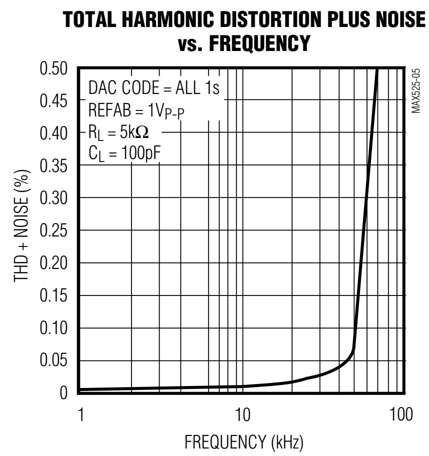
SUPPLY CURRENT vs. TEMPERATURE

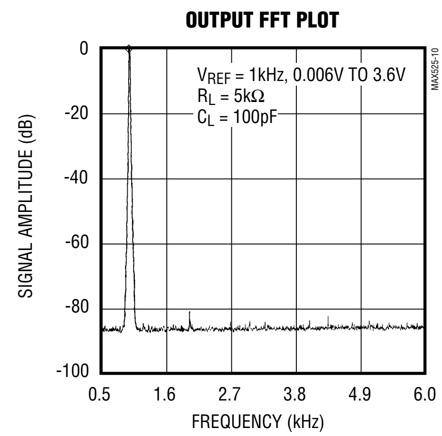


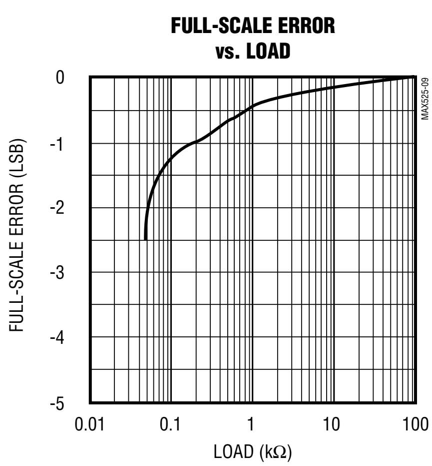
Typical Operating Characteristics (continued)

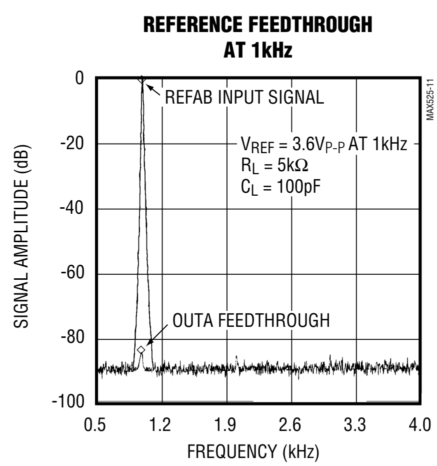
(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)









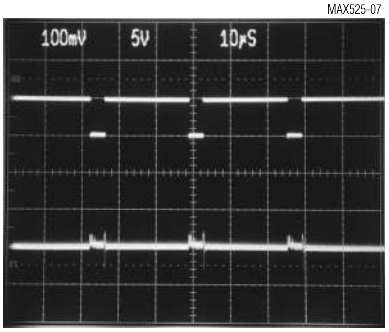


Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

MAJOR-CARRY TRANSITION

MAX525-07

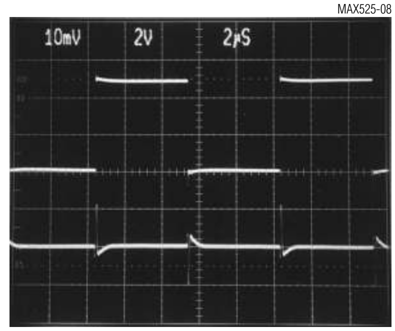


10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF

DIGITAL FEEDTHROUGH (SCLK = 100kHz)

MAX525-08

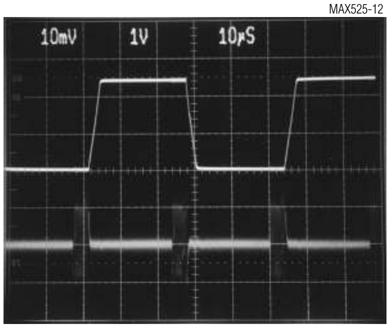


2µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 5V, DIN = 0V
DAC A CODE SET TO 800 HEX

ANALOG CROSSTALK

MAX525-12

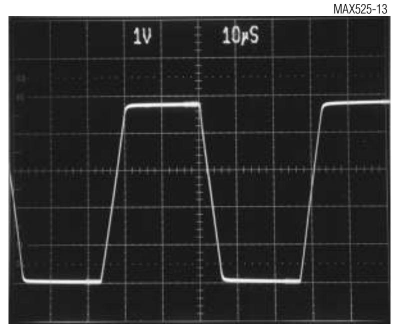


10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
DAC A CODE SWITCHING FROM 00B HEX TO FFF HEX
DAC B CODE SET TO 800 HEX

DYNAMIC RESPONSE

MAX525-13



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 HEX TO FB4 HEX
OUTPUT AMPLIFIER GAIN = +2

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clear All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

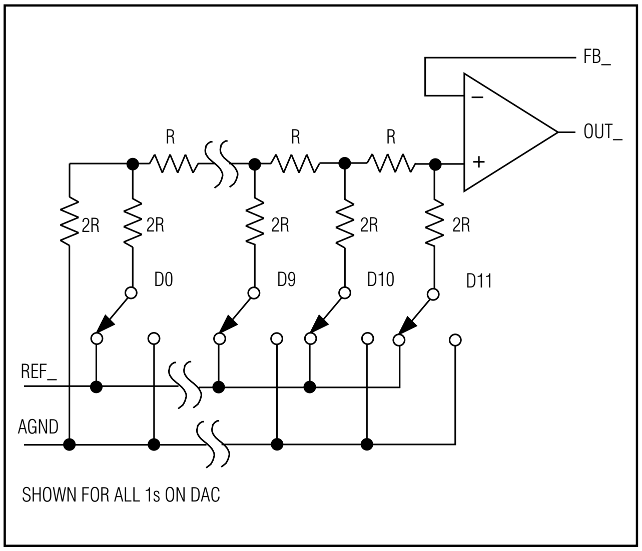


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX525 contains four 12-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 555 hex, to a high value exceeding several gigohms (leakage currents) with an input code of 000 hex. Because the input impedance at the reference pins is code-dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.025LSB (0.061LSB worst case) when driving both MAX525 reference inputs simultaneously at 2.5V. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX525's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All MAX525 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX525 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX525 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Power-Down Mode

The MAX525 features a software-programmable shutdown that reduces supply current to a typical value of 10µA. The power-down lockout ($\overline{PDL}$) pin must be high to enable the shutdown mode. Writing 1100XXXXXXXXXXXX as the input-control word puts the MAX525 in power-down mode (Table 1).

In power-down mode, the MAX525 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in power-down, allowing the MAX525 to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 15µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX525's 3-wire serial interface is compatible with both MICROWIRE (Figure 2) and SPI/QSPI (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX525's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX525's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX525's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX525 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 12 data bits D11...D0 (Figure 4). The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out through the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when coming out of shutdown mode.

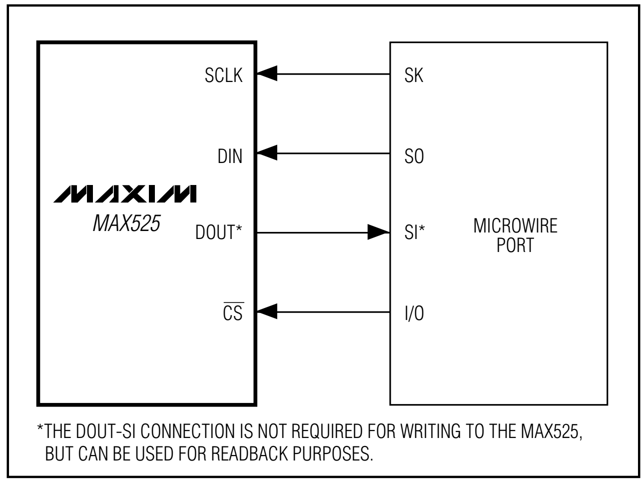


Figure 2. Connections for Microwire

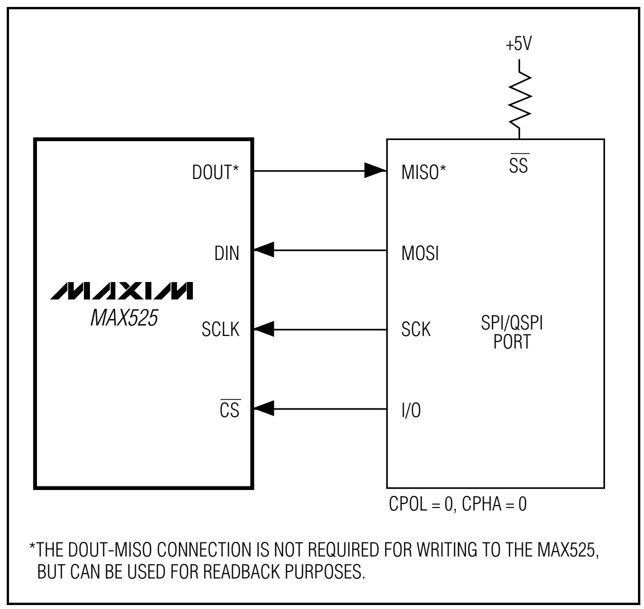


Figure 3. Connections for SPI/QSPI

MSB ....LSB		
←16 Bits of Serial Data→		
Address Bits	Control Bits	Data Bits MSB ....LSB
A1 A0	C1 C0	D11 ....D0
←4 Address/Control Bits→		←12 Data Bits→

Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.................D0 MSB LSB	
0 0 1 1	0 1 0 1	0 0 0 0	1 1 1 1	12-bit DAC data 12-bit DAC data 12-bit DAC data 12-bit DAC data	Load input register A; DAC registers unchanged. Load input register B; DAC registers unchanged. Load input register C; DAC registers unchanged. Load input register D; DAC registers unchanged.
0 0 1 1	0 1 0 1	1 1 1 1	1 1 1 1	12-bit DAC data 12-bit DAC data 12-bit DAC data 12-bit DAC data	Load input register A; all DAC registers updated. Load input register B; all DAC registers updated. Load input register C; all DAC registers updated. Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (start-up).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (start-up).
1	1	0	0	XXXXXXXXXXXX	Shutdown (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register through the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX525 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX525 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX525 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with MICROWIRE, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled through the MAX525 serial interface (Table 1).

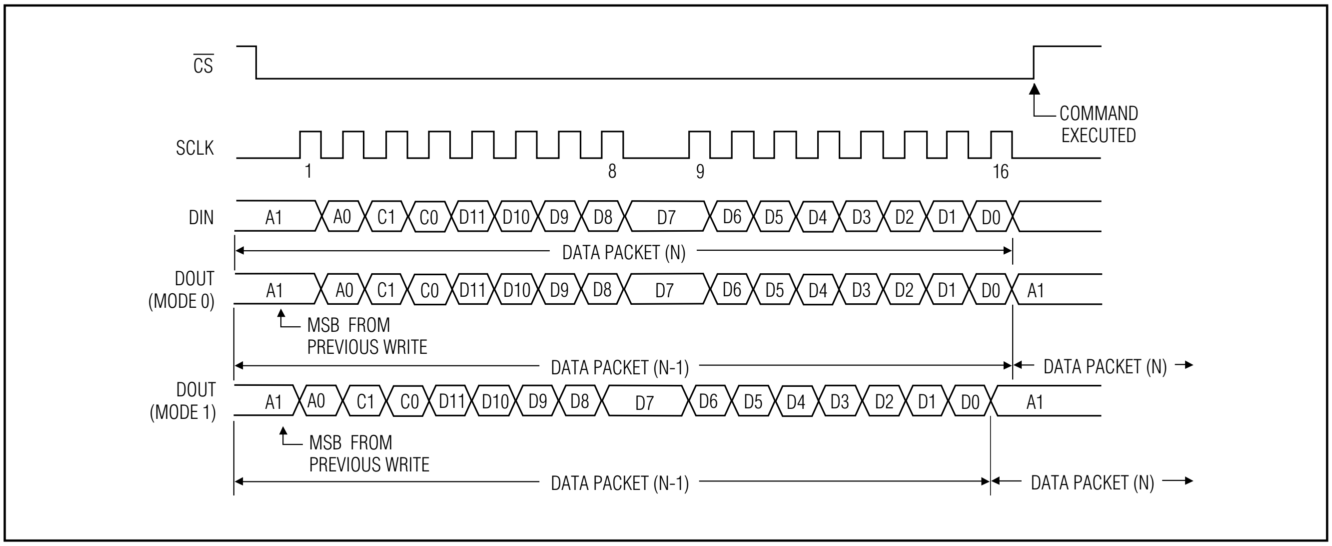


Figure 5. Serial-Interface Timing Diagram

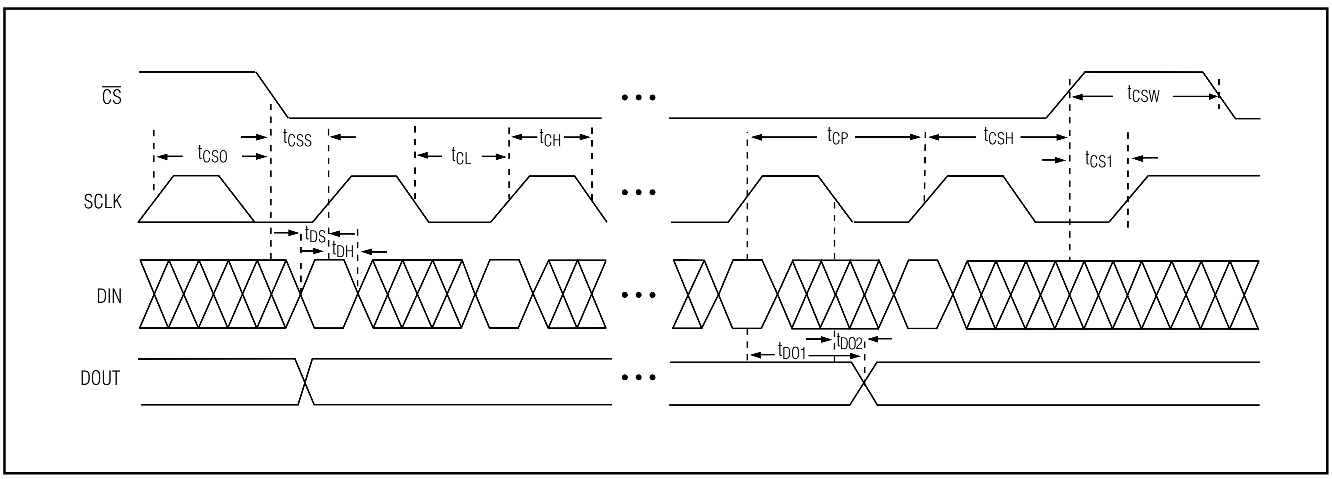


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout (PDL)

The power-down lockout pin PDL disables software shutdown when low. When in shutdown, transitioning PDL from high to low wakes up the part with the output set to the state prior to shutdown. PDL could also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX525s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX525's DOUT pin has an internal active pullup, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Figure 8 shows an alternate method of connecting several MAX525s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input (CS) is required for each IC.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

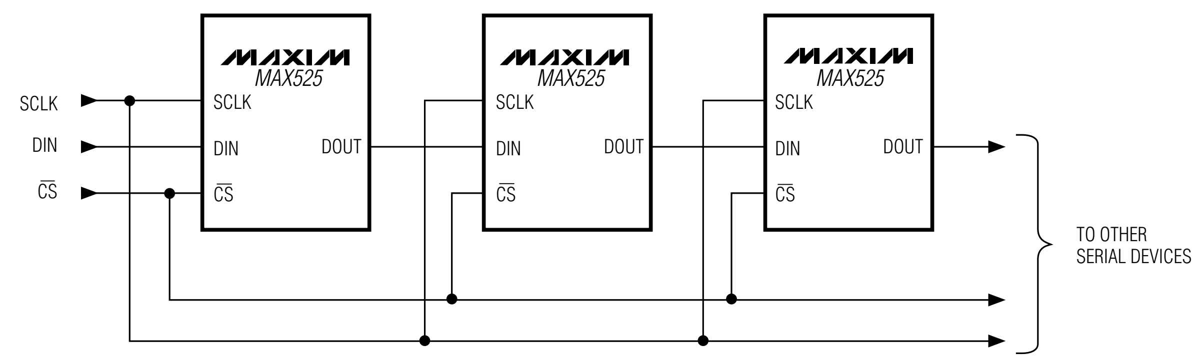


Figure 7. Daisy-Chaining MAX525s

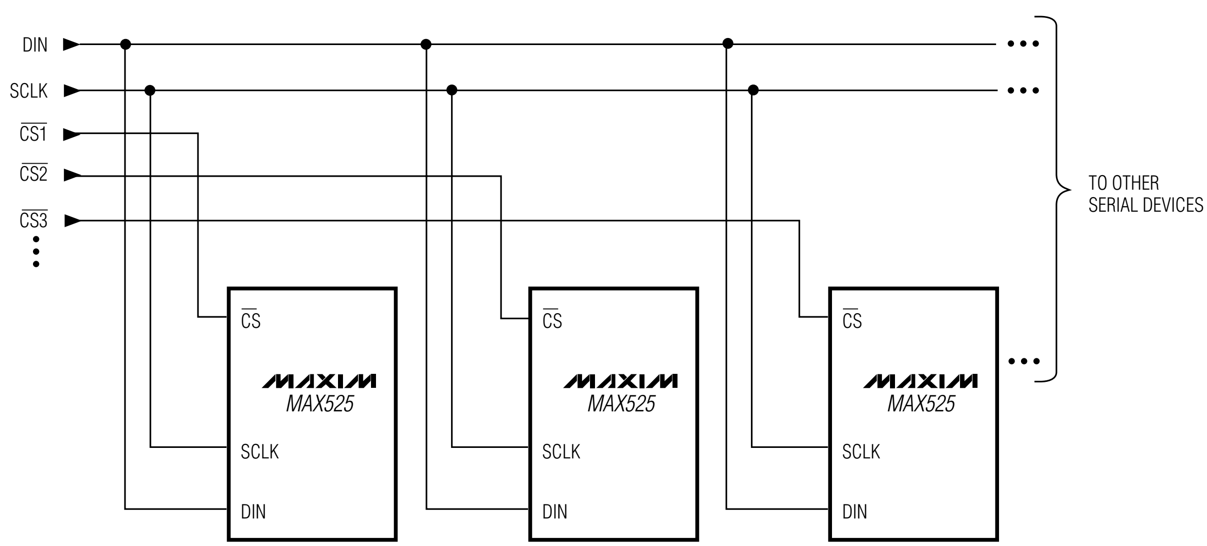


Figure 8. Multiple MAX525s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX525 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX525 with the output amplifiers configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF} \left(\frac{4095}{4096}\right)$
1000	0000	0001	$+V_{REF} \left(\frac{2049}{4096}\right)$
1000	0000	0000	$+V_{REF} \left(\frac{2048}{4096}\right) = \frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF} \left(\frac{2047}{4096}\right)$
0000	0000	0001	$+V_{REF} \left(\frac{1}{4096}\right)$
0000	0000	0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF} \left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF} \left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{REF} \left(\frac{1}{2048}\right)$
0000	0000	0001	$-V_{REF} \left(\frac{2047}{2048}\right)$
0000	0000	0000	$-V_{REF} \left(\frac{2048}{2048}\right) = -V_{REF}$

Note: $1LSB = (V_{REF}) \left(\frac{1}{4096}\right)$

Bipolar Output

The MAX525 outputs can be configured for bipolar operation using Figure 11's circuit.

$$V_{OUT} = V_{REF} [(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

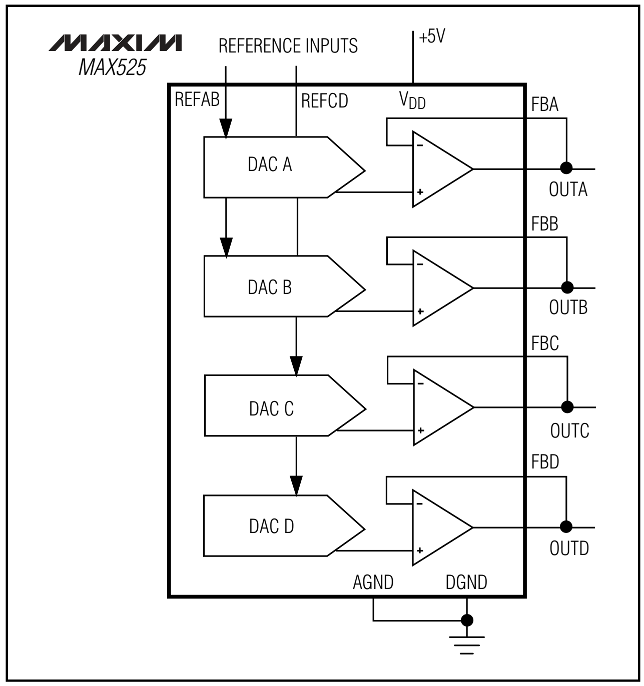


Figure 9. Unipolar Output Circuit

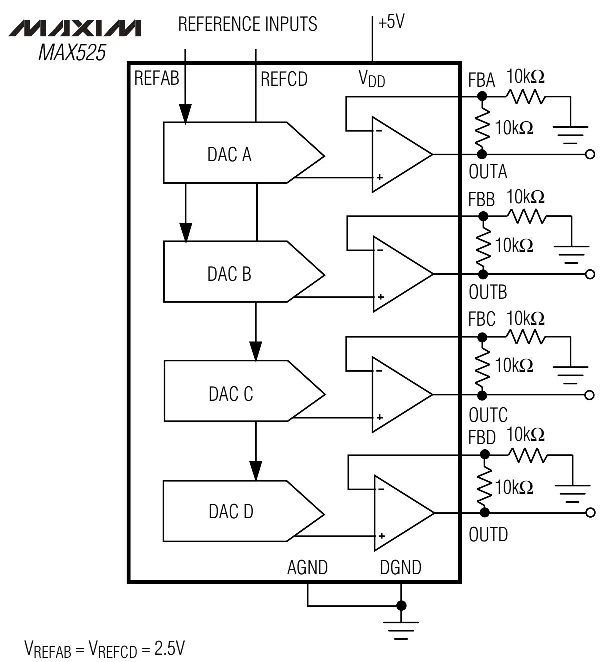


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX525 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX525's total harmonic distortion plus noise (THD + N) is typically less than -72dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

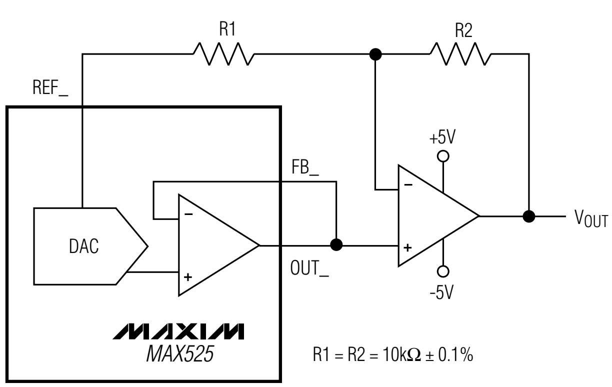


Figure 11. Bipolar Output Circuit

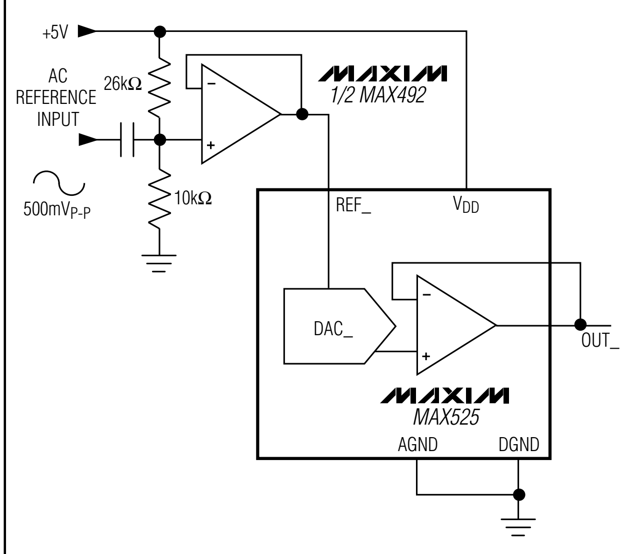


Figure 12. AC Reference Input Circuit

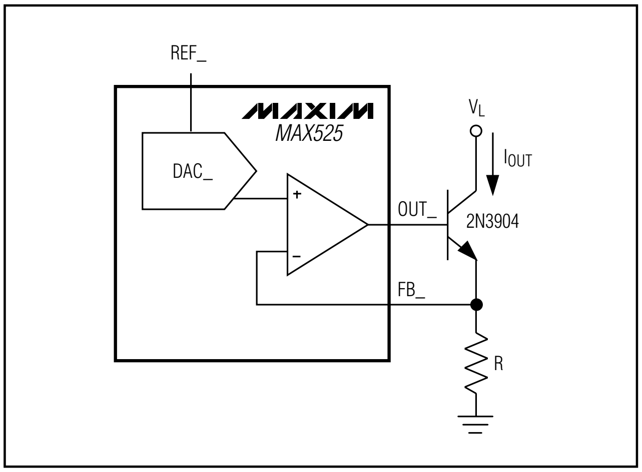


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

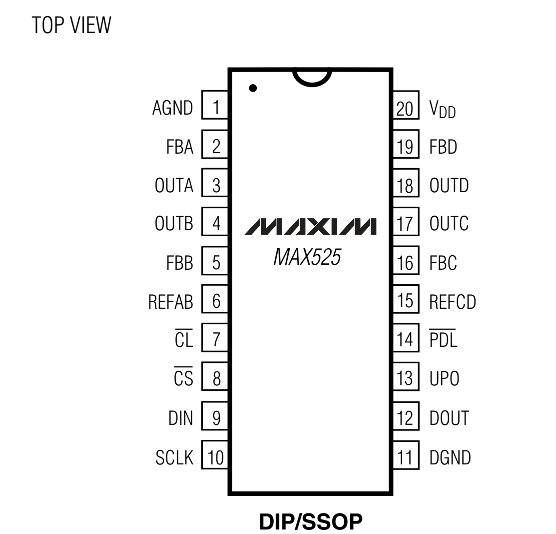
For rated MAX525 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSBs)
MAX525BC/D	0°C to +70°C	Dice*	±1
MAX525AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX525BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX525AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX525BEAP	-40°C to +85°C	20 SSOP	±1
MAX525AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX525BMJP	-55°C to +125°C	20 CERDIP**	±1

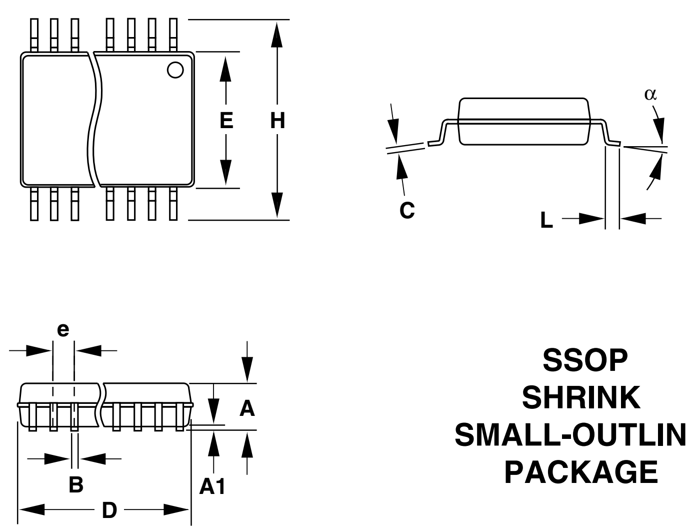
** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 4337

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0˚	8˚	0˚	8˚

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

SSOP SHRINK SMALL-OUTLINE PACKAGE

21-0056A

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