



MC92604

The MC92604 Dual Gigabit Ethernet transceiver is a 1.25 giga-baud, full-duplex, interface device that can be used to transmit data between chips across a board, through a backplane, or through cabling, as well as to interface to GBIC/SFP modules. It was designed with the intent to meet the requirements of IEEE Std. 802.3-2002*.

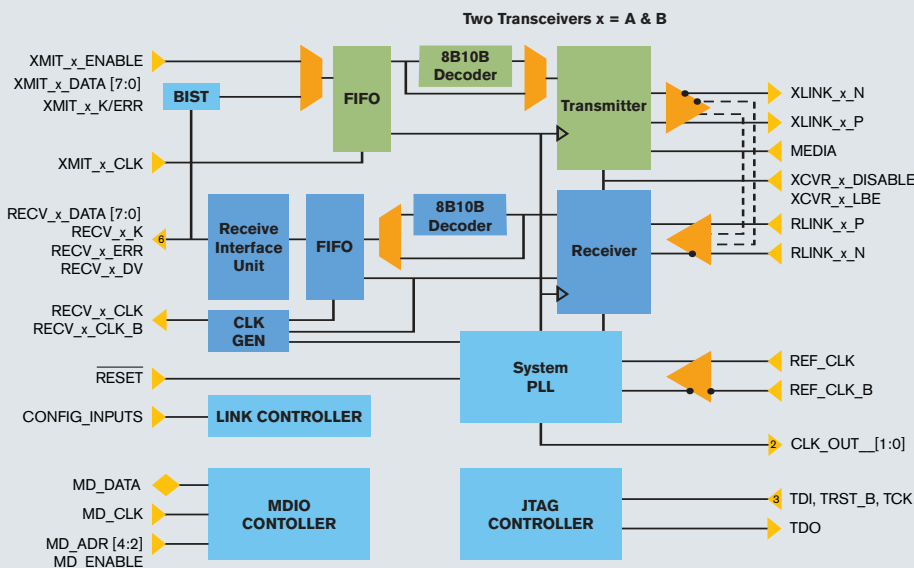
The MC92604 is two parts in one. It may be configured as either a dual channel 1 gigabit backplane serializer/deserializer, SerDes, or it is a dual 1 gigabit GMII or TBI PHY for Ethernet 1000Base-X applications. The dual MC92604 may optionally be configured as a single channel transceiver with serial link redundancy. The device fully supports the MDIO interface defined in the above referenced standard.

The MC92604 features transmit FIFOs and source-synchronous transmit clocks per channel to further simplify interfacing that will support many other non-Ethernet applications. And finally, IEEE Std 1149.1 JTAG boundary scan is added for board test support.

The Gigabit Ethernet transceiver is carefully designed for low power consumption and is built upon the proven transceiver technology in the MC92600 and MC92602 Quad SerDes devices. The MC92604 transceiver is offered in a JEDEC standard 196 pin 15 mm body size package to provide excellent board density in applications with a large number of channels.

MC92604 DUAL GIGABIT ETHERNET TRANSCEIVER BLOCK DIAGRAM

(As a single with redundancy, only channel A is used.)



Typical applications

- > High-density board applications for communications designs utilizing IEEE 802.3 protocol
- > High-speed data transfer applications in high-bandwidth backplane and chassis-to-chassis networking
- > PHY interface to Motorola C-port (C-3e or C-5e) network processors and Power QUICC III (MPC8560 or MPC8540) communications processors



Common features

- > Independent SerDes channels with full-duplex differential data links
- > Configurable as a single channel device to provide redundant transmit and receive serial links
- > Selectable speed range: 1.25 Gbaud or 0.625 Gbaud
- > Internal 8B/10B encoder/decoders
- > Source synchronous parallel data input interfaces
- > Selectable source-synchronous or source-centered timing on receiver interface
- > Links drive 50-ohm or 75-ohm media (100- or 150-ohm differential), backplane or cable
- > Link inputs have on-chip receiver link termination and are "hot-swap" compatible
- > Low power: <0.6 W, under typical conditions, while operating in backplane mode with all transceivers at full speed
- > Unused transceiver channels may be individually disabled to reduce power consumption

- > IEEE Std 1149.1 JTAG support and full-speed built-in self test functions

Backplane application features

- > Link-to-link synchronization supports aligned, multi-channel, word transfers. Synchronization mechanism tolerates up to 40 bit-times of link-to-link media delay skew
- > Supports Disparity Based Word Sync Events for compatibility with legacy transceivers
- > Selectable COMMA code group alignment mode enables aligned or unaligned transfers

Ethernet friendly features

- > GMII, TBI, RGMII or RTBI data interface options
- > COMMA code group alignment in receivers
- > Provides the PCS and PMA layers for Ethernet PHYs as specified in IEEE Std. 802.3-2002
- > MDIO slave interface and registers as defined in IEEE Std. 802.3-2002 is fully supported
- > MDIO interface is available in all operating modes

Technical specifications

- > All channels have:
 - 8B/10B encoder/decoder that can be enabled or bypassed in Ten-Bit Interface (TBI) mode
 - Clock generation/recovery
 - Independent 8/10-bit or 4/5-bit system I/F with parallel-to-serial, serial-to-parallel conversion
- > Transmit data clock is selectable between per-channel transmit clock or channel 'A' transmit clock
- > Received data may be clocked at the recovered clock or the reference clock frequencies
- > Half frequency, split-phase recovered clock in TBI (10-bit) mode
- > Transceiver Links operate over 50-ohm or 75-ohm media (100- or 150-ohm differential) for lengths of up to 1.5 meters of FR-4 board/back-plane, or 10 meters of coax
- > No external loop filter components required
- > System BIST test modes with error counter
- > Loopback BIST isolated from link inputs and outputs
- > IEEE Std 1149.1 JTAG boundary scan support
- > LVPECL differential reference clock input with single-ended LVTTTL reference clock input option
- > Two single ended buffered Ref Clock outputs provided for associated logic interfaces
- > Frequency offset tolerance between transmitter and receiver in excess of ± 250 ppm

Parametrics

- > Power Supply
 - Core Power Supply: 1.8 V \pm 0.15 Vdc
 - Data I/O Power Supply: (LVTTTL) 3.3 V \pm 0.10 Vdc or (SSTL-2) 2.5 V \pm 0.20 Vdc
 - Link I/O Power Supply: 1.8 V \pm 0.15 Vdc
- > Power Dissipation
 - Typical operation at maximum speed: <250 mW per channel in backplane mode <350 mW per channel in Ethernet mode

Package

- > 196 pin MAPBGA (15x15 mm body size, 1.0 mm ball pitch)

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