TS5A2066 Dual-Channel 10-Ω SPST Analog Switch

1 Features

- Low ON-State Resistance (10 Ω)
- Control Inputs Are 5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits
- Cell Phones
- Low-Voltage Data-Acquisition Systems
- PDAs

3 Description

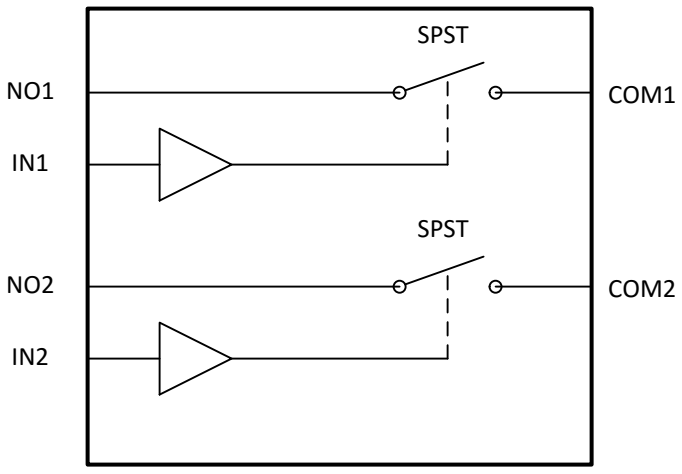
The TS5A2066 device is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_{CC} can be transmitted in either direction.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A2066	SSOP (DCT)	2.95 mm x 2.80 mm
	VSSOP (DCU)	2.30 mm x 2.00 mm
	DSBGA (YZP)	1.25 mm x 2.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2017) to Revision F **Page**

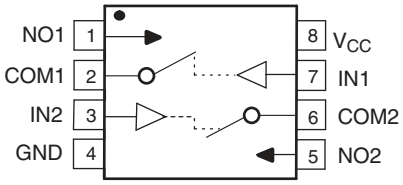
- Changed the YZP Package From: Top View To: Bottom View ... 3

Changes from Revision D (April 2010) to Revision E **Page**

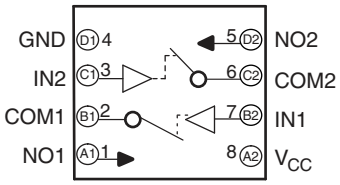
- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted the *Summary of Characteristics* table ... 3
- Changed pin 8 From: V_+ To: V_{CC} in the pinout images ... 3
- Deleted the ON-state resistance Min values of 10 Ω and 12 Ω in the *Electrical Characteristics For 3.3-V Suppy* table ... 7
- Deleted the ON-state resistance Min values of 20 Ω in the *Electrical Characteristics For 2.5-V Supply* table ... 9
- Changed Test Conditions for Charge injection From: See Figure 23 To; See Figure 24 in the *Electrical Characteristics For 2.5-V Supply* table ... 10
- Deleted the ON-state resistance Min values of 80 Ω and 90 Ω in the *Electrical Characteristics For 1.8-V Supply* table ... 11
- Changed V_+ to V_{CC} in the *Typical Performance* graphs ... 13
- Changed V_+ to V_{CC} in the *Parameter Measurement Information* images ... 16

5 Pin Configuration and Functions

DCT or DCU Package
8 Pin (SSOP or VSSOP)
Top View



YZP Package
8 Pin (DSBGA)
Bottom View



Pin Functions

NO.	NAME	DESCRIPTION
1	NO1	Normally open
2	COM1	Common
3	IN2	Digital control to connect COM to NO
4	GND	Digital ground
5	NO2	Normally open
6	COM2	Common
7	IN1	Digital control to connect COM to NO
8	V_{CC}	Power supply

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(3)(4)(5)		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_{CC}	–50	50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–50	50	mA
V_{IN}	Digital input voltage range(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	1.65	5.5	V
V_{NO} V_{COM}	Analog voltage range	0	V_{CC}	V
V_{IN}	Digital input voltage range	0	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		TS5A2066			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.1	212.8	99.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.8	93.6	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	127.8	133.6	29.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.2	30.4	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	125.5	133.1	29.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics For 5-V Supply(1)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –32 mA,	Switch ON, See Figure 16	25°C	4.5 V		7.5	10	Ω
				Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 3.15 V, I_{COM} = –32 mA,	Switch ON, SeeFigure 16	25°C	4.5 V		0.4	1	Ω
				Full				3	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –32 mA,	Switch ON, See Figure 16	25°C	4.5 V		3.5	5	Ω
				Full				8	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 17	25°C	5.5 V	–30	–10	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, See Figure 17	25°C	5.5 V	–50	–8	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open	Switch ON, See Figure 18	25°C	5.5 V	–40	–12	40	nA
				Full		–4		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, See Figure 18	25°C	5.5 V	–70	–30	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_{CC} × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_{CC} × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	5.5 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics For 5-V Supply[1] (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	5 V	4.4	5.2	5.8	ns
				Full	4.5 V to 5.5 V	3.4		6.1	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	5 V	1.7	2.6	3.6	ns
				Full	4.5 V to 5.5 V	1.3		4.2	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	5 V		1		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	5 V		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	5 V		5.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	5 V		13.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	5 V		13.5		pF
Digital input capacitance	C_{IN}	V_{IN} = V_{CC} or GND,	See Figure 19	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 21	25°C	5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	5 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	5 V		0.01%		
Supply									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	5.5 V		0.1	1	µA
				Full				5	

6.6 Electrical Characteristics For 3.3-V Supply(1)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –24 mA,	Switch ON, See Figure 16	25°C	3 V		12	15	Ω
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 16	25°C	3 V		0.5	1.5	Ω
				Full				3.5	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –24 mA,	Switch ON, See Figure 16	25°C	3 V		7	8	Ω
				Full				12	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 17	25°C	3.6 V	–30	–6	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, See Figure 17	25°C	3.6 V	–50	–7	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 18	25°C	3.6 V	–40	–7	40	nA
				Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, See Figure 18	25°C	3.6 V	–70	–20	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_{CC} × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_{CC} × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics For 3.3-V Supply[1] (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V	4.9	5.6	6.4	ns
				Full	3 V to 3.6 V	4.3		7.1	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V	2	2.7	3.7	ns
				Full	3 V to 3.6 V	1.3		4.7	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	3.3 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	3.3 V		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	3.3 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	3.3 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	3.3 V		14		pF
Digital input capacitance	C_I	V_{IN} = V_{CC} or GND,	See Figure 19	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 21	25°C	3.3 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	3.3 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	3.3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	3.3 V		0.065%		
Supply									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	3.6 V		0.1	1	µA
				Full				5	

6.7 Electrical Characteristics For 2.5-V Supply(1)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_{CC}	V
ON-state resistance	r_{on}	$0 \le V_{NO} \le V_{CC}$, I_{COM} = –8 mA, Switch ON, See Figure 16	25°C	2.3 V		22		Ω
			Full				30	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.6 V, I_{COM} = –8 mA, Switch ON, SeeFigure 16	25°C	2.3 V		0.5	1.5	Ω
			Full				5	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_{CC}$, I_{COM} = –8 mA, Switch ON, See Figure 16	25°C	2.3 V		16	18	Ω
			Full				25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NO} = 2.2 V, V_{COM} = 0.5 V, Switch OFF, See Figure 17	25°C	2.7 V	–30	–5.5	30	nA
			Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.5 V, V_{NO} = 2.2 V, or V_{COM} = 2.2 V, V_{NO} = 0.5 V, Switch OFF, See Figure 17	25°C	2.7 V	–50	–7.5	50	nA
			Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.2 V, V_{COM} = Open, Switch ON, See Figure 18	25°C	2.7 V	–40	–5	40	nA
			Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.2 V, V_{NO} = Open, Switch ON, See Figure 18	25°C	2.7 V	–70	–12	70	nA
			Full		–70		70	
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		V_{CC} × 0.7		5.5	V
Input logic low	V_{IL}		Full		0		V_{CC} × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0	25°C	2.7 V	–0.1	0.05	0.1	µA
			Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics For 2.5-V Supply[1] (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V	5.7	6.4	8.1	ns
				Full	2.3 V to 2.7 V	4.4		8.5	
Turn-off time	t_{OFF}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V	2.1	3.1	4.3	ns
				Full	2.3 V to 2.7 V	1.8		4.8	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	2.5 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	2.5 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	2.5 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	2.5 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	2.5 V		14		pF
Digital input capacitance	C_{IN}	V_{IN} = V_{CC} or GND,	See Figure 19	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 21	25°C	2.5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	2.5 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	2.5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	2.5 V		0.35%		
Supply									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	2.7 V		0.1	1	µA
				Full				5	

6.8 Electrical Characteristics For 1.8-V Supply(1)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –4 mA,	Switch ON, See Figure 16	25°C	1.65 V		85		Ω
				Full				120	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 16	25°C	1.65 V		0.9	2	Ω
				Full				6	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_{CC}, I_{COM} = –4 mA,	Switch ON, See Figure 16	25°C	1.65 V		75	85	Ω
				Full				100	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 17	25°C	1.95 V	–30	–6	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.3 V, V_{NO} = 1.65 V, or V_{COM} = 1.65 V, V_{NO} = 0.3 V,	Switch OFF, See Figure 17	25°C	1.95 V	–50	–7	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 18	25°C	1.95 V	–40	7	40	nA
				Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.3 V, V_{NO} = Open, or V_{COM} = 1.65 V, V_{NO} = Open,	Switch ON, See Figure 18	25°C	1.95 V	–70	–8.5	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_{CC} × 0.65		5.5	V
Input logic low	V_{IL}			Full		0		V_{CC} × 0.35	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 5.5 V or 0		25°C	1.95 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics For 1.8-V Supply(1) (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	1.8 V	9.3	10.4	11.5	ns
				Full	1.65 V to 1.95 V	6.8		12.9	
Turn-off time	t_{OFF}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	1.8 V	3.3	4.3	5.2	ns
				Full	1.65 V to 1.95 V	2.4		6.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 24	25°C	1.8 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	1.8 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 19	25°C	1.8 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	1.8 V		14.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 19	25°C	1.8 V		14.5		pF
Digital input capacitance	C_{IN}	V_{IN} = V_{CC} or GND,	See Figure 19	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 21	25°C	1.8 V		293		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 22	25°C	1.8 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 23	25°C	1.8 V		–66		dB
Total harmonic distortion	THD	R_L = 10 kΩ, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	1.8 V		2.7%		
Supply									
Positive supply current	I_{CC}	V_{IN} = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		0.1	1	µA
				Full				5	

6.9 Typical Performance

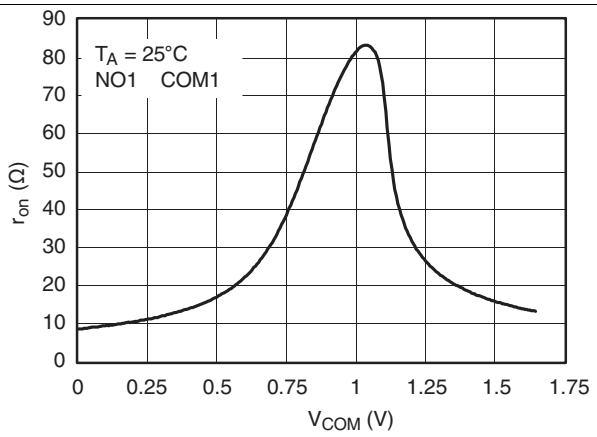


Figure 1. r_{on} vs V_{COM}

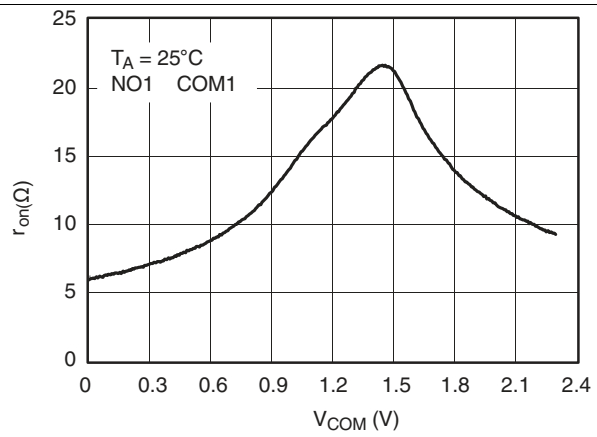


Figure 2. r_{on} vs V_{COM}

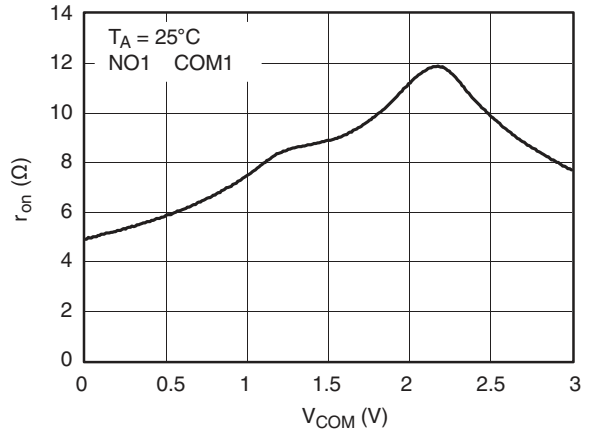


Figure 3. r_{on} vs V_{COM}

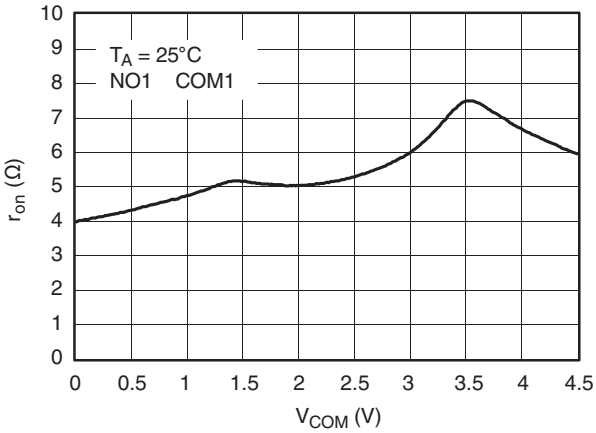


Figure 4. r_{on} vs V_{COM}

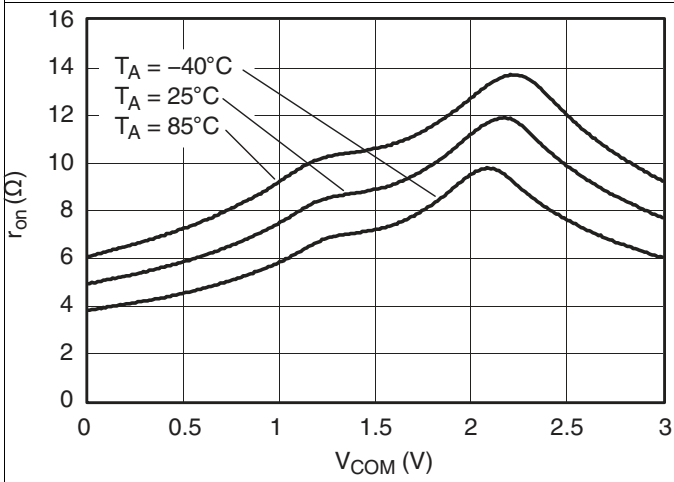


Figure 5. r_{on} vs V_{COM} (V_{CC} = 3 V)

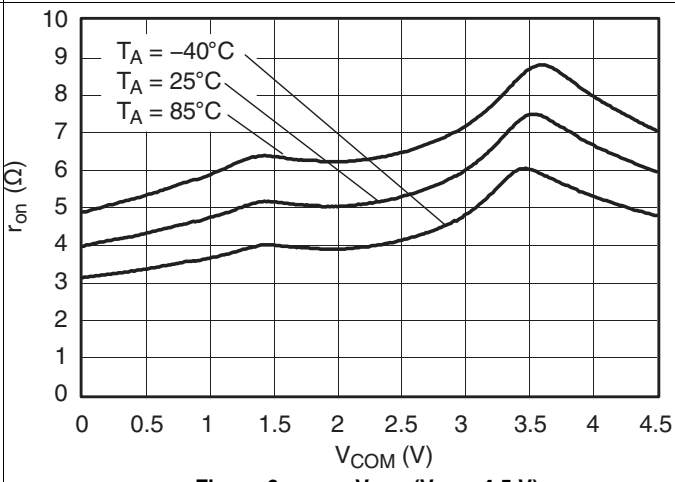


Figure 6. r_{on} vs V_{COM} (V_{CC} = 4.5 V)

Typical Performance (continued)

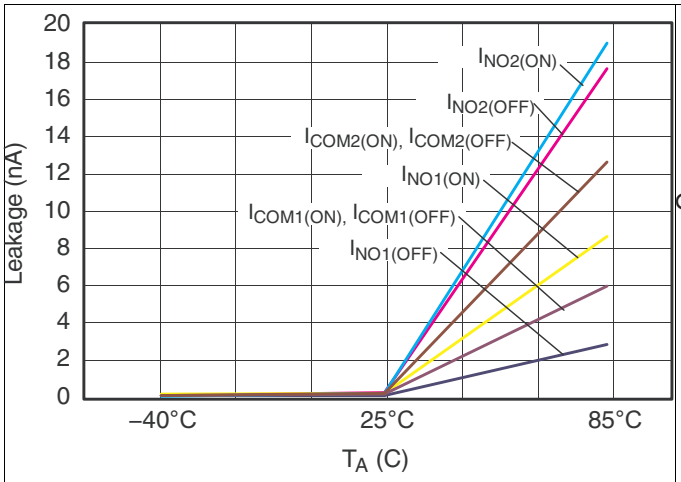


Figure 7. Leakage Current vs Temperature

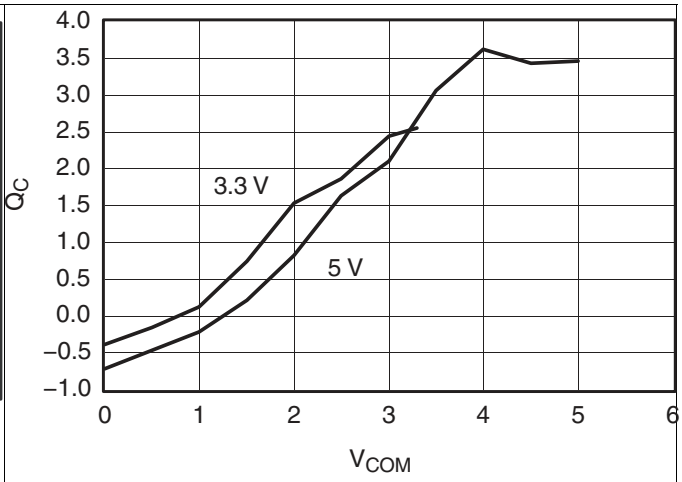


Figure 8. Charge Injection (Q_C) vs V_{COM}

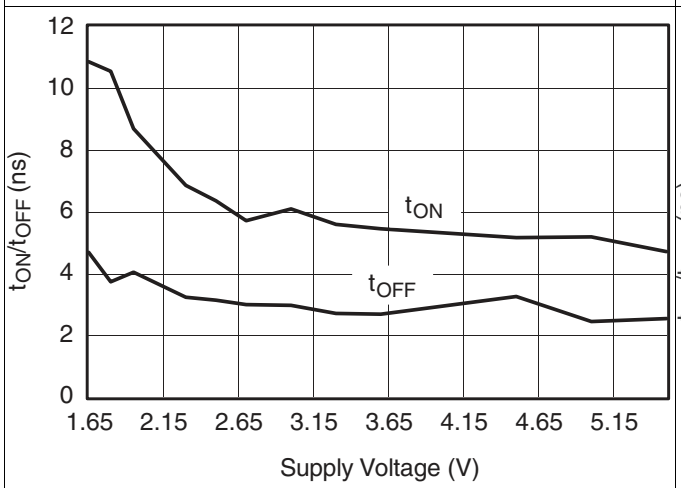


Figure 9. t_{ON} and t_{OFF} vs V_{CC}

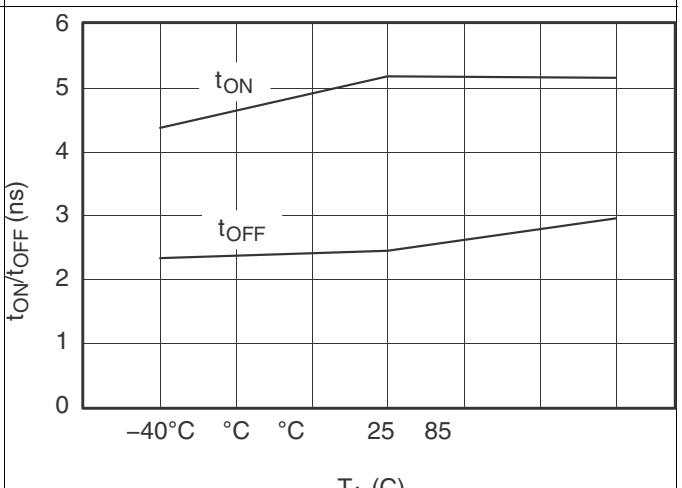


Figure 10. t_{ON} and t_{OFF} vs Temperature (V_{CC} = 5 V)

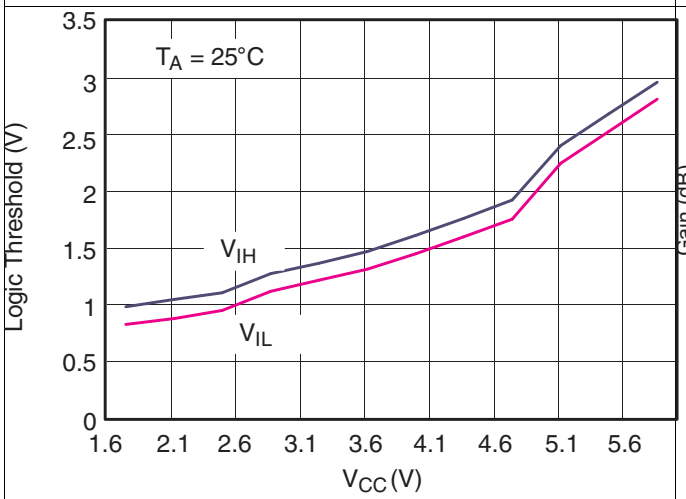


Figure 11. Logic Threshold vs V_{CC}

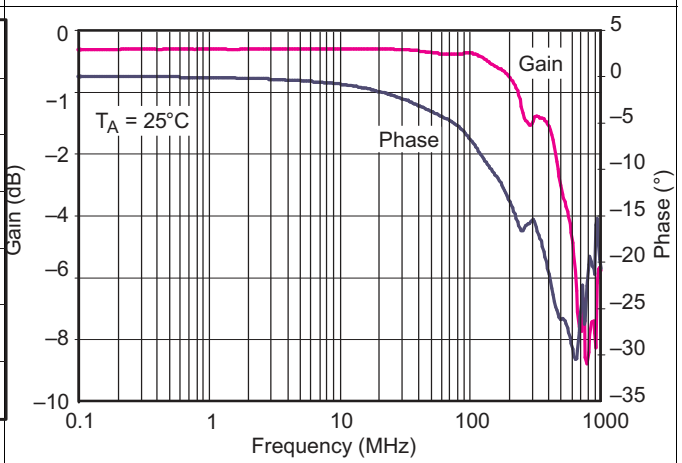


Figure 12. Bandwidth (V_{CC} = 5 V)

Typical Performance (continued)

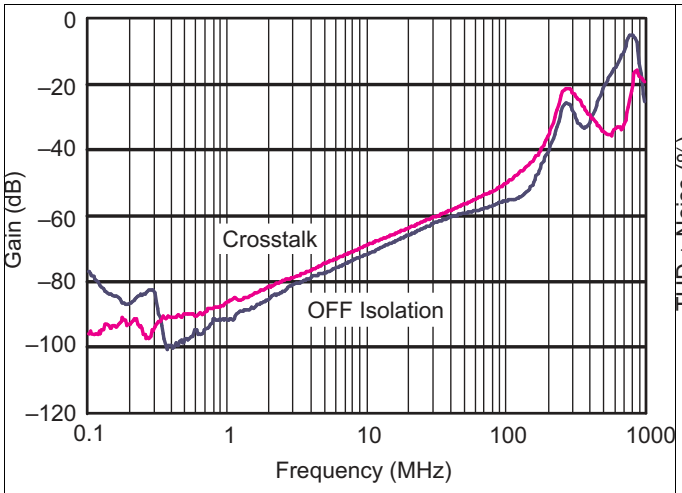


Figure 13. OFF Isolation and Crosstalk (V_{CC} = 5 V)

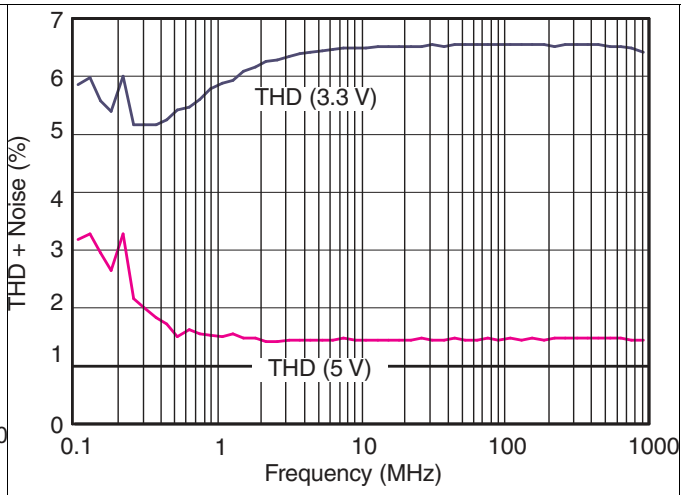


Figure 14. Total Harmonic Distortion vs Frequency

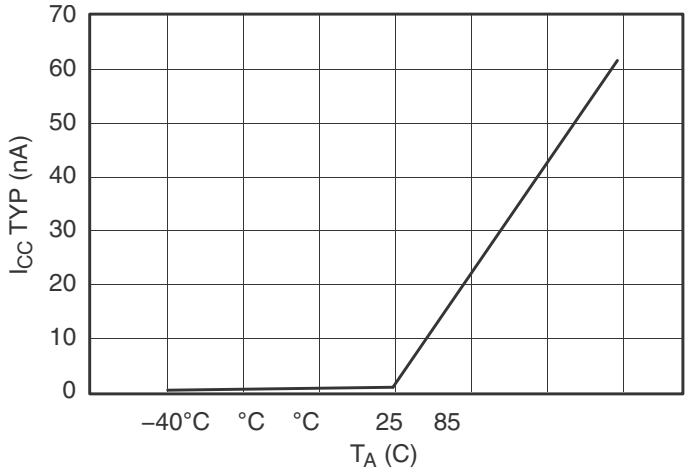


Figure 15. Power-Supply Current vs Temperature (V_{CC} = 5 V)

7 Parameter Measurement Information

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND

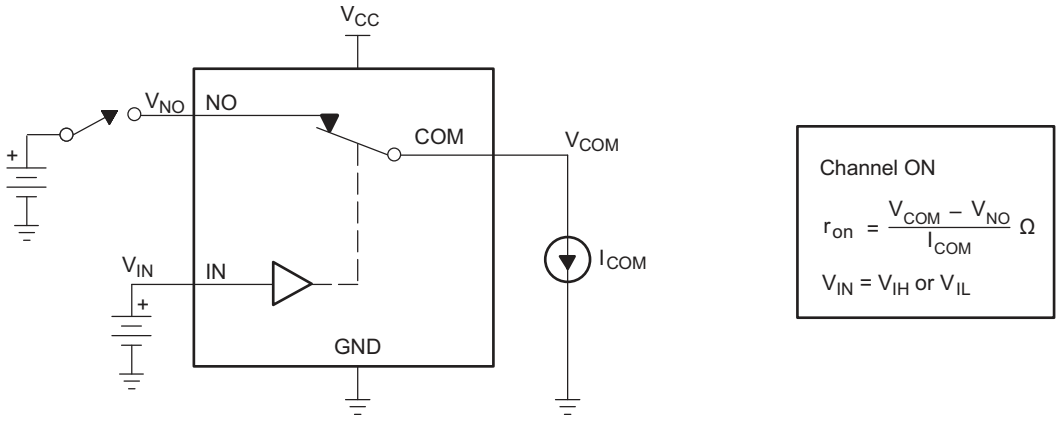


Figure 16. ON-State Resistance (r_{on})

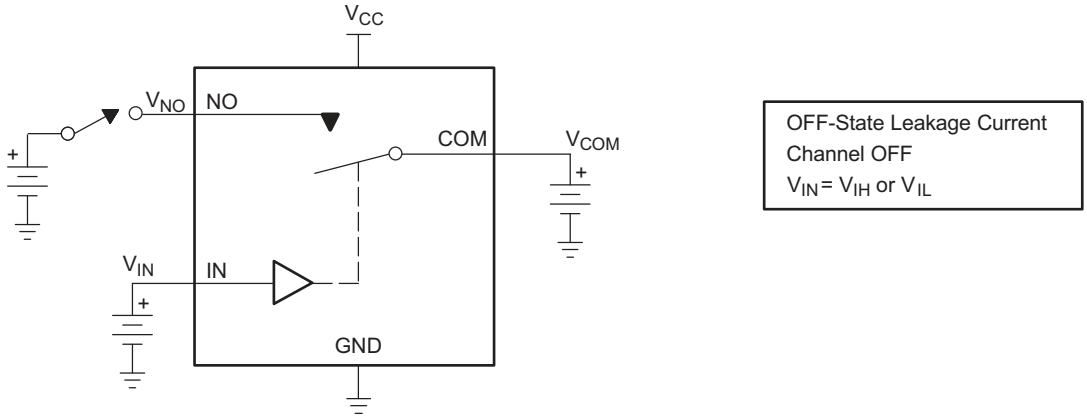


Figure 17. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

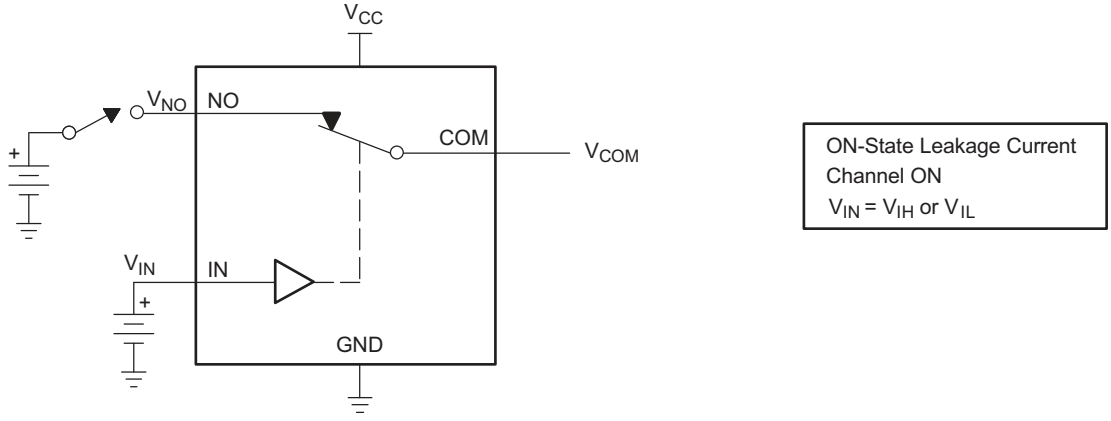


Figure 18. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

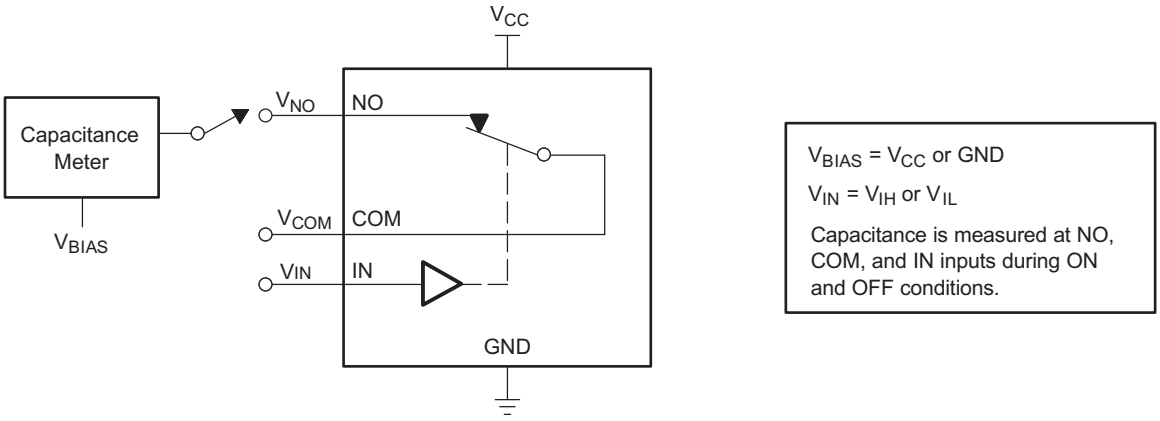
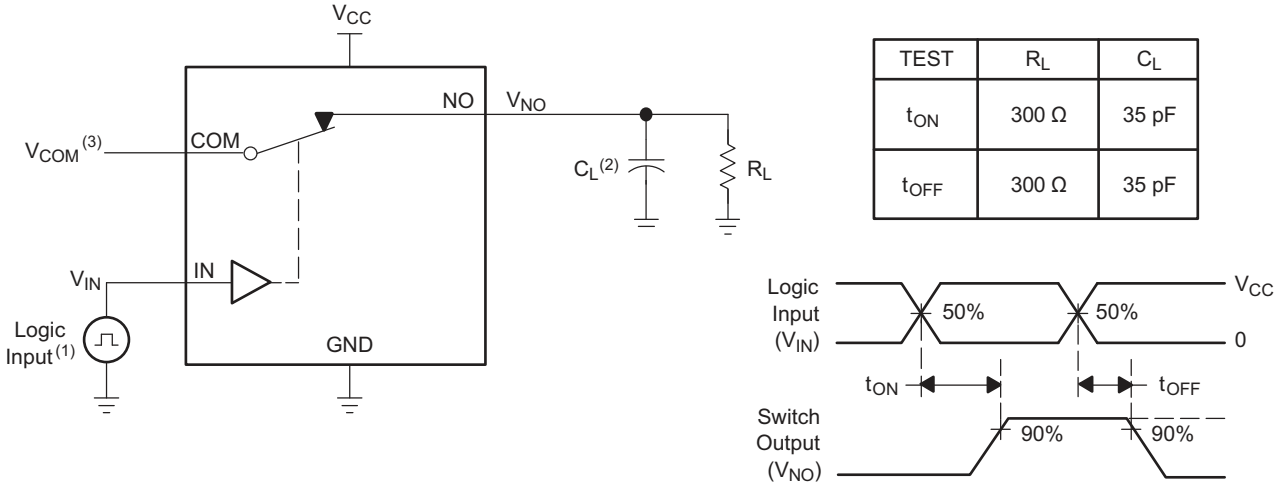


Figure 19. Capacitance (C_{IN}, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

(3) See Electrical Characteristics tables for V_{COM}.

Figure 20. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

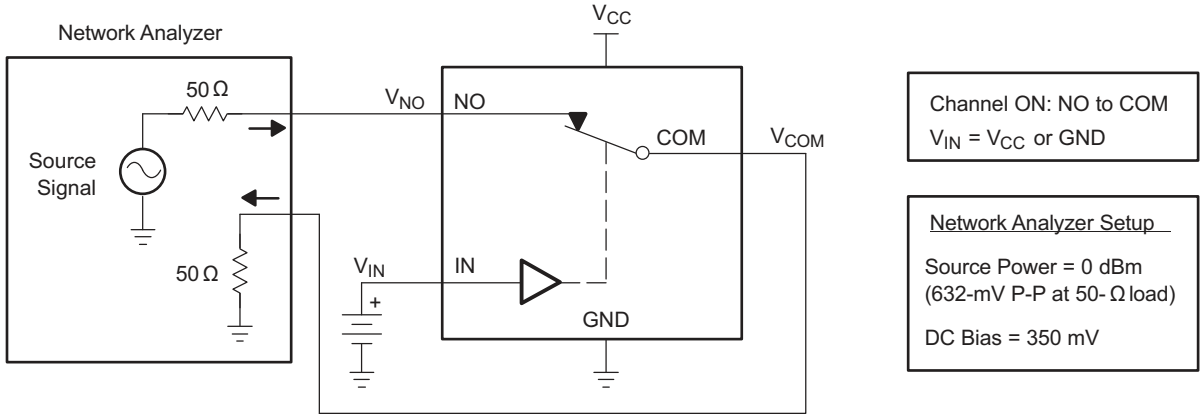


Figure 21. Bandwidth (BW)

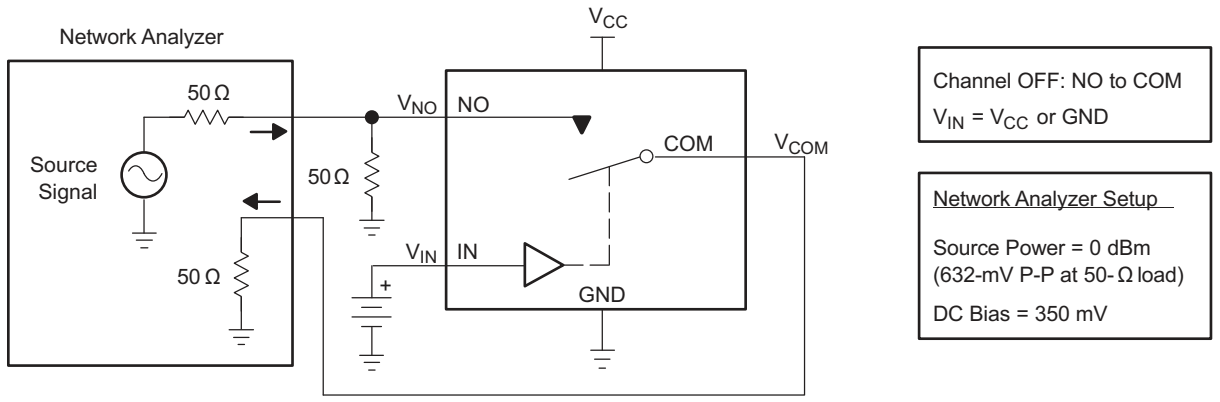


Figure 22. OFF Isolation (O_{ISO})

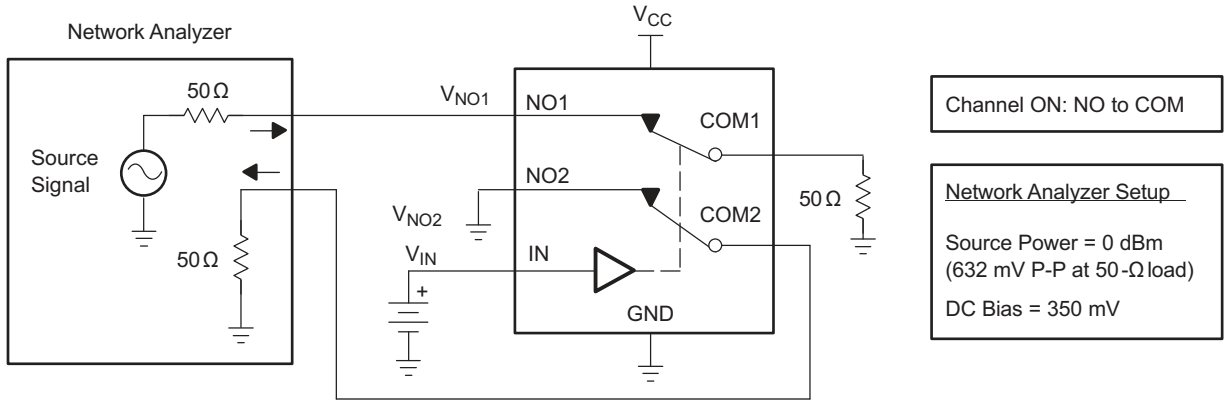
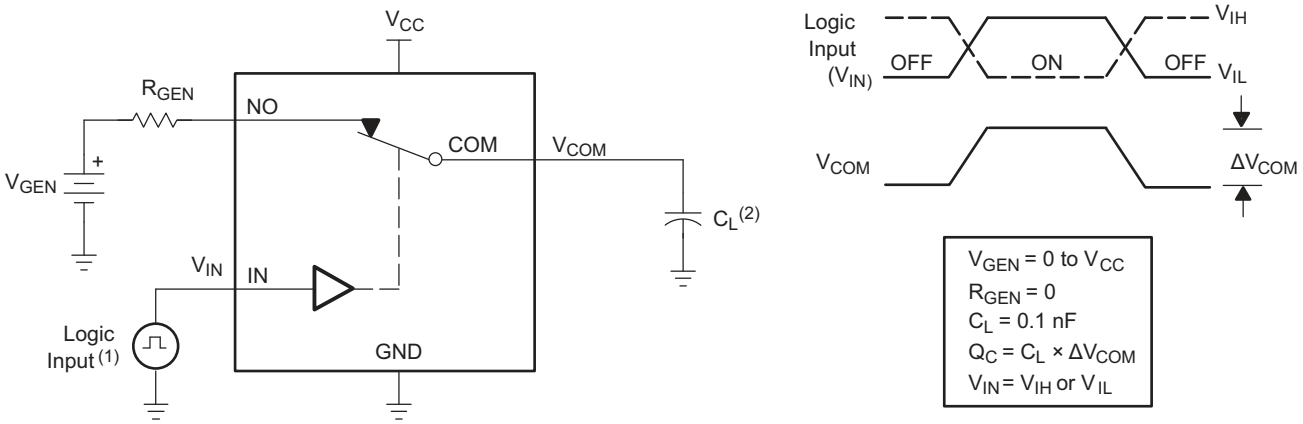


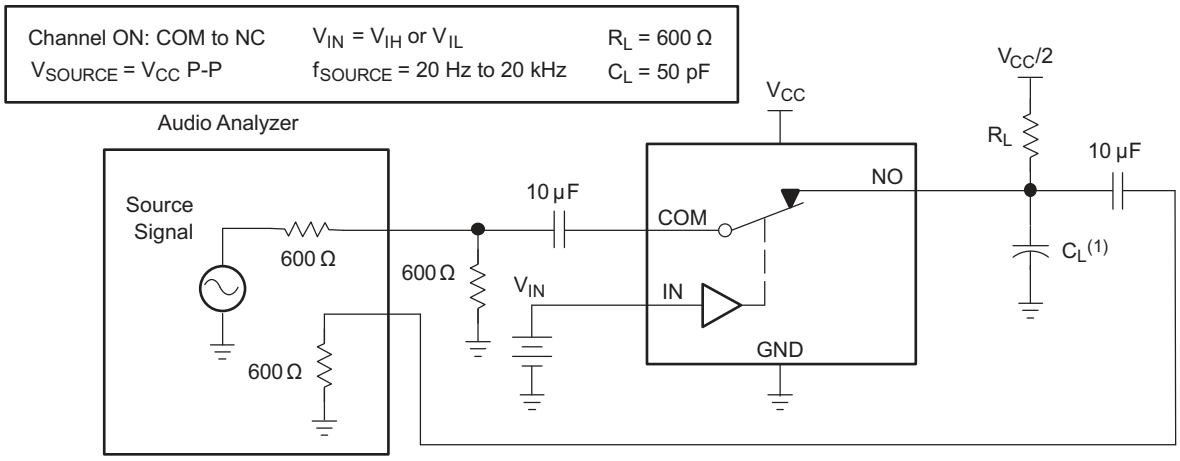
Figure 23. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 24. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

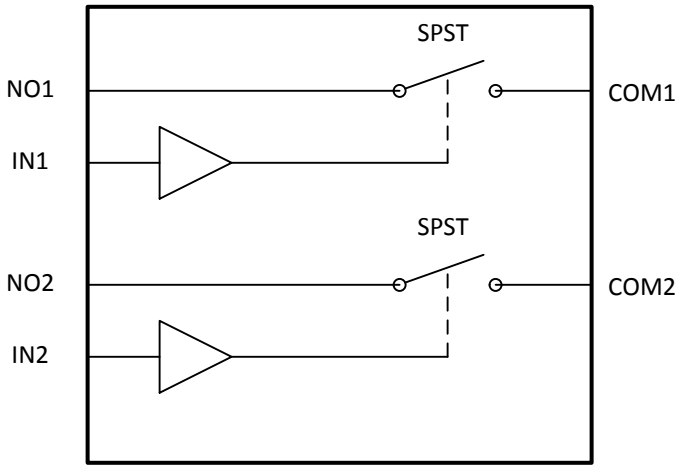
Figure 25. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A2066 device is a 2-channel single-pole single-throw (1:1 SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_{CC} can be transmitted in either direction

8.2 Functional Block Diagram



8.3 Feature Description

5-V tolerant control inputs allow 5-V logic levels to be present on the IN pin irrespective of the voltage on VCC pin.

Low ON-resistance and THD performance allows minimal signal distortion through device.

8.4 Device Functional Modes

Table 2 shows the functional modes for TS5A23166.

Table 2. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A2066 2-channel, 1:1 SPST analog switch is a basic component that could be used in any electrical system design that signal isolation.

9.2 Typical Application

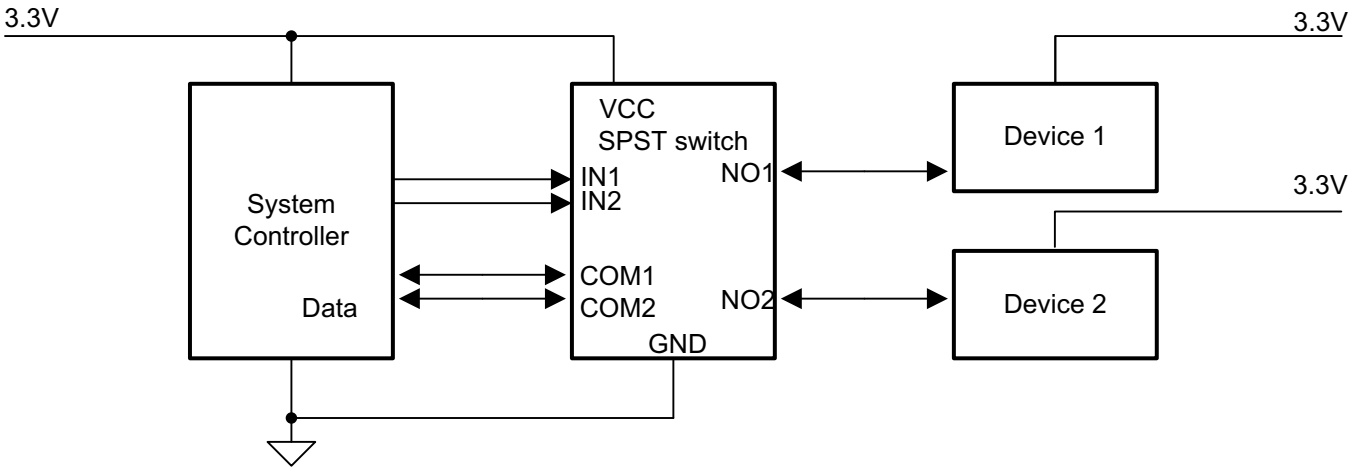


Figure 26. Typical Application Circuit

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges in the recommended operating conditions to ensure proper performance.

9.2.2 Detailed Design Procedure

The TS5A2066 can be properly operated without any external components.

Unused signal path pins COM or NO maybe left floating or connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

TI recommends that the digital control pins (INX) be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. Leaving the logic pins floating may increase I_{CC}. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004), for further details.

Typical Application (continued)

9.2.3 Application Curves

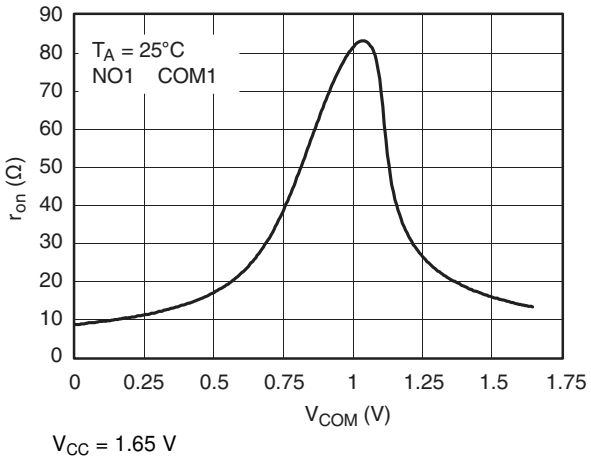


Figure 27. r_{on} vs V_{COM}

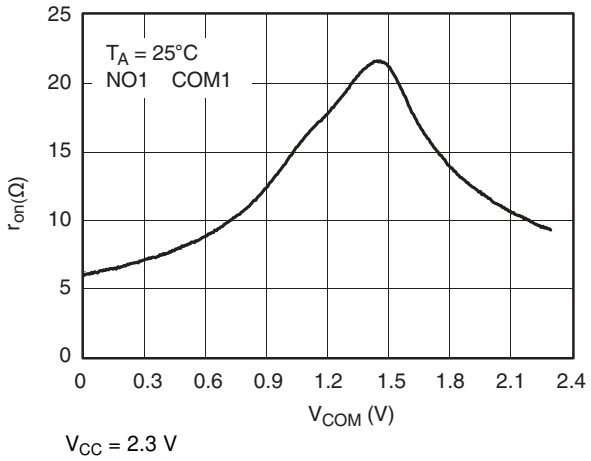


Figure 28. r_{on} vs V_{COM}

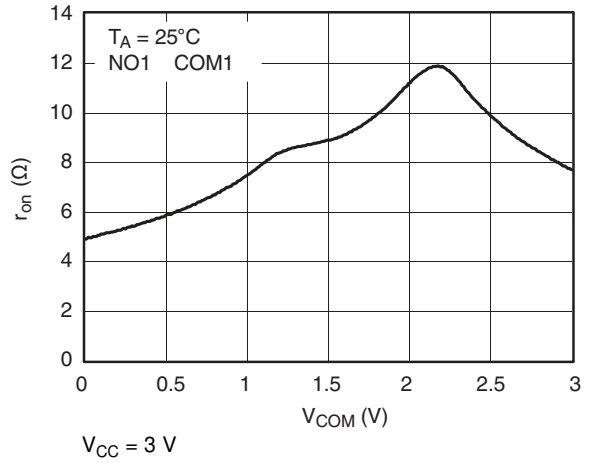


Figure 29. r_{on} vs V_{COM}

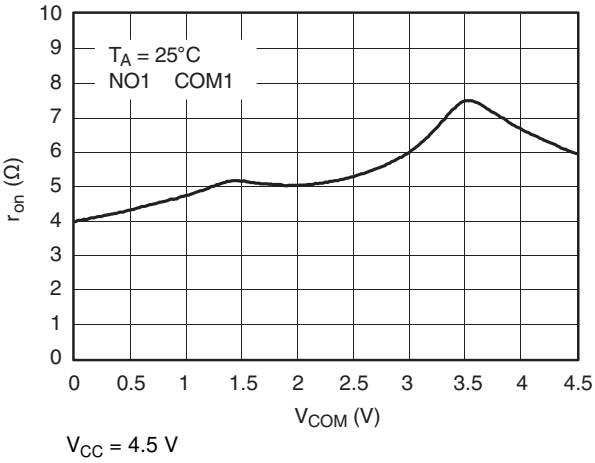


Figure 30. r_{on} vs V_{COM}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications. Copyright

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

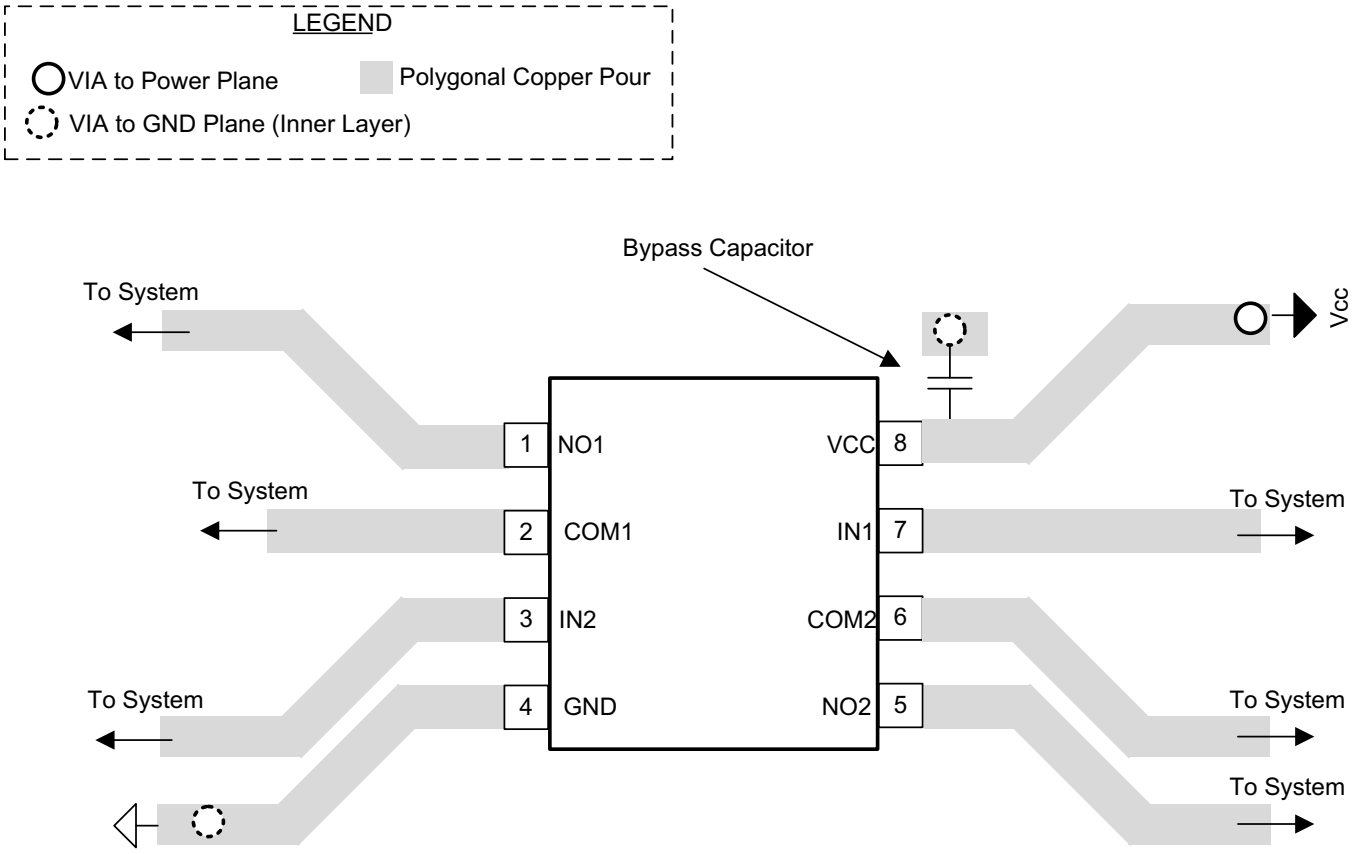


Figure 31. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A2066DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAG Z	Samples
TS5A2066DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066DCURE4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J4N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

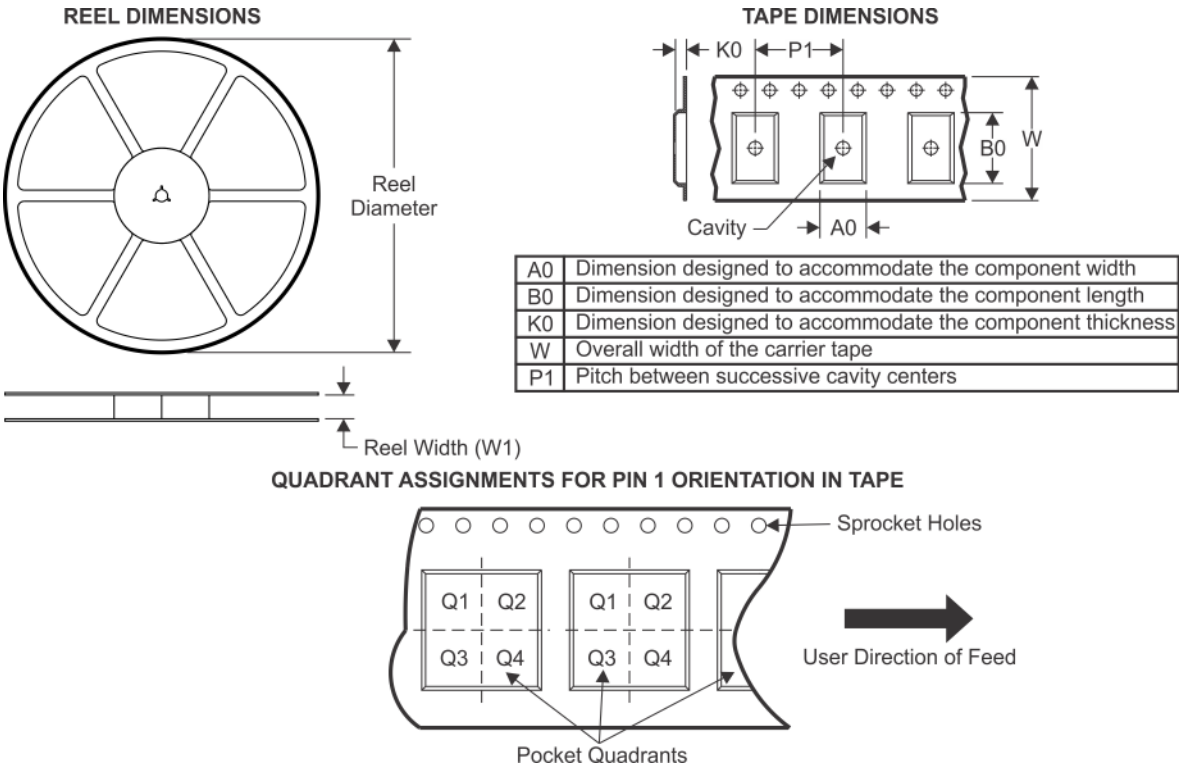
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

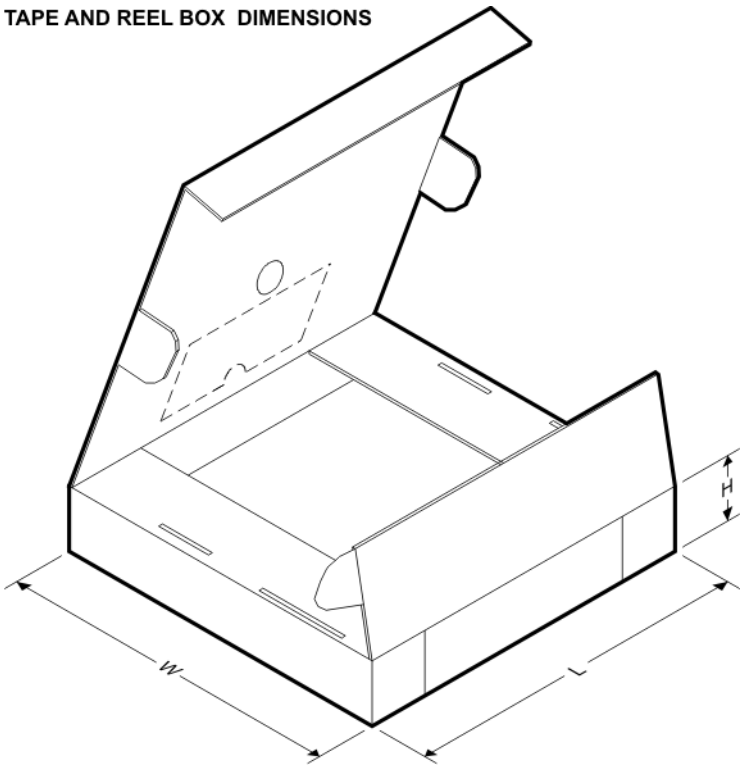


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2066DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2066DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2066DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2066YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

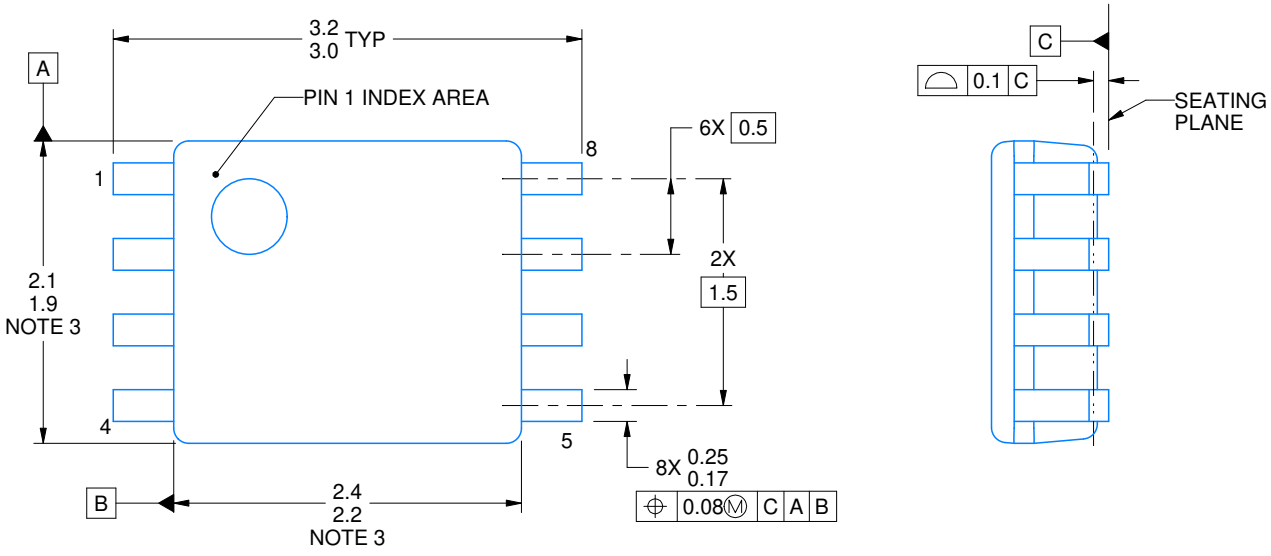
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A2066DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
TS5A2066DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A2066DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A2066YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

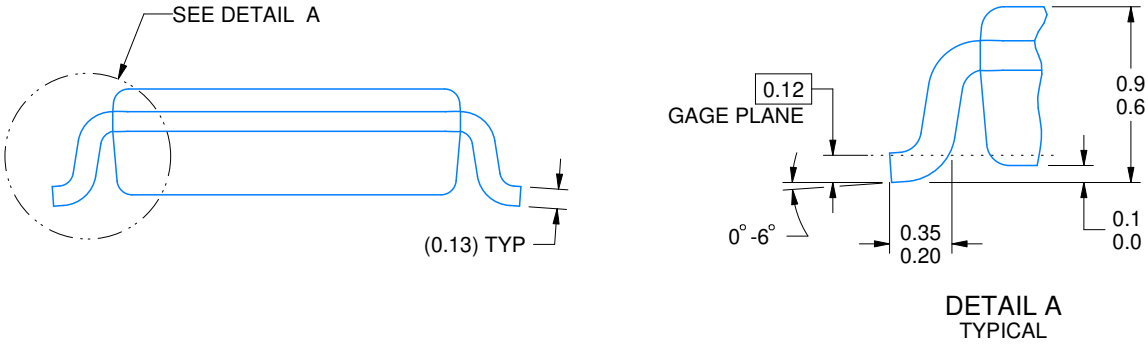
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

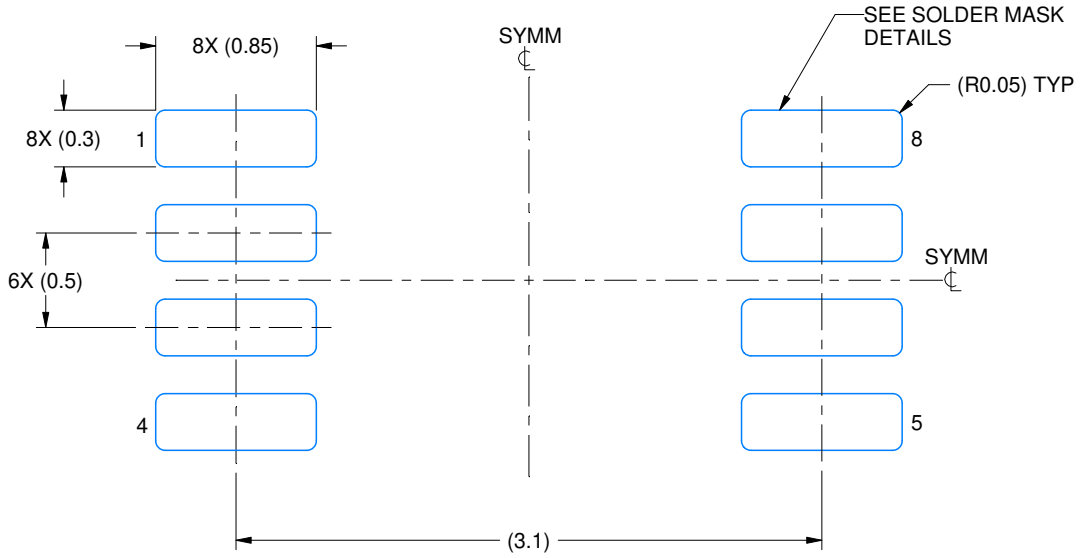




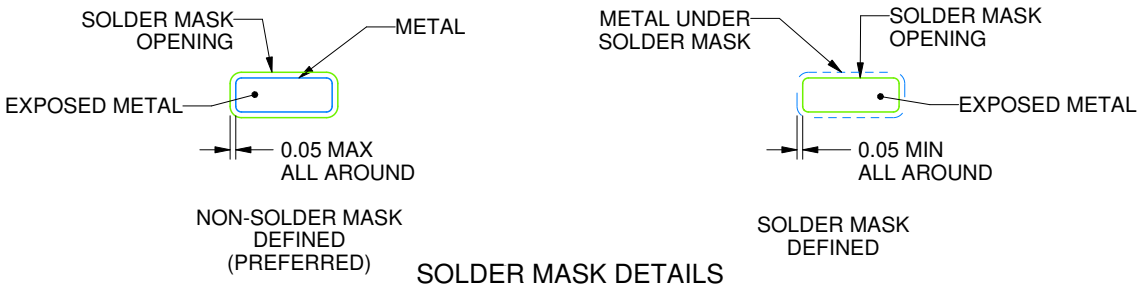
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

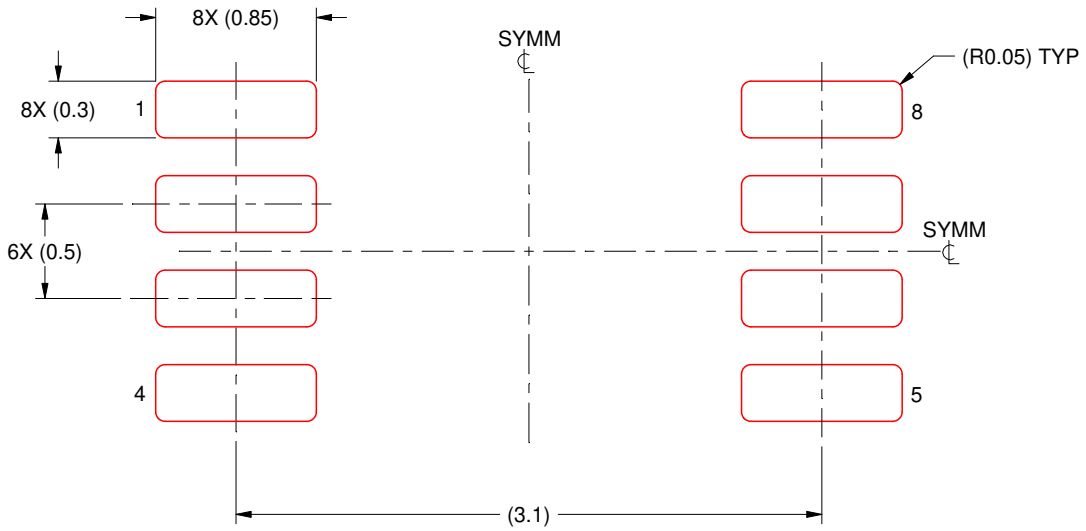


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

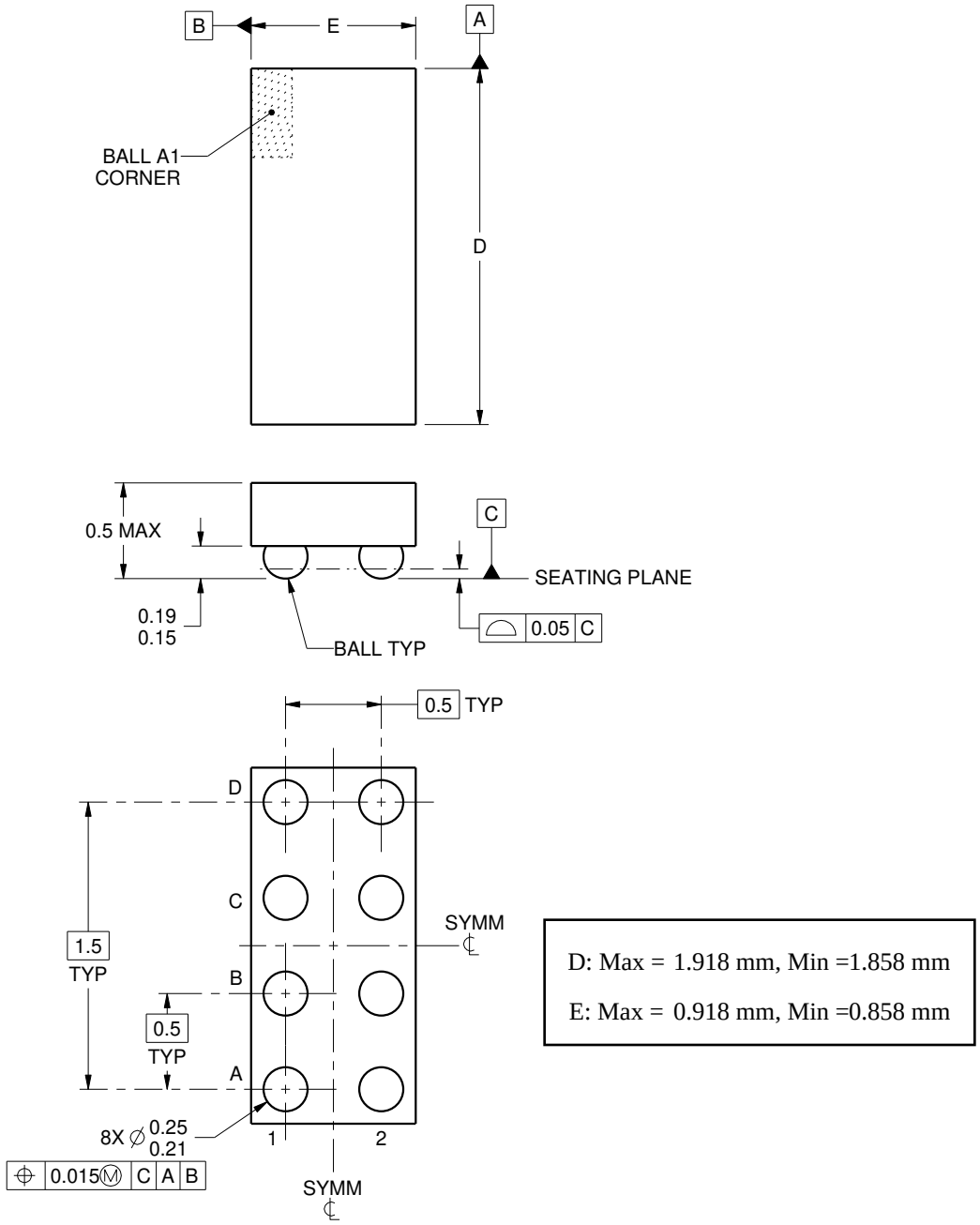
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

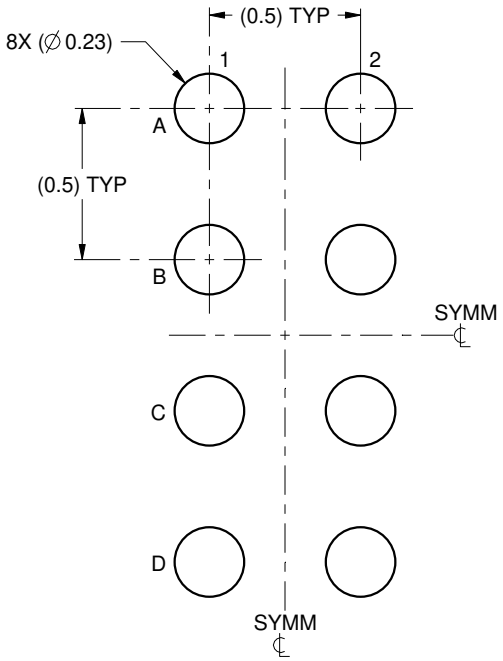
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

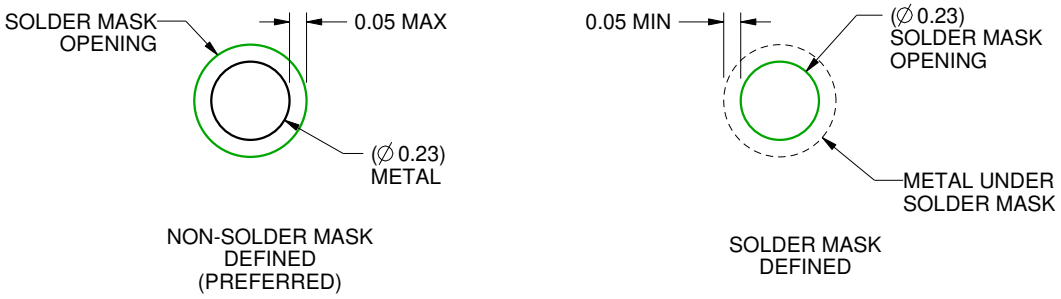


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

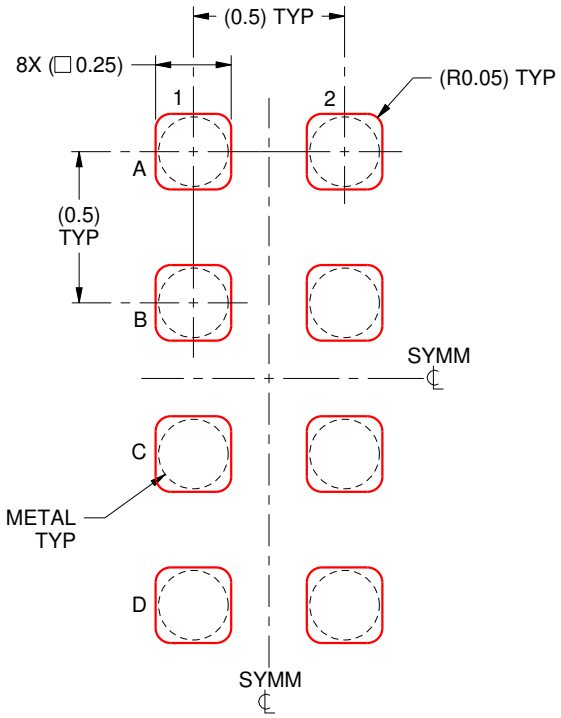


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

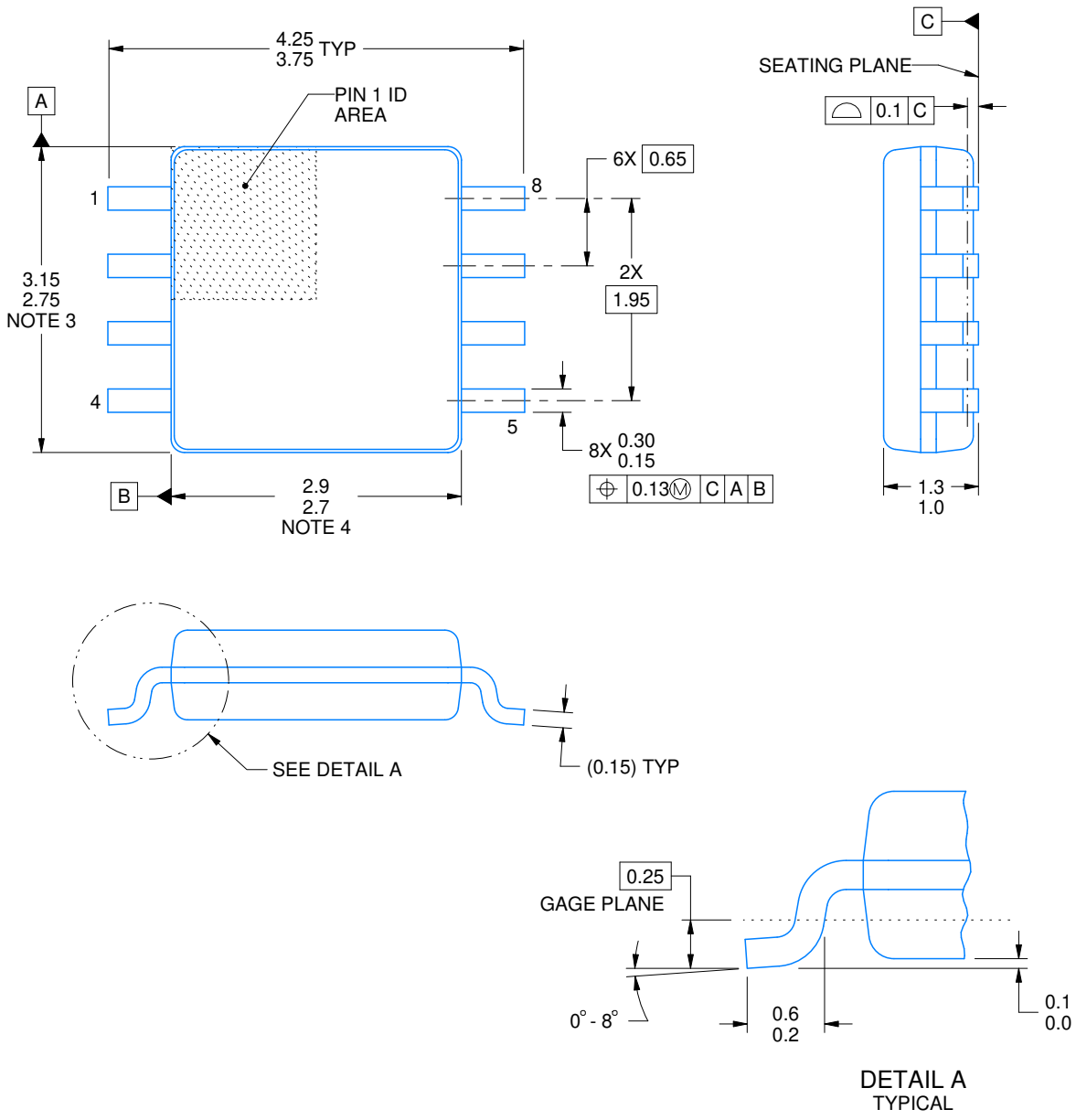
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

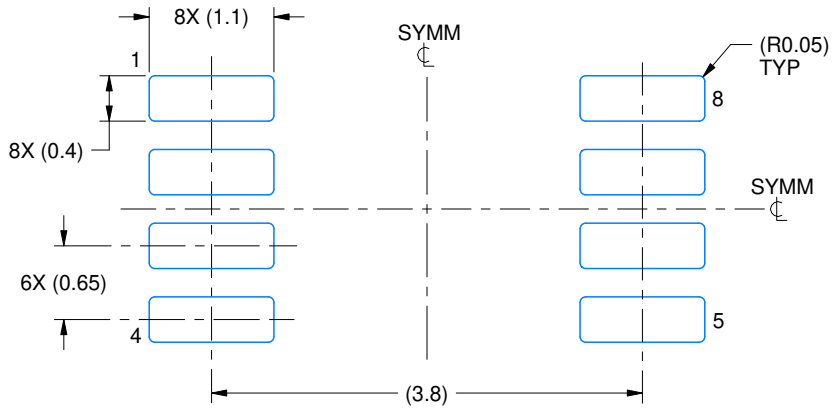
SMALL OUTLINE PACKAGE



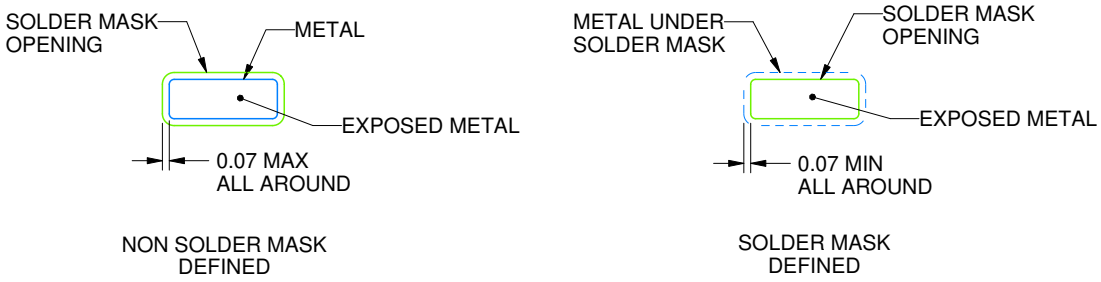
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

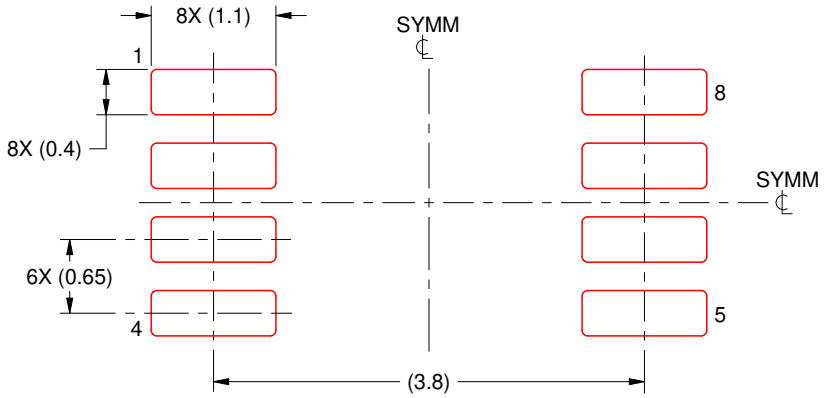


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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