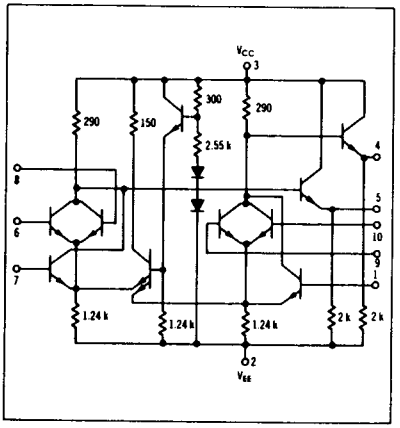
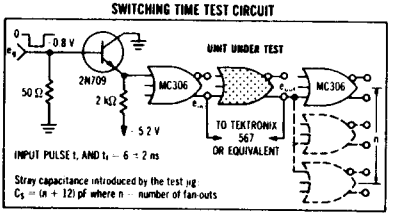
MC312A

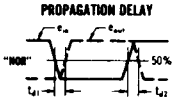
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC312.



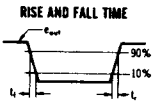
SWITCHING TIME TEST CIRCUIT



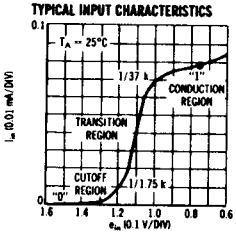
PROPAGATION DELAY



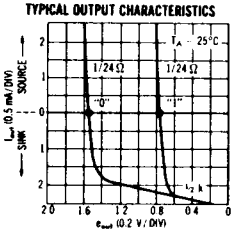
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions $V_{dc} \pm 1\%$			
−55°C	—	−0.945	1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_S (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	nAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (5)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
								V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_0 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_0 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_0 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_0 (5)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_0 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_0 (4)							
								V_0 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5①	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	1	2,6,7,8,9,10	—	4①	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_1 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_1 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,10	8①	—	3	V_1 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1①	—	3	V_1 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9①	—	3	V_1 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10①	—	3	V_1 (4)	—		—		—		
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{pd} (5)	6.5	10.5	6.5	10.5	7.5	13.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{pd} (4)	6.5	10.5	6.5	10.5	7.5	13.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{pd} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{pd} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	8.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	

Pins not listed are left open.
① Input voltage is adjusted to obtain dv "NOR" / $dV_{in} = 0$. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)