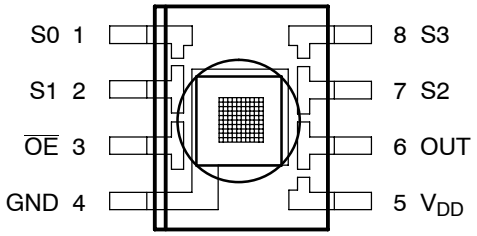
# TSL230RD, TSL230ARD, TSL230BRD
# PROGRAMMABLE LIGHT-TO-FREQUENCY CONVERTERS

TAOS054P – OCTOBER 2007

- **High-Resolution Conversion of Light Intensity to Frequency With No External Components**
- **Programmable Sensitivity and Full-Scale Output Frequency**
- **Communicates Directly With a Microcontroller**
- **High Irradiance Responsivity . . . 790 Hz/(μW/cm²) Typical at 640 nm**
- **Single-Supply Operation . . . 2.7 V to 5.5 V**
- **Power-Down Feature . . . 5 μA Typical**
- **Nonlinearity Error Typically 0.2% at 100 kHz**
- **Stable 200 ppm/°C Temperature Coefficient**
- **Low-Profile Lead (Pb) Free and RoHS Compliant Surface-Mount Package**

**PACKAGE D**
**8-LEAD SOIC**
**(TOP VIEW)**

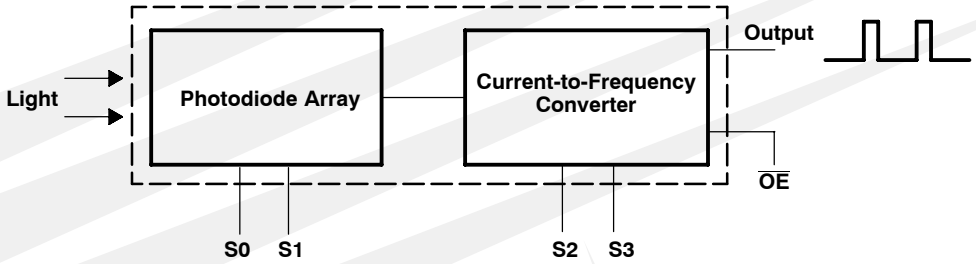



## Description

The TSL230RD, TSL230ARD, and TSL230BRD programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuit. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. Device sensitivity is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two-way communication with a microcontroller for programming and output interface. The output enable ($\overline{OE}$) places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line.

The devices are available with absolute output frequency tolerances of ±10% (TSL230BRD), ±15% (TSL230ARD), and ±20% (TSL230RD). They have been temperature compensated for the ultraviolet-to-visible light range of 320 nm to 700 nm and respond over the light range of 320 nm to 1050 nm. The devices are characterized over the temperature range of −25°C to 70°C.

## Functional Block Diagram






Texas Advanced Optoelectronic Solutions Inc.
1001 Klein Road • Suite 300 • Plano, TX 75074 • (972) 673-0759
www.taosinc.com

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| GND | 4 | | Ground |
| $\overline{OE}$ | 3 | I | Enable for $f_O$ (active low) |
| OUT | 6 | O | Scaled-frequency ($f_O$) output |
| S0, S1 | 1, 2 | I | Sensitivity-select inputs |
| S2, S3 | 7, 8 | I | $f_O$ scaling-select inputs |
| $V_{DD}$ | 5 | | Supply voltage |

## Selectable Options

| S1 | S0 | SENSITIVITY |
|---|---|---|
| L | L | Power down |
| L | H | 1× |
| H | L | 10× |
| H | H | 100× |

| S3 | S2 | $f_O$ SCALING (divide-by) |
|---|---|---|
| L | L | 1 |
| L | H | 2 |
| H | L | 10 |
| H | H | 100 |

## Available Options

| DEVICE | $T_A$ | PACKAGE – LEADS | PACKAGE DESIGNATOR | ORDERING NUMBER |
|---|---|---|---|---|
| TSL230RD | –25°C to 70°C | SOIC–8 | D | TSL230RD |
| TSL230ARD | –25°C to 70°C | SOIC–8 | D | TSL230ARD |
| TSL230BRD | –25°C to 70°C | SOIC–8 | D | TSL230BRD |

## Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . . . 6 V
Input voltage range, all inputs, $V_I$ . . . . . –0.3 V to $V_{DD}$ + 0.3 V
Operating free-air temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range . . . . . –40°C to 85°C
Solder conditions in accordance with JEDEC J–STD–020A, maximum temperature (see Note 2) . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The device may be hand soldered provided that heat is applied only to the solder pad and no contact is made between the tip of the solder iron and the device lead. The maximum time heat should be applied to the device is 5 seconds.

## Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 2.7 | 5 | 5.5 | V |
| High-level input voltage, $V_{IH}$ | $V_{DD}$ = 4.5 V to 5.5 V | 2 | | $V_{DD}$ | V |
| Low-level input voltage, $V_{IL}$ | $V_{DD}$ = 4.5 V to 5.5 V | 0 | | 0.8 | V |
| Operating free-air temperature range, $T_A$ | | –25 | | 70 | °C |

## Electrical Characteristics at $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA | 4 | 4.5 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | V |
| $I_{IH}$ | High-level input current | | | | 5 | μA |
| $I_{IL}$ | Low-level input current | | | | 5 | μA |
| $I_{DD}$ | Supply current | Power-on mode | | 2 | 3 | mA |
| | | Power-down mode | | 5 | 12 | μA |
| F.S. | Full-scale frequency (See Note 3) | S0=S1=H, S2=S3=L | 1.1 | | | MHz |
| | Temperature coefficient of output frequency | λ ≤ 700 nm (See Note 4) | | ±200 | | ppm/°C |
| $k_{SVS}$ | Supply voltage sensitivity | $V_{DD}$ = 5 V ±10% | | ±0.5 | | %/V |

NOTES: 3. Full-scale frequency is the maximum operating frequency of the device without saturation.
4. The temperature coefficient of output frequency is measured with constant irradiance as the temperature is varied between –25°C and 70°C. The constant irradiance is sufficiently high that the output frequency is much greater than the dark frequency over the entire temperature range.

## Operating Characteristics at $V_{DD}$ = 5 V, $T_A$ = 25°C, $E_e$ = 126 μW/cm², $\lambda_p$ = 640 nm (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TSL230RD | | | TSL230ARD | | | TSL230BRD | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_O$ | Output frequency | S0 = S1 = H, S2 = S3 = L | 80 | 100 | 120 | 85 | 100 | 115 | 90 | 100 | 110 | kHz |
| | | S1 = H, S0 = S2 = S3 = L | 8 | 10 | 12 | 8.5 | 10 | 11.5 | 9 | 10 | 11 | |
| | | S0 = H, S1 = S2 = S3 = L | 0.8 | 1 | 1.2 | 0.85 | 1 | 1.15 | 0.9 | 1 | 1 | |
| | | S0 = S1 = S2 = H, S3 = L | 40 | 50 | 60 | 42.5 | 50 | 57.5 | 45 | 50 | 55 | |
| | | S0 = S1 = S3 = H, S2 = L | 8 | 10 | 12 | 8.5 | 10 | 11.5 | 9 | 10 | 11 | |
| | | S0 = S1 = S2 = S3 = H | 0.8 | 1 | 1.2 | 0.85 | 1 | 1.15 | 0.9 | 1 | 1.1 | |
| $f_D$ | Dark frequency | $E_e$ = 0, S0 = S1 = H, S2 = S3 = L | | 0.4 | 10 | | 0.4 | 10 | | 0.4 | 10 | Hz |
| $R_e$ | Responsivity | S0 = S1 = H, S2 = S3 = L | | 0.79 | | | 0.79 | | | 0.79 | | kHz/(μW/cm²) |
| $t_w$ | Output pulse duration | S2 = S3 = L | 125 | | 600 | 125 | | 600 | 125 | | 600 | ns |
| | | S2 or S3 = H | | $1/2f_O$ | | | $1/2f_O$ | | | $1/2f_O$ | | s |
| | Nonlinearity (See Notes 5 and 6) | $f_O$ = 0 MHz to 10 kHz | | ±0.1% | | | ±0.1% | | | ±0.1% | | %F.S. |
| | | $f_O$ = 0 MHz to 100 kHz | | ±0.2% | | | ±0.2% | | | ±0.2% | | |
| | | $f_O$ = 0 MHz to 1 MHz | | ±0.5% | | | ±0.5% | | | ±0.5% | | |
| | Recovery from power down | | | | 100 | | | 100 | | | 100 | μs |
| | Step response to full-scale step input | | 1 pulse of new frequency plus 1 μs | | | | | | | | | |
| | Response time to programming change | | 2 periods of new principal frequency plus 1 μs (Note 7) | | | | | | | | | |
| | Response time to output enable ($\overline{OE}$) | | | 50 | 150 | | 50 | 150 | | 50 | 150 | ns |

NOTES: 5. Nonlinearity is defined as the deviation of $f_O$ from a straight line between zero and full scale, expressed as a percent of full scale.
6. Nonlinearity test condition: S0 = S1 = H, S2 = S3 = L.
7. Principal frequency is the internal oscillator frequency, equivalent to divide-by-1 output selection.

## TYPICAL CHARACTERISTICS

**OUTPUT FREQUENCY vs IRRADIANCE**

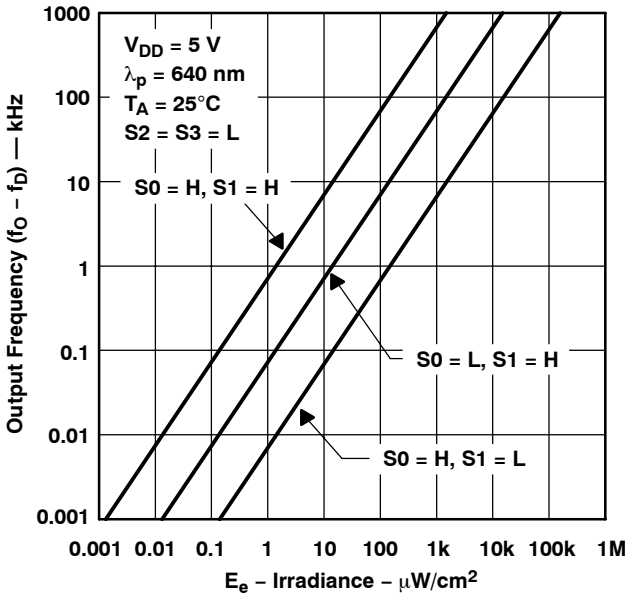



**Figure 1**

**PHOTODIODE SPECTRAL RESPONSIVITY**

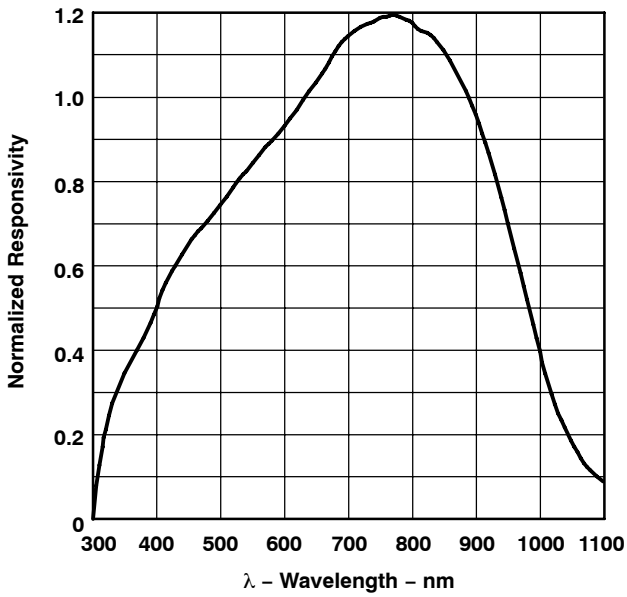



**Figure 2**

**DARK FREQUENCY vs TEMPERATURE**

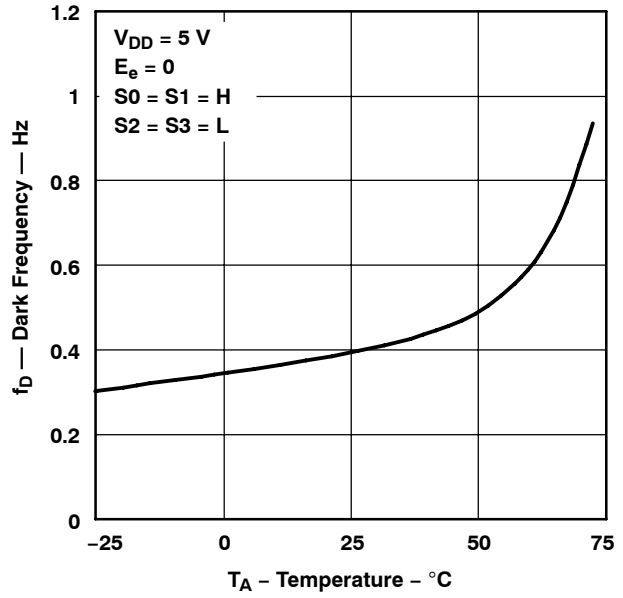



**Figure 3**

**TEMPERATURE COEFFICIENT OF OUTPUT FREQUENCY vs WAVELENGTH OF INCIDENT LIGHT**

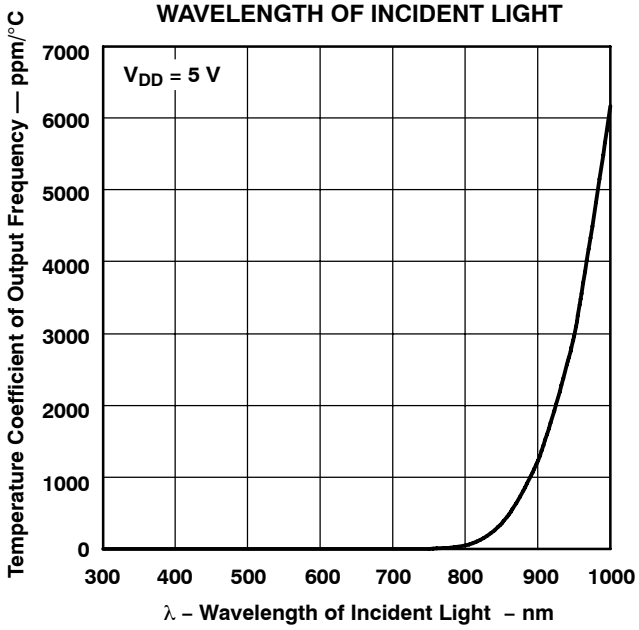



**Figure 4**

## TYPICAL CHARACTERISTICS

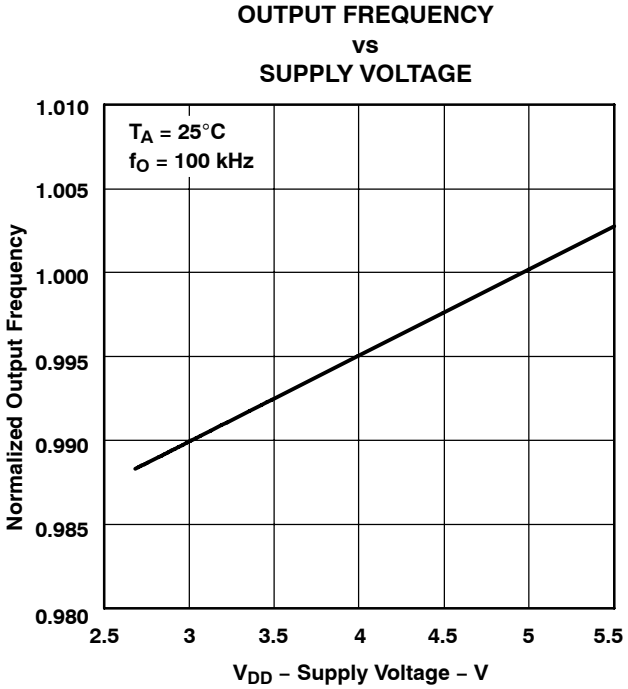



**Figure 5**

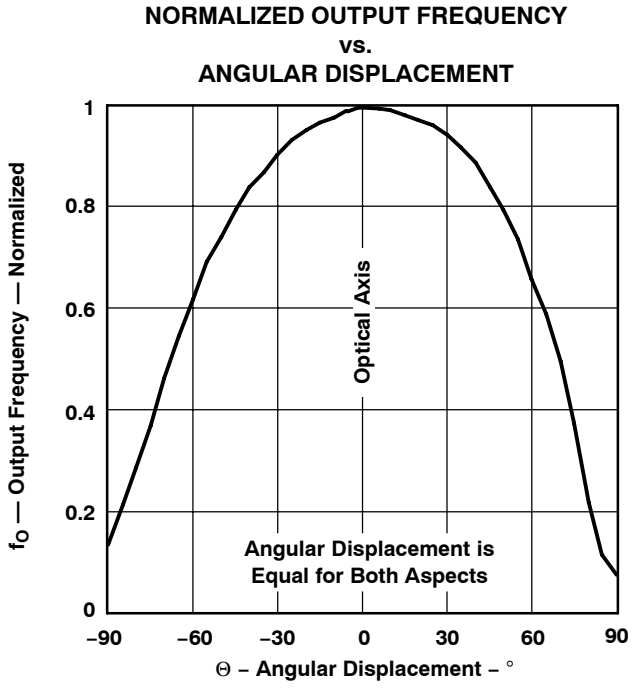



**Figure 6**

## APPLICATION INFORMATION

### Power-Supply Considerations

Power-supply lines must be decoupled by a 0.01-μF to 0.1-μF capacitor with short leads placed close to the TSL230RD device package. A low-noise power supply is required to minimize jitter on output pulses.

### Device Operational Details

The frequency at the output pin (OUT) is given by:

$$f_O = f_D + (R_e)(E_e)$$

where:

| | |
|---|---|
| $f_O$ | is the output frequency |
| $f_D$ | is the output frequency for dark condition ($E_e$ = 0) |
| $R_e$ | is the device responsivity for a given wavelength of light given in kHz/(μW/cm$^2$) |
| $E_e$ | is the incident irradiance in μW/cm$^2$ |

$f_D$ is an output frequency resulting from leakage currents. As shown in the equation above, this frequency represents a light-independent term in the total output frequency $f_O$. At very low light levels, this dark frequency can be a significant portion of $f_O$. The dark frequency is temperature dependent. For optimum performance of any given device over the full output range, the value of $f_D$ should be measured (in the absence of light) and later subtracted from subsequent light measurement (see Figure 1).

### Input Interface

A low-impedance electrical connection between the device $\overline{OE}$ pin and the device GND pin is required for improved noise immunity.

### Output Interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

### Sensitivity Adjustment

Sensitivity is controlled by two logic inputs, S0 and S1. Sensitivity is adjusted using an electronic iris technique — effectively an aperture control — to change the response of the device to a given amount of light. The sensitivity can be set to one of three levels: 1×, 10×, or 100×, providing two decades of adjustment. This allows the responsivity of the device to be optimized to a given light level while preserving the full-scale output-frequency range. Changing of sensitivity also changes the effective photodiode area by the same factor.

## APPLICATION INFORMATION

### Output-Frequency Scaling

Output-frequency scaling is controlled by two logic inputs, S2 and S3. Scaling is accomplished on chip by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs available are divide-by 2, 10, 100, and 1 (no division). Divided outputs are 50 percent-duty-cycle square waves while the direct output (divide-by 1) is a fixed-pulse-width pulse train. Because division of the output frequency is accomplished by counting pulses of the principal (divide-by 1) frequency, the final-output period represents an average of n (where n is 2, 10, or 100) periods of the principal frequency. The output-scaling-counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, or OE lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period in the divided output modes. In contrast with the sensitivity adjust, use of the divided outputs lowers both the full-scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The divide-by-1 or straight-through output can be used with a frequency counter, pulse accumulator, or high-speed timer (period measurement). The divided-down outputs may be used where only a slower frequency counter is available, such as a low-cost microcontroller, or where period measurement techniques are used. The divide-by-10 and divide-by-100 outputs provide lower frequency ranges for high resolution-period measurement.

### Measuring the Frequency

The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

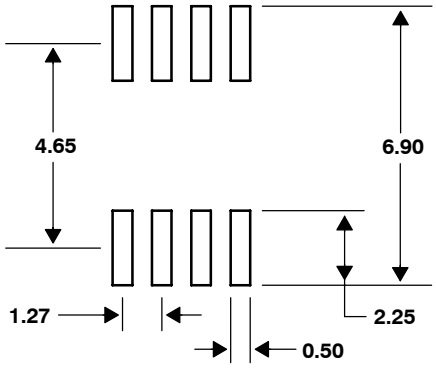
Using the divide-by-2 output, data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random or high-frequency variations (jitter) resulting from noise in the light signal or from noise in the power supply. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

## APPLICATION INFORMATION

### PCB Pad Layout

Suggested PCB pad layout guidelines for the D package are shown in Figure 7.



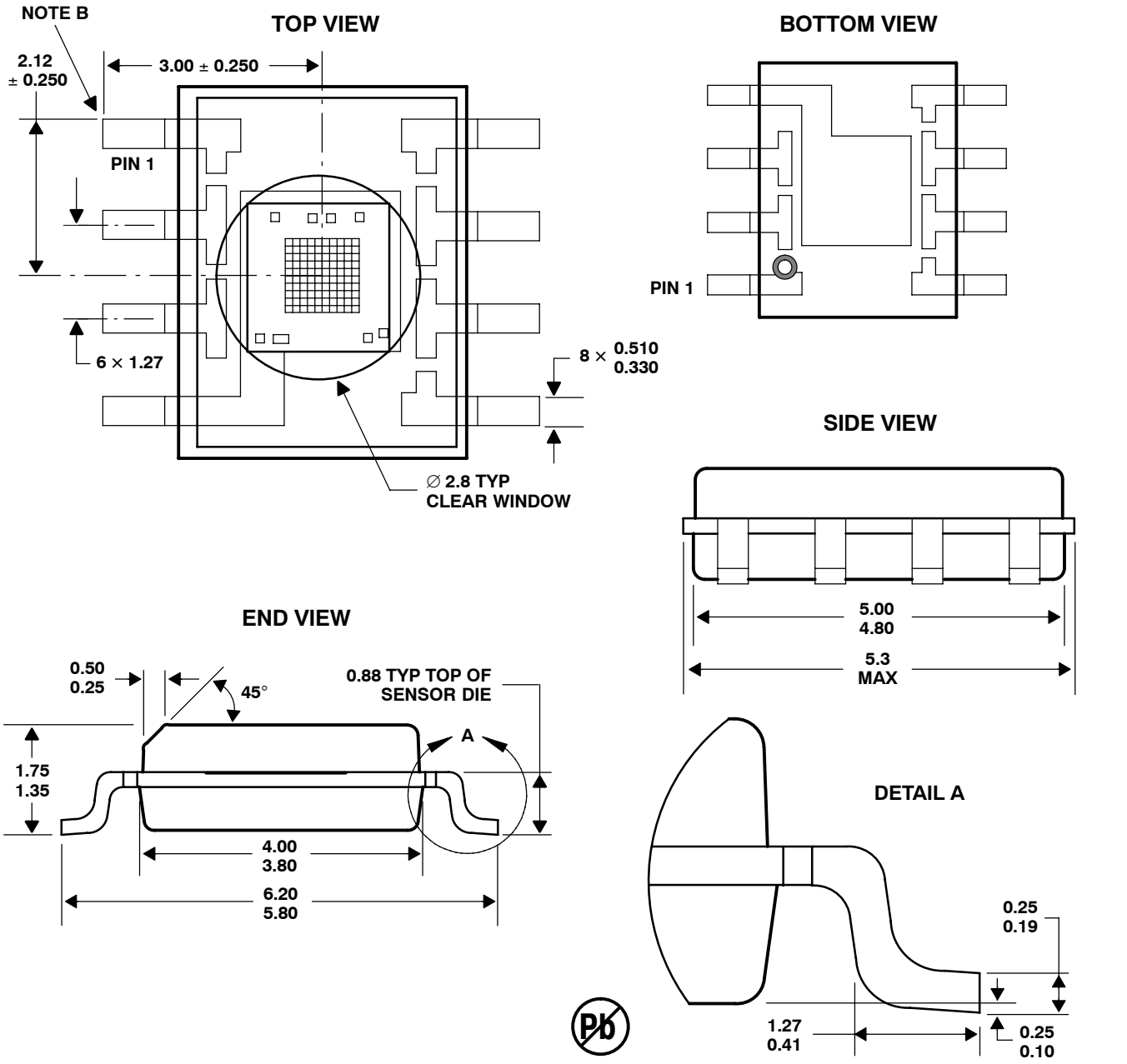

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

**Figure 7. Suggested D Package PCB Layout**

## MECHANICAL DATA

This SOIC package consists of an integrated circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound. The TSL230RD has a 10 × 10 array of photodiodes with a total size of 0.96 mm by 0.96 mm. The photodiodes are 0.084 mm × 0.084 mm in size and are positioned on 0.096 mm centers.

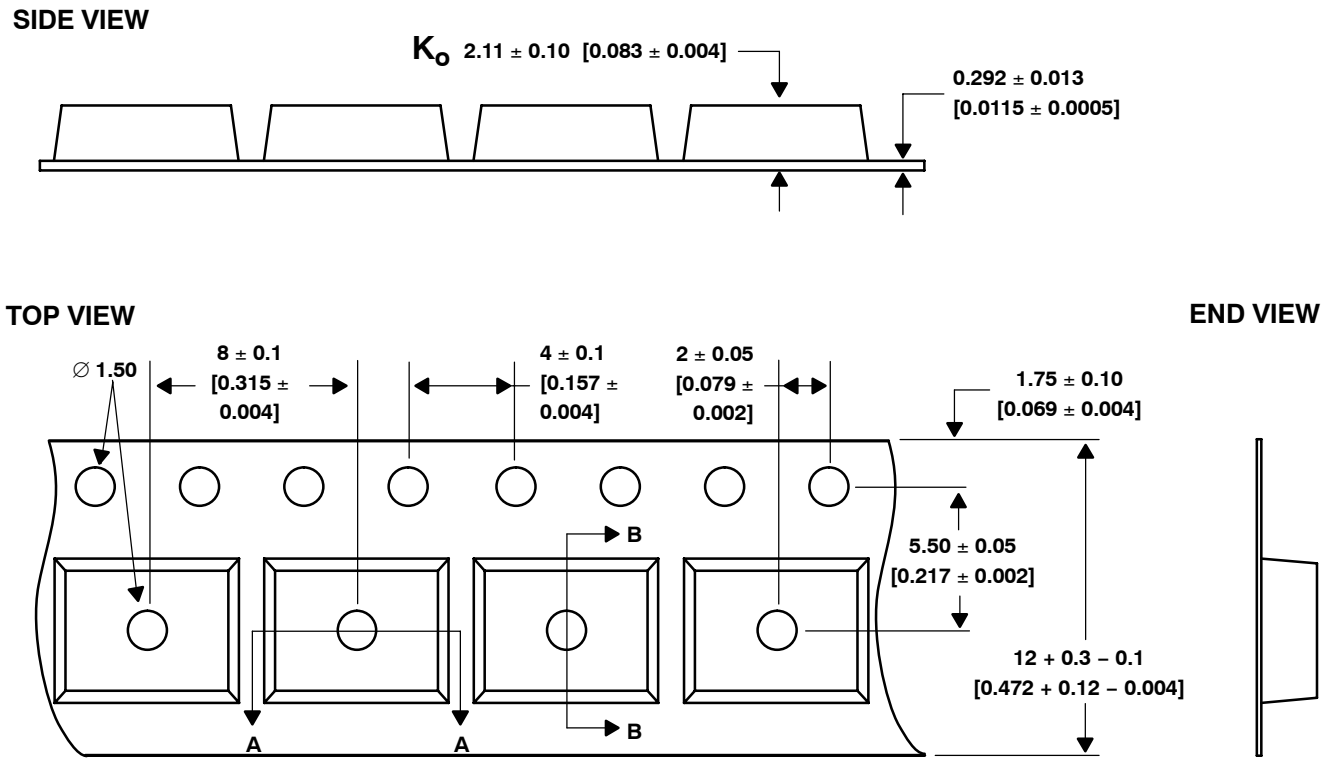
**PACKAGE D** **PLASTIC SMALL-OUTLINE**

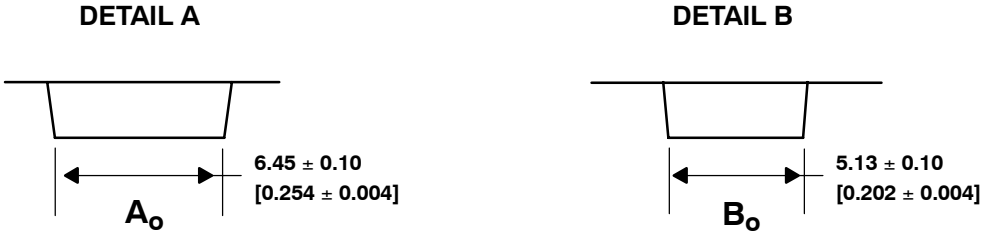



NOTES: A. All linear dimensions are in millimeters.
B. The center of the 0.96-mm by 0.96-mm photo-active area is referenced to the upper left corner tip of the lead frame (Pin 1).
C. Package is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
D. This drawing is subject to change without notice.

**Figure 8. Package D — Plastic Small Outline IC Packaging Configuration**

## MECHANICAL DATA




NOTES: A. All linear dimensions are in millimeters [inches].
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing $A_o$, $B_o$, and $K_o$ are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 1000 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. This drawing is subject to change without notice.

**Figure 9. Package D Carrier Tape**

## MANUFACTURING INFORMATION

The Plastic Small Outline IC package (D) has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The component should be limited to a maximum of three passes through this solder reflow profile.

**Table 1. TSL230RD Solder Reflow Profile**

| PARAMETER | REFERENCE | TSL230RD |
|---|---|---|
| Average temperature gradient in preheating | | 2.5°C/sec |
| Soak time | $t_{soak}$ | 2 to 3 minutes |
| Time above 217°C | $t_1$ | Max 60 sec |
| Time above 230°C | $t_2$ | Max 50 sec |
| Time above $T_{peak}$ –10°C | $t_3$ | Max 10 sec |
| Peak temperature in reflow | $T_{peak}$ | 260° C (–0°C/+5°C) |
| Temperature gradient in cooling | | Max –5°C/sec |

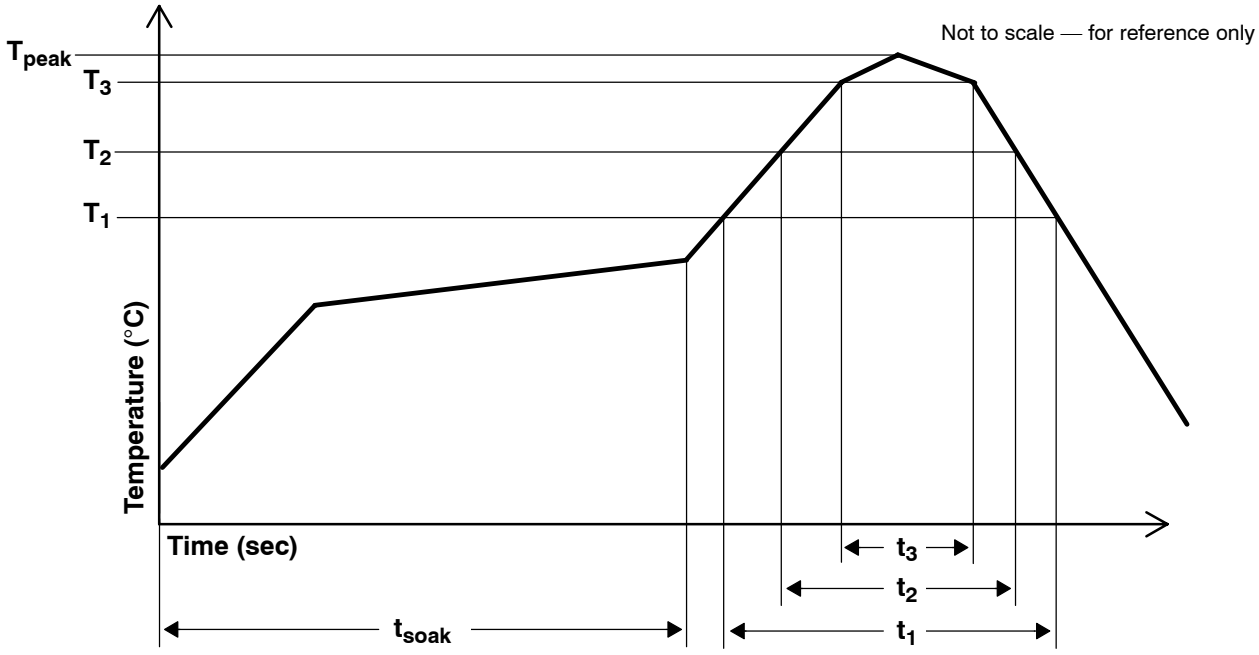



**Figure 10. TSL230RD Solder Reflow Profile Graph**

## Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package molding compound. To prevent these adverse conditions, all devices shipped in carrier tape have been pre-baked and shipped in a sealed moisture-barrier bag. No further action is necessary if these devices are processed through solder reflow within 24 hours of the seal being broken on the moisture-barrier bag.

However, for all devices shipped in tubes or if the seal on the moisture barrier bag has been broken for 24 hours or longer, it is recommended that the following procedures be used to ensure the package molding compound contains the smallest amount of absorbed moisture possible.

***For devices shipped in tubes:***

1. Remove devices from tubes
2. Bake devices for 4 hours, at 90°C
3. After cooling, load devices back into tubes
4. Perform solder reflow within 24 hours after bake

Bake only a quantity of devices that can be processed through solder reflow in 24 hours. Devices can be re-baked for 4 hours, at 90°C for a cumulative total of 12 hours (3 bakes for 4 hours at 90°C).

***For devices shipped in carrier tape:***

1. Bake devices for 4 hours, at 90°C in the tape
2. Perform solder reflow within 24 hours after bake

Bake only a quantity of devices that can be processed through solder reflow in 24 hours. Devices can be re–baked for 4 hours in tape, at 90°C for a cumulative total of 12 hours (3 bakes for 4 hours at 90°C).

**PRODUCTION DATA** — information in this document is current at publication date. Products conform to specifications in accordance with the terms of Texas Advanced Optoelectronic Solutions, Inc. standard warranty. Production processing does not necessarily include testing of all parameters.

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