TPS3700EVM-114 High voltage (18V) window voltage detector evaluation module for SOT-23 package

This user's guide describes the operational use of the TPS3700EVM-114 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TPS3700 high voltage window voltage detector for over and undervoltage monitoring. Included in this user's guide are setup instructions, a schematic diagram, PCB layout drawings, and a bill of materials for the evaluation module.

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1 Introduction

The Texas Instruments (TI) TPS3700EVM-114 Evaluation Module (EVM) helps design engineers evaluate the operation and performance of the TPS3700 IC for possible use in their own circuit application. This particular EVM configuration contains an over- and under-voltage detector circuit with a wide supply range, independent open-drain outputs, very low quiescent current, and high accuracy in a TSOT23-6 DDC package. This document describes the configuration and set up of the EVM board.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the EVM.

2.1 Input/Output Connector and Jumper Descriptions

2.1.1 J1 — V_{DD}

This connector is the power supply connection.

This also may be the signal being monitored by the TPS3700.

2.1.2 J2 — GND

Return connector for the input power supply. This connector is also connected to J4, J6, and J8 in the EVM.

2.1.3 J3 — SENSE

This connector is an additional voltage signal that is monitored if V_{DD} is not monitored.

2.1.4 J4 — GND

Return connector for the SENSE voltage signal. This connector is also connected to J2, J6, and J8 in the EVM.

2.1.5 J5 — OUTA

This connector is the under-voltage open-drain output of the TPS3700 that pulls up to VPU through a 100-kΩ resistor in the EVM. Connect a voltage meter or oscilloscope probe from J5 to GND (J6).

2.1.6 J6 — GND

Return connector for the OUTA voltage signal. This connector is also connected to J2, J4, and J8 in the EVM.

2.1.7 J7 — OUTB

This connector is the over-voltage open-drain output of the TPS3700 that pulls up to VPU through a 10-kΩ resistor in the EVM. Connect a voltage meter or oscilloscope probe from J7 to GND (J6).

2.1.8 J8 — GND

Return connector for the OUTB voltage signal. This connector is also connected to J2, J4, and J6 in the EVM.

2.1.9 J9 — VEXT

This connector is an external voltage. OUTA and OUTB can be pulled up to this voltage.

2.1.10 J10 — MONITOR SENSE and MONITOR V_{DD} SELECT

The EVM is designed to monitor either the supply voltage V_{DD} or an additional voltage signal SENSE.

A shorting jumper allows the user to choose between monitoring V_{DD} or SENSE. Table 1 shows the connections for choosing between the two.

Table 1. Connector J10 Selections

Short Pins	Monitor
1 and 2	SENSE
2 and 3	V_{DD}

2.1.11 J11 — VPU

The EVM is designed for OUTA and OUTB to pull up to V_{DD} or an external voltage source VEXT. Table 2 shows the connections for choosing between the two.

Table 2. Connector J11 Selections

Short Pins	Pullup Voltage VPU
1 and 2	V_{DD}
2 and 3	VEXT

2.2 Equipment Setup

- Set the first power-supply voltage between 1.8 V-18 V. Turn the power supply off. Connect the positive voltage lead from the power supply to J1 (V_{DD}). Connect the ground lead from the power supply to J2 (GND).
- Set the second power-supply voltage between 1.8 V-18 V. Turn the power supply off. Connect the positive voltage lead from the power supply to J3 (SENSE). Connect the ground lead from the power supply to J4 (GND).
- Set the third power-supply voltage between 1.8 V-18 V. Turn the power supply off. Connect the positive voltage lead from the power supply to J9 (VEXT). Connect the ground lead from the power supply to J4 (GND).
- Use the shorting jumper on J10 and select Monitor Sense.
- Use the shorting jumper on J11 and select VEXT.
- Turn on all power supplies.

3 Operation

This section provides information about the operation of the EVM.

3.1 General Operation

The EVM is an over- and under-voltage supervisor. The EVM monitors a selected voltage signal (SENSE or V_{DD}). OUTA triggers LOW when INA+ is below the 394.5-mV threshold and triggers HIGH (VPU) when INA+ goes above 400 mV. OUTB triggers LOW when INB- is above the 400-mV threshold and triggers HIGH (VPU) when INB- falls beneath 394.5 mV.

The EVM is designed to sense a 12-V rail and trigger when the rail falls below 10% or rises above 10% of 12 V. Specifically, OUTA will trigger LOW during a –10% drop (10.8 V) while OUTB will trigger LOW during a +10% rise (13.2 V). In between this window, the outputs are pulled up to VPU. Figure 1 and Figure 2 shows the OUTA and OUTB response for monitoring V_{DD} and the output pulled up (VPU) to an external 5V source (VEXT=5V).

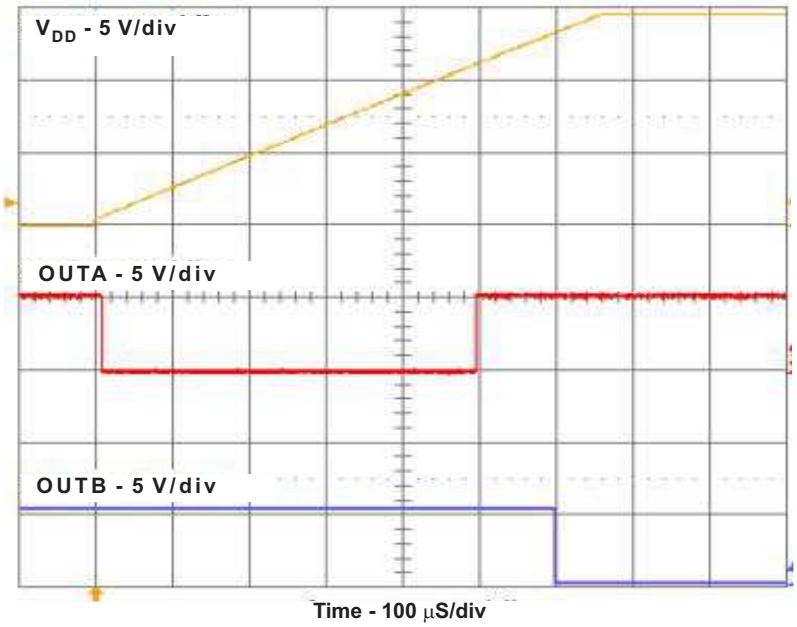

Figure 1. OUTA and OUTB Response for V_{DD} Voltage Rising

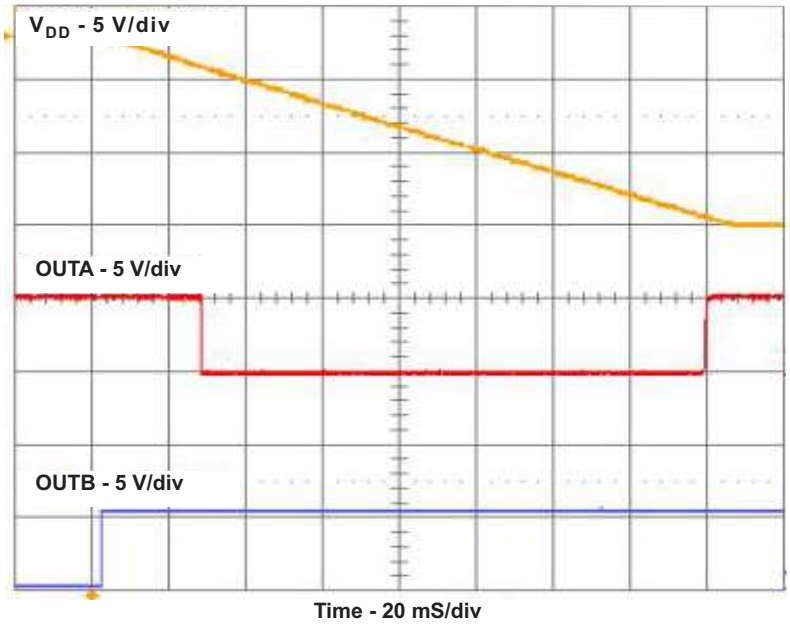

Figure 2. OUTA and OUTB Response for V_{DD} Voltage Falling

Resistors R1, R2, and R3 can be replaced with different values to change the window at which OUTA and OUTB triggers HIGH and LOW. Design information can be found in the applications section of the TPS3700 datasheet (SBVS187A).

4 Board Layout

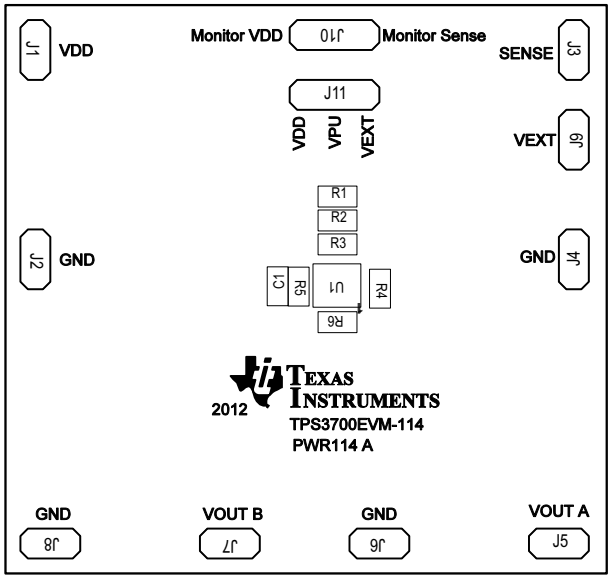

Figure 3. Assembly Layer

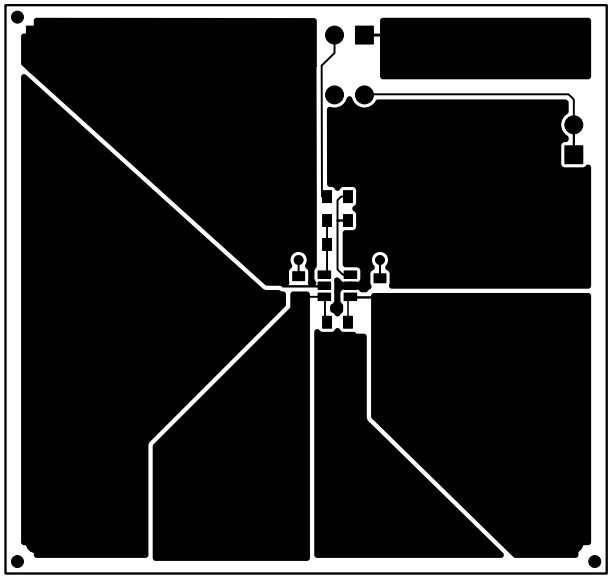

Figure 4. Top Layer Routing

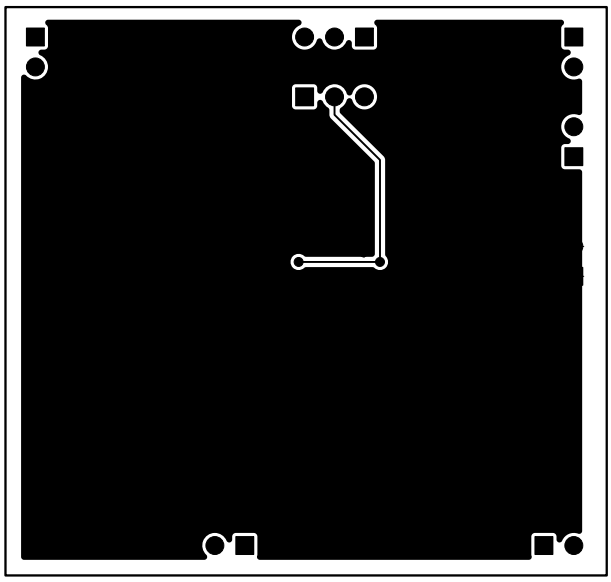

Figure 5. Bottom Layer Routing

5 Schematic

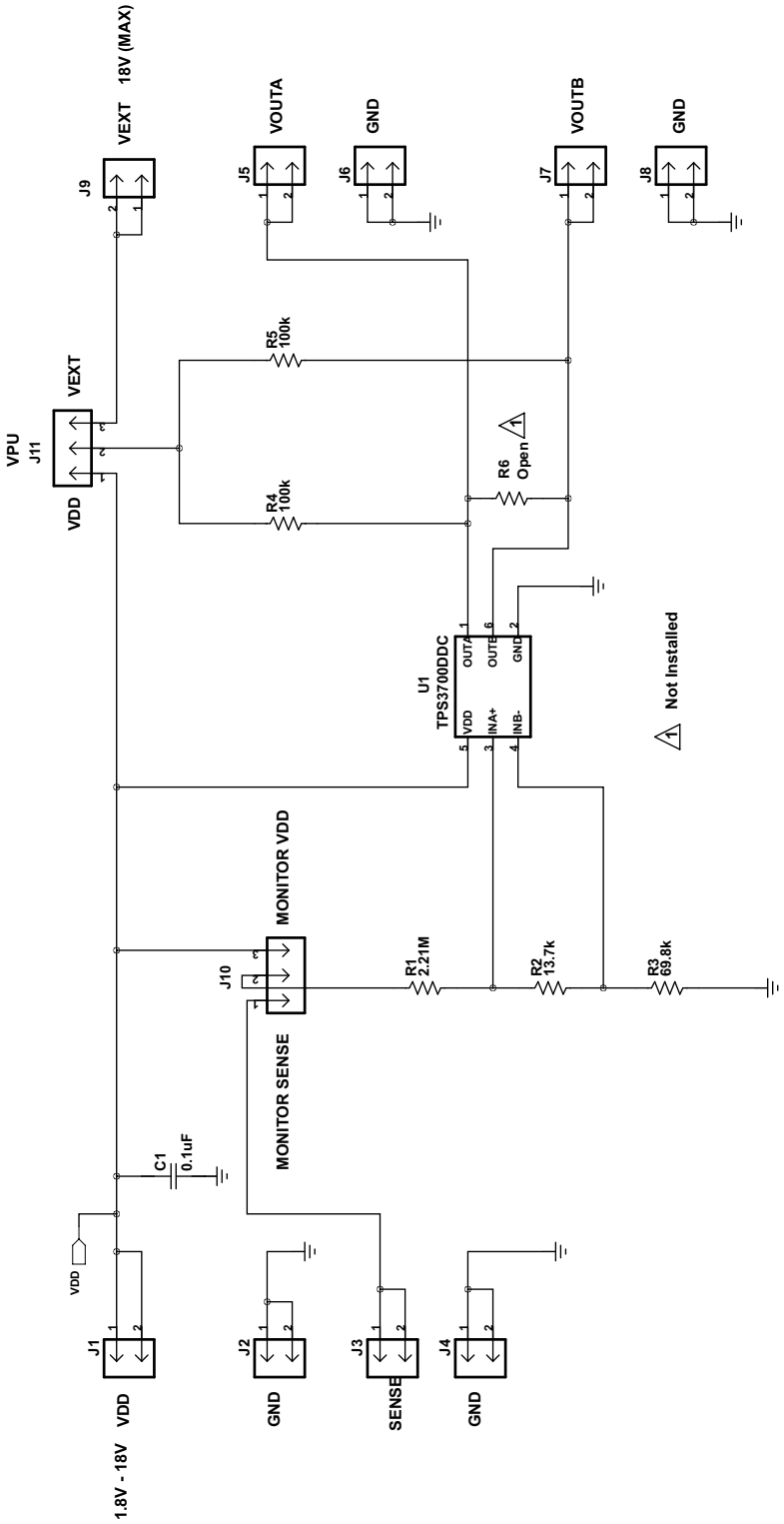

Figure 6. TPS3700EVM-114 Schematic

6 Bill of Materials

Table 3 lists the bill of materials for the TPS300EVM-114.

Table 3. TPS3700EVM-114 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	0.1 µF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	STD	STD
9	J1-9	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	J10-11	PEC03SAAN	Header, Male 3-pin, 100-mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	R1	2.21 MΩ	Resistor, Chip, 1/16 W, 1%	0603	STD	STD
1	R2	13.7 kΩ	Resistor, Chip, 1/16 W, 1%	0603	STD	STD
1	R3	69.8 kΩ	Resistor, Chip, 1/16 W, 1%	0603	STD	STD
2	R4 R5	100 kΩ	Resistor, Chip, 1/16 W, 1%	0603	STD	STD
0	R6	Open	Resistor, Chip, 1/16 W, 1%	0603	STD	STD
1	U1	TPS3700DDC	IC, High Voltage, Window Voltage Detector for Over and Undervoltage Monitoring	SOT-23	TPS3700DDC	TI

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2012) to A Revision	Page
• Changed title of document	1
• Changed comparator to voltage detector	8

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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