

# PHD22NQ20T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 08 March 2004

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Low on-state resistance
- Fast switching.

### 1.3 Applications

- DC-to-DC converters
- General purpose switching.

### 1.4 Quick reference data

- $V_{DS} \leq 200 \text{ V}$
- $I_D \leq 21.1 \text{ A}$
- $P_{tot} \leq 150 \text{ W}$
- $R_{DSon} \leq 120 \text{ m}\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view <span style="float: right;">MBK091</span></p> <p><b>SOT428 (D-PAK)</b></p>	<p>MBB076</p>
2	drain (d) <span style="color: red;">[1]</span>		
3	source (s)		
mb	mounting base; connected to drain (d)		

[1] It is not possible to make a connection to pin 2 of the SOT428 package.



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### 3. Ordering information

Table 2: Ordering information

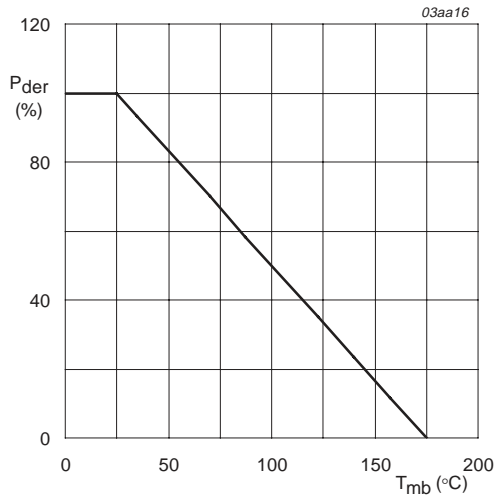
Type number	Package		Version
	Name	Description	
PHD22NQ20T	D-PAK	Plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428

### 4. Limiting values

Table 3: Limiting values

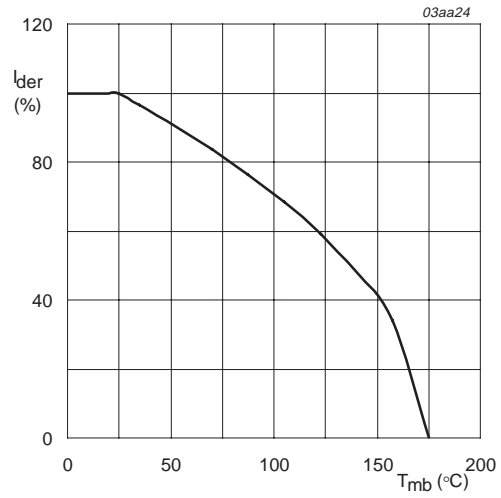
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	200	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	200	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2 and 3</b>	-	21.1	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2</b>	-	14.9	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b>	-	42.2	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <b>Figure 1</b>	-	150	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	21.6	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	42.2	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 9.3\text{ A}$ ; $t_p = 0.13\text{ ms}$ ; $V_{DD} \leq 200\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	150	mJ



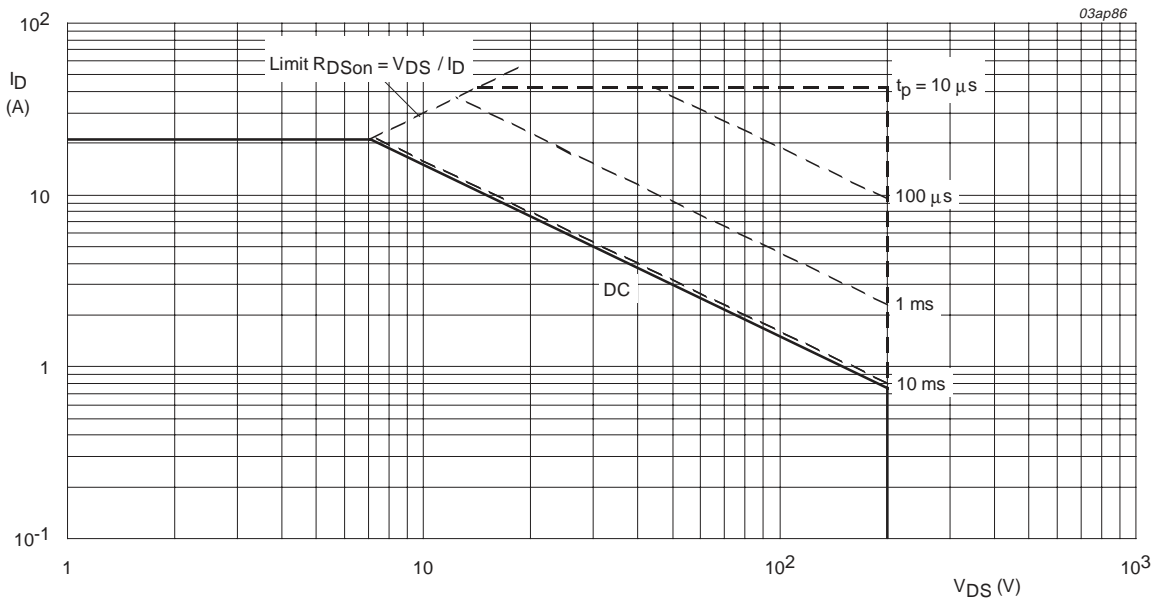
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10 V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

### 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.0	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; vertical in still air; SOT428 minimum footprint	-	75	-	K/W
		mounted on a printed-circuit board; vertical in still air; SOT404 minimum footprint	-	50	-	K/W

#### 5.1 Transient thermal impedance

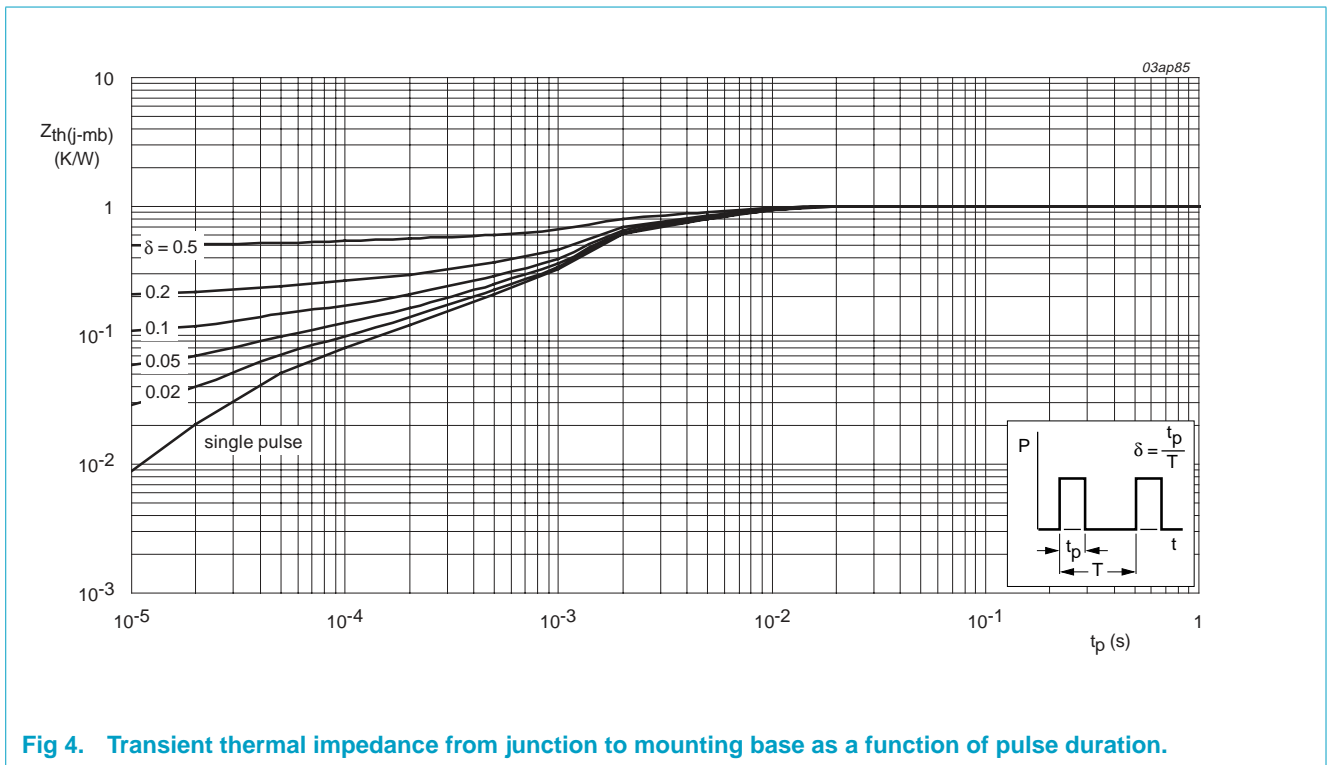
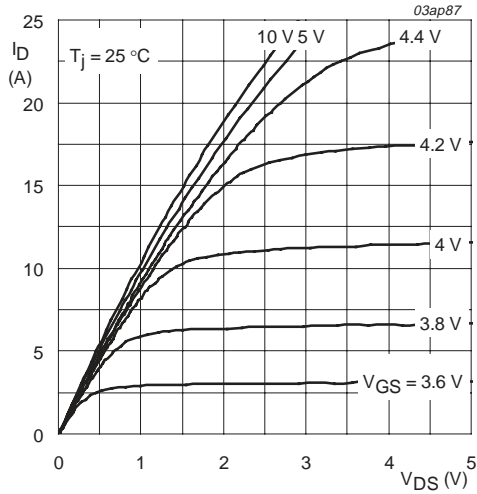


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 6. Characteristics

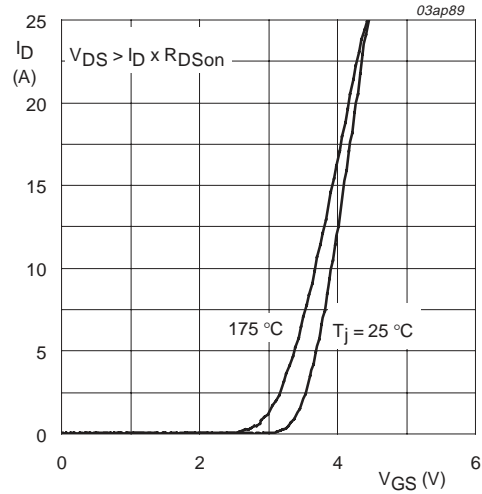
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	200	-	-	V
		T <sub>j</sub> = -55 °C	178	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <b>Figure 9</b>				
		T <sub>j</sub> = 25 °C	2	3	4	V
		T <sub>j</sub> = 175 °C	1	-	-	V
		T <sub>j</sub> = -55 °C	-	-	4.4	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 160 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	10	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 12 A; <b>Figure 7 and 8</b>				
		T <sub>j</sub> = 25 °C	-	98	120	mΩ
		T <sub>j</sub> = 175 °C	-	274	336	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 15 A; V <sub>DD</sub> = 160 V; V <sub>GS</sub> = 10 V;	-	30.8	-	nC
Q <sub>gs</sub>	gate-source charge	<b>Figure 13</b>	-	5	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	11.3	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;	-	1380	-	pF
C <sub>oss</sub>	output capacitance	<b>Figure 11</b>	-	145	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	50	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 100 V; R <sub>L</sub> = 5.6 Ω;	-	10	-	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 5.6 Ω	-	30	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	30	-	ns
t <sub>f</sub>	fall time		-	37	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.86	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	140	-	ns
Q <sub>r</sub>	recovered charge		-	680	-	nC



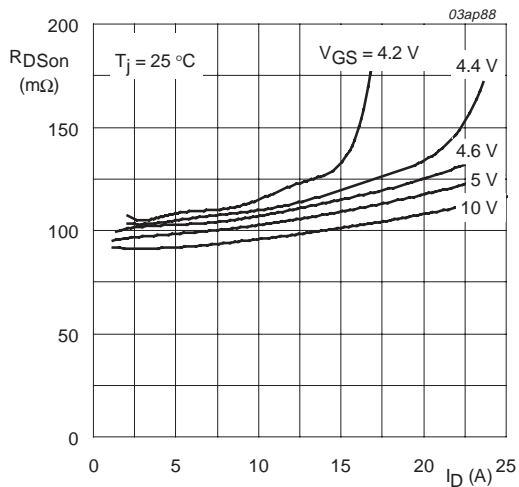
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



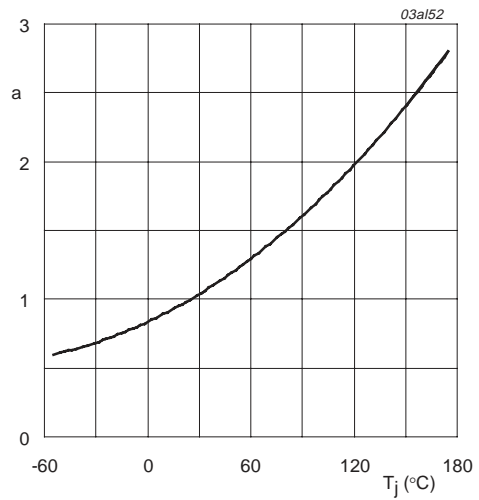
$T_j = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



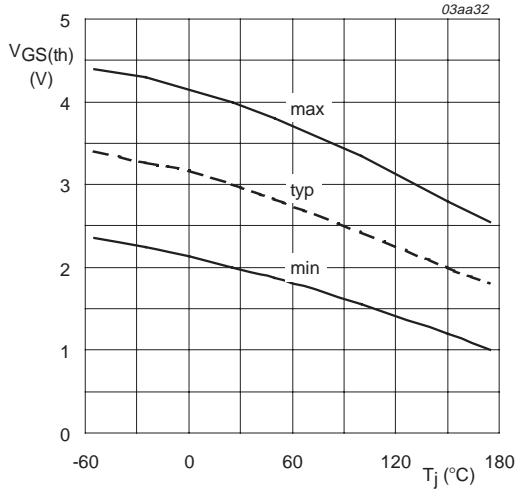
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



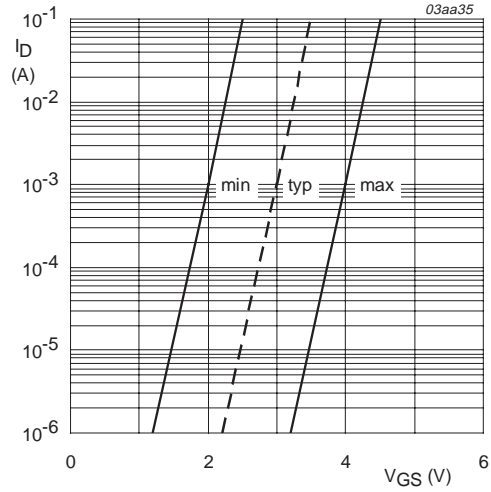
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



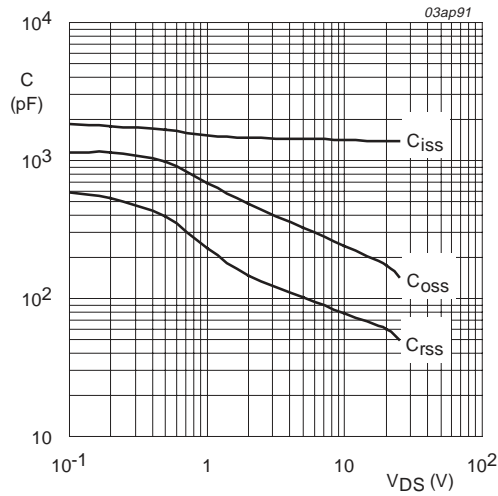
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



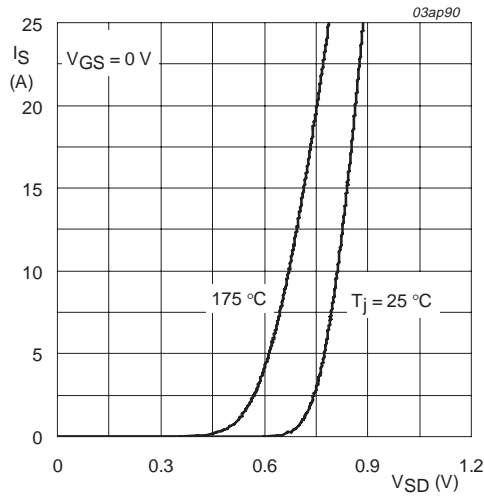
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



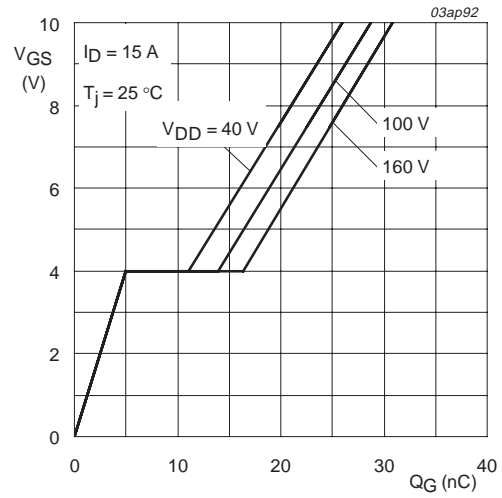
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 15\text{ A}$ ;  $V_{DD} = 40\text{ V}$ ,  $100\text{ V}$  and  $160\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



7. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

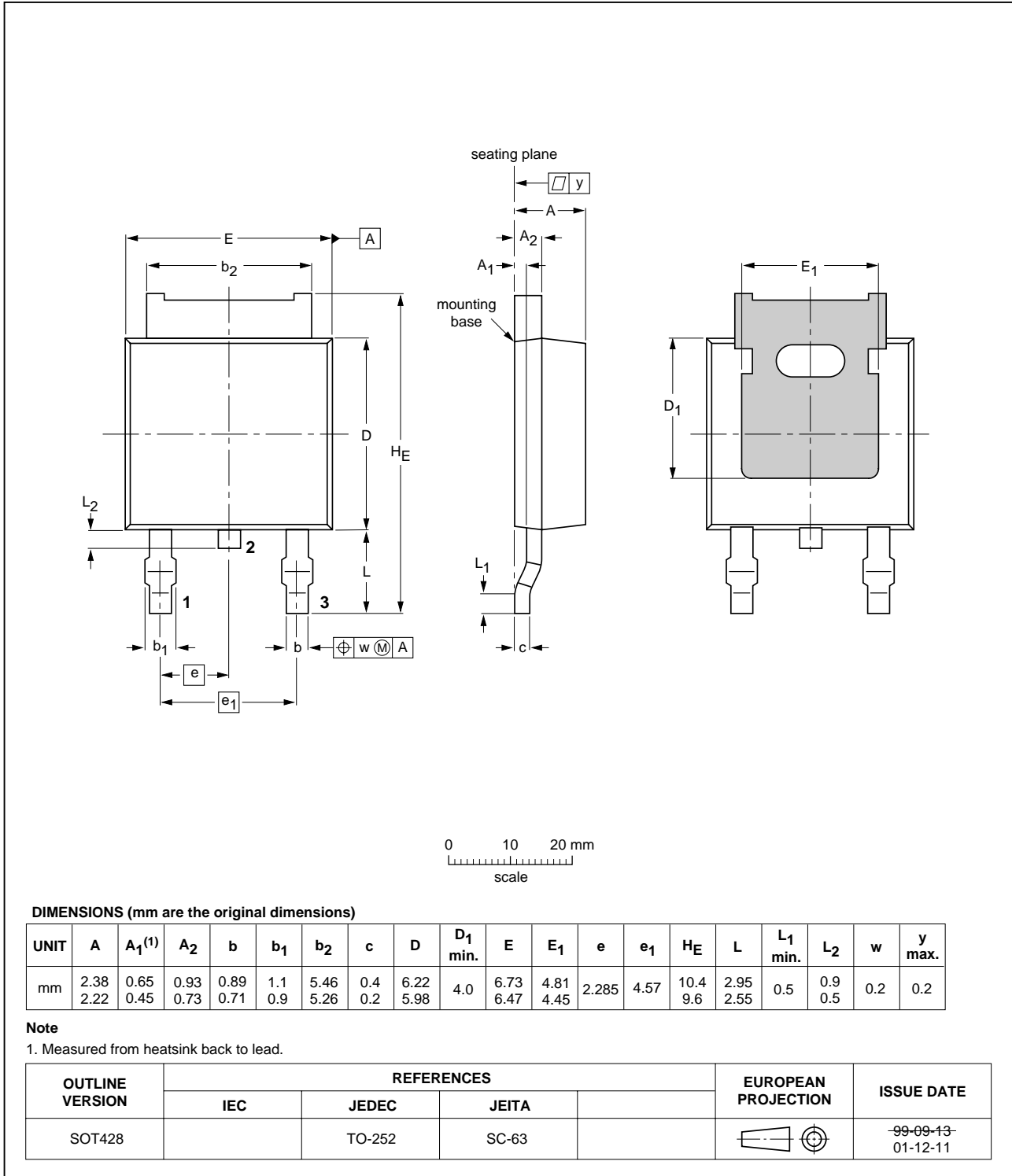


Fig 14. SOT428 (D-PAK).

## 8. Revision history

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Table 6: Revision history

Rev	Date	CPCN	Description
01	20040308	-	Product data (9397 750 12882)

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## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

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Date of release: 08 March 2004

Document order number: 9397 750 12882



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