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74VHC161284 IEEE 1284 Transceiver

General Description

The VHC161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE 1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive (± 14 mA). The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the V_{CC} supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard LOW-drive CMOS outputs. The DIR input controls data flow on the A_1 – A_8 / B_1 – B_8 transceiver pins.

Features

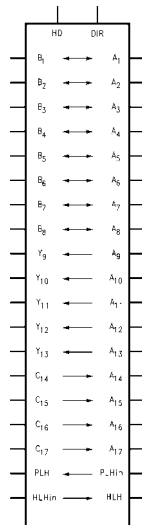
- Supports IEEE 1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Replaces the function of two (2) 74ACT1284 devices
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- Inputs and outputs on cable side have internal pull-up resistors
- Flow-through pin configuration allows easy interface between the Peripheral and Host

Ordering Code:

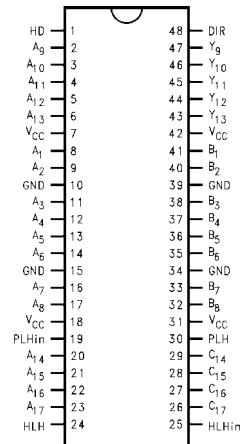
| Ordering Number | Package Number | Package Description |
|-----------------|----------------|---|
| 74VHC161284MEA | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74VHC161284MTD | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|----------------------------------|---------------------------------------|
| HD | HIGH Drive Enable Input (Active HIGH) |
| DIR | Direction Control Input |
| A ₁ -A ₈ | Inputs or Outputs |
| B ₁ -B ₈ | Inputs or Outputs |
| A ₉ -A ₁₃ | Inputs |
| Y ₉ -Y ₁₃ | Outputs |
| A ₁₄ -A ₁₇ | Outputs |
| C ₁₄ -C ₁₇ | Inputs |
| PLH _{IN} | Peripheral Logic HIGH Input |
| PLH | Peripheral Logic HIGH Output |
| HLH _{IN} | Host Logic HIGH Input |
| HLH | Host Logic HIGH Output |

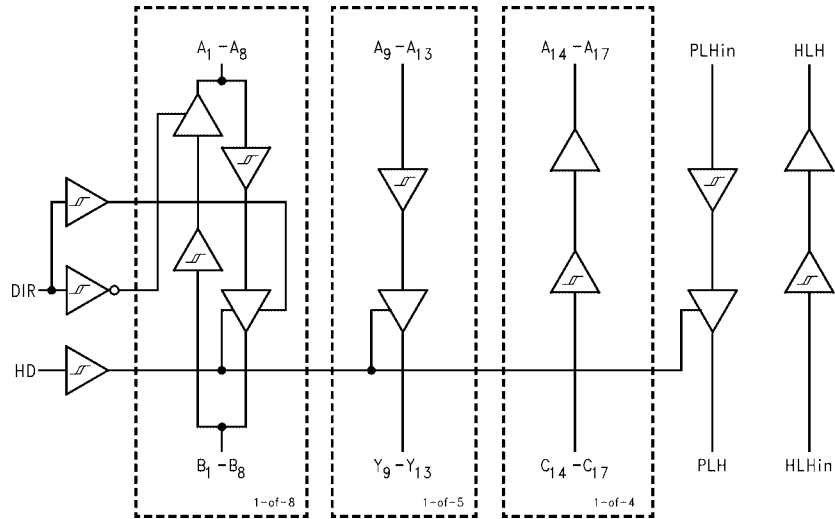
Truth Table

| Inputs | | Outputs |
|--------|----|--|
| DIR | HD | |
| L | L | B ₁ -B ₈ Data to A ₁ -A ₈ , and A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ (Note 1) C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ PLH Open Drain Mode |
| L | H | B ₁ -B ₈ Data to A ₁ -A ₈ , and A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ |
| H | L | A ₁ -A ₈ Data to B ₁ -B ₈ (Note 2) A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ (Note 1) C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ PLH Open Drain Mode |
| H | H | A ₁ -A ₈ Data to B ₁ -B ₈ A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ |

Note 1: Y₉-Y₁₃ Open Drain Outputs

Note 2: B₁-B₈ Open Drain Outputs

Logic Diagram



Absolute Maximum Ratings(Note 3)

| | | |
|---|--------------------------|------------------|
| Supply Voltage | | |
| V_{CC} | -0.5V to + 7.0V | |
| Input Voltage (V_I) (Note 4) | | |
| A ₁ -A ₁₃ , PLH _{IN} , DIR, HD | -0.5V to V_{CC} + 0.5V | |
| B ₁ -B ₈ , C ₁₄ -C ₁₇ , HLH _{IN} | -0.5V to + 5.5V (DC) | |
| B ₁ -B ₈ , C ₁₄ -C ₁₇ , HLH _{IN} | -2.0V to + 7.0V * | *40 ns Transient |
| Output Voltage (V_O) | | |
| A ₁ -A ₈ , A ₁₄ -A ₁₇ , HLH | -0.5V to V_{CC} + 0.5V | |
| B ₁ -B ₈ , Y ₉ -Y ₁₃ , PLH | -0.5V to + 5.5V (DC) | |
| B ₁ -B ₈ , Y ₉ -Y ₁₃ , PLH | -2.0V to + 7.0V* | *40 ns Transient |
| DC Output Current (I_O) | | |
| A ₁ -A ₈ , HLH | ±25 mA | |
| B ₁ -B ₈ , Y ₉ -Y ₁₃ | ±50 mA | |
| PLH (Output LOW) | 84 mA | |
| PLH (Output HIGH) | -50 mA | |
| Input Diode Current (I_{IK}) (Note 4) | | |
| DIR, HD, A ₉ -A ₁₃ , | | |
| PLH, HLH, C ₁₄ -C ₁₇ | -20 mA | |
| Output Diode Current (I_{OK}) | | |
| A ₁ -A ₈ , A ₁₄ -A ₁₇ , HLH | ±50 mA | |
| B ₁ -B ₈ , Y ₉ -Y ₁₃ , PLH | -50 mA | |
| DC Continuous V_{CC} or Ground Current | ±200 mA | |
| Storage Temperature | -65°C to + 150°C | |
| ESD (HBM) Last Passing Voltage | 2000V | |

Recommended Operating Conditions

| | | |
|---------------------------------|----------|-----------------|
| Supply Voltage | V_{CC} | 4.5V to 5.5V |
| DC Input Voltage (V_I) | | 0V to V_{CC} |
| Open Drain Voltage (V_O) | | 0V to 5.5V |
| Operating Temperature (T_A) | | -40°C to + 85°C |

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ | | Units | Conditions | |
|-------------|-----------------------------------|--|--|--------------|-------|-----------------------|------------------------------|
| | | | Guaranteed Limits | | | | |
| V_{IK} | Input Clamp Diode Voltage | 3.0 | -1.2 | | V | $I_I = -18\text{ mA}$ | |
| V_{IH} | Minimum HIGH Level Input Voltage | A _n , PLH _{IN} , DIR, HD | 4.5 - 5.5 | 0.7 V_{CC} | | V | |
| | | B _n | 4.5 - 5.5 | 2.0 | | | |
| | | C _n | 4.5 - 5.5 | 2.3 | | | |
| | | HLH _{IN} | 4.5 - 5.5 | 2.6 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | A _n , PLH _{IN} , DIR, HD | 4.5 - 5.5 | 0.3 V_{CC} | | V | |
| | | B _n | 4.5 - 5.5 | 0.8 | | | |
| | | C _n | 4.5 - 5.5 | 0.8 | | | |
| | | HLH _{IN} | 4.5 - 5.5 | 1.6 | | | |
| ΔVT | Minimum Input Hysteresis | A _n , PLH _{IN} , DIR, HD | 4.5 - 5.5 | 0.4 | | V | $V_{T^+} - V_{T^-}$ |
| | | B _n | 4.5 - 5.5 | 0.4 | | | $V_{T^+} - V_{T^-}$ |
| | | C _n | 5.0 | 0.8 | | | $V_{T^+} - V_{T^-}$ |
| | | HLH _{IN} | 5.0 | 0.3 | | | $V_{T^+} - V_{T^-}$ |
| V_{OH} | Minimum HIGH Level Output Voltage | A _n , HLH | 4.5 | 4.4 | | V | $I_{OH} = -50\ \mu\text{A}$ |
| | | | 4.5 | 3.8 | | | $I_{OH} = -8\text{ mA}$ |
| | | B _n , Y _n | 4.5 | 3.73 | | | $I_{OH} = -14\text{ mA}$ |
| | | PLH | 4.5 | 4.45 | | | $I_{OH} = -500\ \mu\text{A}$ |

DC Electrical Characteristics (Continued)

| Symbol | Parameter | V _{CC} (V) | T _A = -40°C to +85°C | | Units | Conditions |
|------------------------------------|---------------------------------------|---|---------------------------------|------|-------|---|
| | | | Guaranteed Limits | | | |
| V _{OL} | Maximum LOW Level Output Voltage | A _n , HLH | 4.5 | 0.1 | V | I _{OL} = 50 μA I _{OL} = 8 mA I _{OL} = 14 mA I _{OL} = 84 mA |
| | | | 4.5 | 0.44 | | |
| | | | 4.5 | 0.77 | | |
| | | | 4.5 | 0.7 | | |
| RD | Maximum Output Impedance | B ₁ -B ₈ , Y ₉ -Y ₁₃ | 5.0 | 55 | Ω | (Note 5)(Note 6) |
| | Minimum Output Impedance | B ₁ -B ₈ , Y ₉ -Y ₁₃ | 5.0 | 35 | Ω | (Note 5)(Note 6) |
| RP | Maximum Pull-Up Resistance | B ₁ -B ₈ , Y ₉ -Y ₁₃ , C ₁₄ -C ₁₇ | 5.0 | 1650 | Ω | |
| | Minimum Pull-Up Resistance | B ₁ -B ₈ , Y ₉ -Y ₁₃ , C ₁₄ -C ₁₇ | 5.0 | 1150 | Ω | |
| I _{IH} | Maximum Input Current in HIGH State | A ₉ -A ₁₃ , PLH _{IN} , HD, DIR, HLH _{IN} | 5.5 | 1.0 | μA | V _I = 5.5V V _I = 5.5V |
| | | C ₁₄ -C ₁₇ | 5.5 | 100 | | |
| I _{IL} | Maximum Input Current in LOW State | A ₉ -A ₁₃ , PLH _{IN} , HD, DIR, HLH _{IN} | 5.5 | -1.0 | μA | V _I = 0.0V V _I = 0.0V |
| | | C ₁₄ -C ₁₇ | 5.5 | -5.0 | | |
| I _{OZH} | Maximum Output Disable Current (HIGH) | A ₁ -A ₈ | 5.5 | 20 | μA | V _O = 5.5V V _O = 5.5V |
| | | B ₁ -B ₈ | 5.5 | 100 | | |
| I _{OZL} | Maximum Output Disable Current (LOW) | A ₁ -A ₈ | 5.5 | -20 | μA | V _O = 0.0V |
| | | B ₁ -B ₈ | 5.5 | -5.0 | | |
| I _{OFF} | Power Down Output Leakage | B ₁ -B ₈ , Y ₉ -Y ₁₃ , PLH | 0.0 | 100 | μA | V _O = 5.5V |
| I _{OFF} | Power Down Input Leakage | C ₁₄ -C ₁₇ , HLH _{IN} | 0.0 | 100 | μA | V _I = 5.5V |
| I _{OFF} - I _{CC} | Power Down Leakage to V _{CC} | | 0.0 | 250 | μA | (Note 7) |
| I _{CC} | Maximum Supply Current | | 5.5 | 70 | mA | V _I = V _{CC} or GND |

Note 5: Output impedance is measured with the output active LOW and active HIGH (HD = HIGH).

Note 6: This parameter is guaranteed but not tested, characterized only.

Note 7: Power-down leakage to V_{CC} is tested by simultaneously forcing all pins on the cable-side (B₁-B₈, Y₉-Y₁₃, PLH, C₁₄-C₁₇ and HLH_{IN}) to 5.5V and measuring the resulting I_{CC}.

| AC Electrical Characteristics | | | | | |
|---|--|---|-------|---|-----------------------|
| Symbol | Parameter | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ | | Units | Figure Number |
| | | Min | Max | | |
| t_{PHL} | A ₁ -A ₈ to B ₁ -B ₈ | 2.0 | 30.0 | ns | Figure 1 |
| t_{PLH} | A ₁ -A ₈ to B ₁ -B ₈ | 2.0 | 30.0 | ns | Figure 2 |
| t_{PHL} | B ₁ -B ₈ to A ₁ -A ₈ | 2.0 | 30.0 | ns | Figure 3 |
| t_{PLH} | B ₁ -B ₈ to A ₁ -A ₈ | 2.0 | 30.0 | ns | Figure 3 |
| t_{PHL} | A ₉ -A ₁₃ to Y ₉ -Y ₁₃ | 2.0 | 30.0 | ns | Figure 1 |
| t_{PLH} | A ₉ -A ₁₃ to Y ₉ -Y ₁₃ | 2.0 | 30.0 | ns | Figure 2 |
| t_{PHL} | C ₁₄ -C ₁₇ to A ₁₄ -A ₁₇ | 2.0 | 30.0 | ns | Figure 3 |
| t_{PLH} | C ₁₄ -C ₁₇ to A ₁₄ -A ₁₇ | 2.0 | 30.0 | ns | Figure 3 |
| t_{SKEW} | LH-LH or HL-HL | | 6.0 | ns | (Note 9) |
| t_{PHL} | PLH _{IN} to PLH | 2.0 | 30.0 | ns | Figure 1 |
| t_{PLH} | PLH _{IN} to PLH | 2.0 | 30.0 | ns | Figure 2 |
| t_{PHL} | HLH _{IN} to HLH | 2.0 | 30.0 | ns | Figure 3 |
| t_{PLH} | HLH _{IN} to HLH | 2.0 | 30.0 | ns | Figure 3 |
| t_{PHZ} | Output Disable Time | 2.0 | 18.0 | ns | Figure 7 |
| t_{PLZ} | DIR to A ₁ -A ₈ | 2.0 | 18.0 | ns | Figure 7 |
| t_{PZH} | Output Enable Time | 2.0 | 25.0 | ns | Figure 8 |
| t_{PZL} | DIR to A ₁ -A ₈ | 2.0 | 25.0 | ns | Figure 8 |
| t_{PHZ} | Output Disable Time | 2.0 | 25.0 | ns | Figure 9 |
| t_{PLZ} | DIR to B ₁ -B ₈ | 2.0 | 25.0 | ns | Figure 9 |
| t_{pEN} | Output Enable Time HD to B ₁ -B ₈ , Y ₉ -Y ₁₃ | 2.0 | 28.0 | ns | Figure 2 |
| t_{pDis} | Output Disable Time HD to B ₁ -B ₈ , Y ₉ -Y ₁₃ | 2.0 | 28.0 | ns | Figure 2 |
| $t_{pEn} - t_{pDis}$ | Output Enable-Output Disable | | 20.0 | ns | |
| t_{SLEW} | Output Slew Rate | | | | |
| t_{PLH} | B ₁ -B ₈ , Y ₉ -Y ₁₃ | 0.05 | 0.40 | V/ns | Figure 5 |
| t_{PHL} | B ₁ -B ₈ , Y ₉ -Y ₁₃ | 0.05 | 0.40 | V/ns | Figure 4 |
| t_r, t_f | t_{RISE} and t_{FALL} B ₁ -B ₈ , Y ₉ -Y ₁₃ (Note 8) | | 120 | ns | Figure 6 (Note 10) |
| | | | 120 | ns | (Note 10) |
| Note 8: Open Drain | | | | | |
| Note 9: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type. | | | | | |
| (i) A ₁ -A ₈ to B ₁ -B ₈ , A ₉ -Y ₁₃ to Y ₉ -Y ₁₃ | | | | | |
| (ii) B ₁ -B ₈ to A ₁ -A ₈ | | | | | |
| (iii) C ₁₄ -C ₁₇ to A ₁₄ -A ₁₇ | | | | | |
| Note 10: This parameter is guaranteed but not tested, characterized only. | | | | | |
| Capacitance (Note 11) | | | | | |
| Symbol | Parameter | Typ | Units | Conditions | |
| C _{IN} | Input Capacitance | 5 | pF | V _{CC} = 0.0V (HD, DIR, A ₉ -A ₁₃ , C ₁₄ -C ₁₇ , PLH _{IN} and HLH _{IN}) | |
| C _{I/O} | I/O Pin Capacitance | 12 | pF | V _{CC} = 3.3V | |
| Note 11: Capacitance is measured at frequency = 1 MHz. | | | | | |

AC Loading and Waveforms

Pulse Generator for all pulses: Rate ≤ 1.0 MHz; $Z_0 \leq 50\Omega$; $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

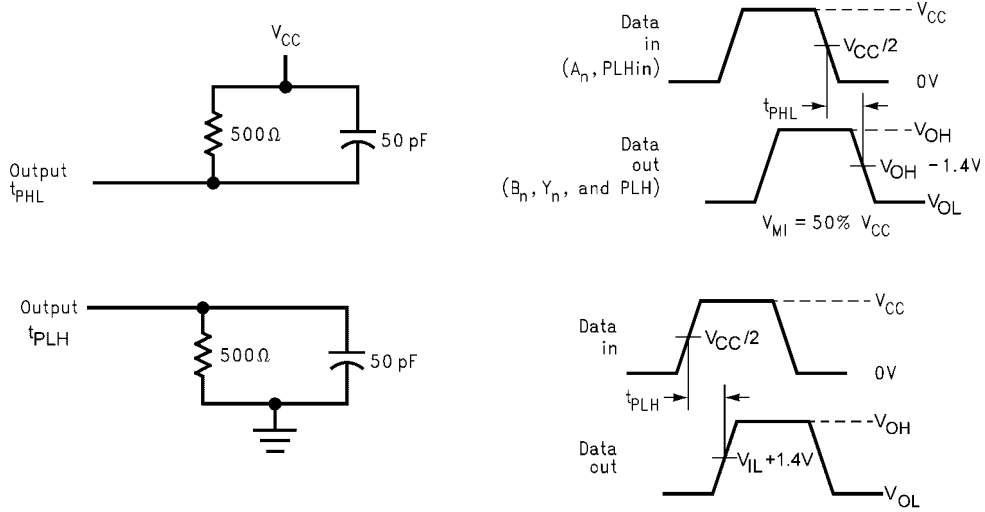


FIGURE 1. Part A to B and A to Y Propagation Delay Load and Waveforms

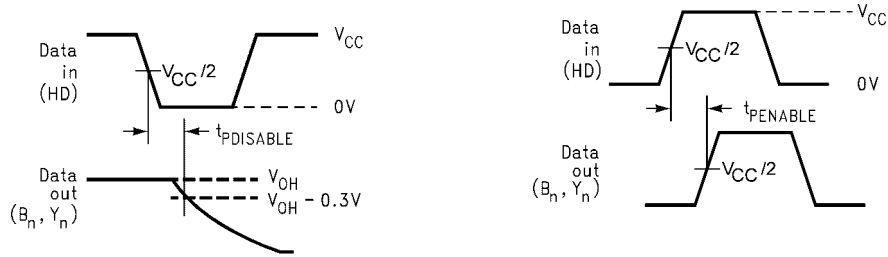


FIGURE 2. Port A to B and a to Y Output Waveforms

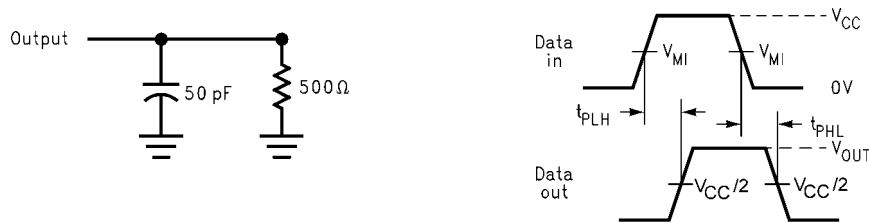


FIGURE 3. Port B to A, C to A and HLHin to HLH Propagation Delay Waveforms

AC Loading and Waveforms (Continued)

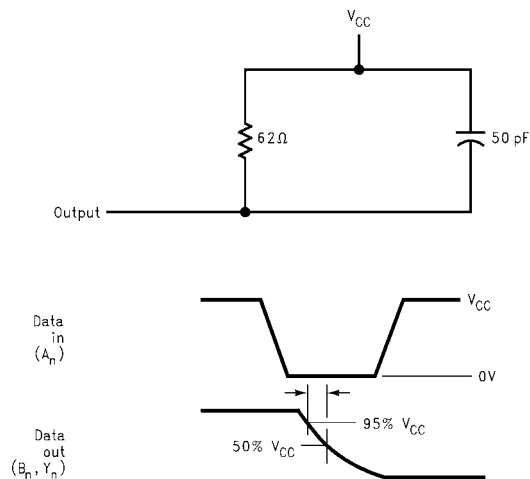


FIGURE 4. Port A to B and A to Y HL Slew Test Load and Waveforms

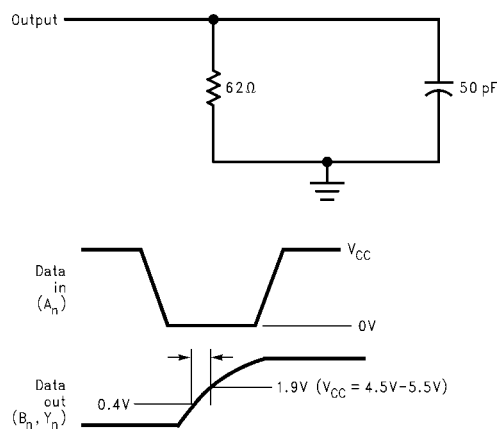
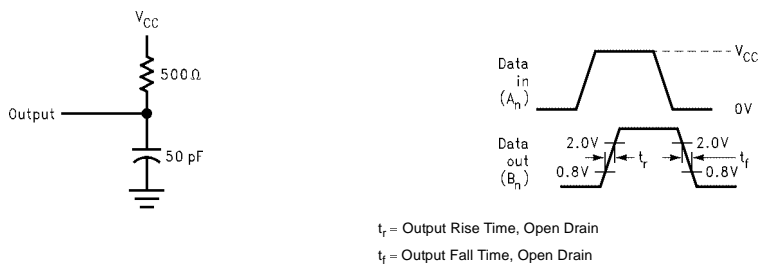


FIGURE 5. Part A to b and A to Y LH Slew Test Load and Waveforms



t_r = Output Rise Time, Open Drain
 t_f = Output Fall Time, Open Drain

FIGURE 6. t_{RISE} and t_{FALL} Test Load and Waveforms for Open Drain Outputs
 A₁-A₈ to B₁-B₈, A₉-A₁₃ to Y₉-Y₁₃

AC Loading and Waveforms (Continued)

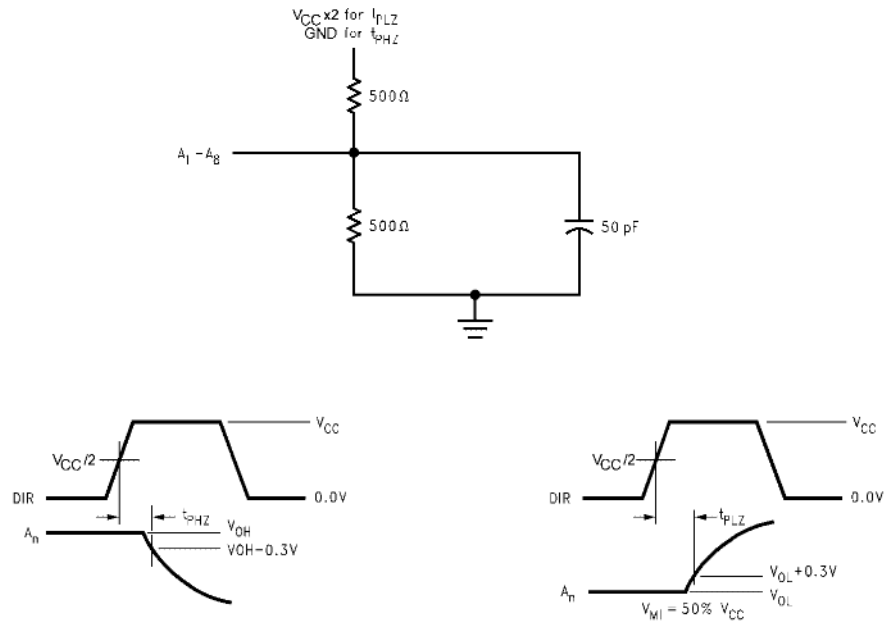


FIGURE 7. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1-A_8

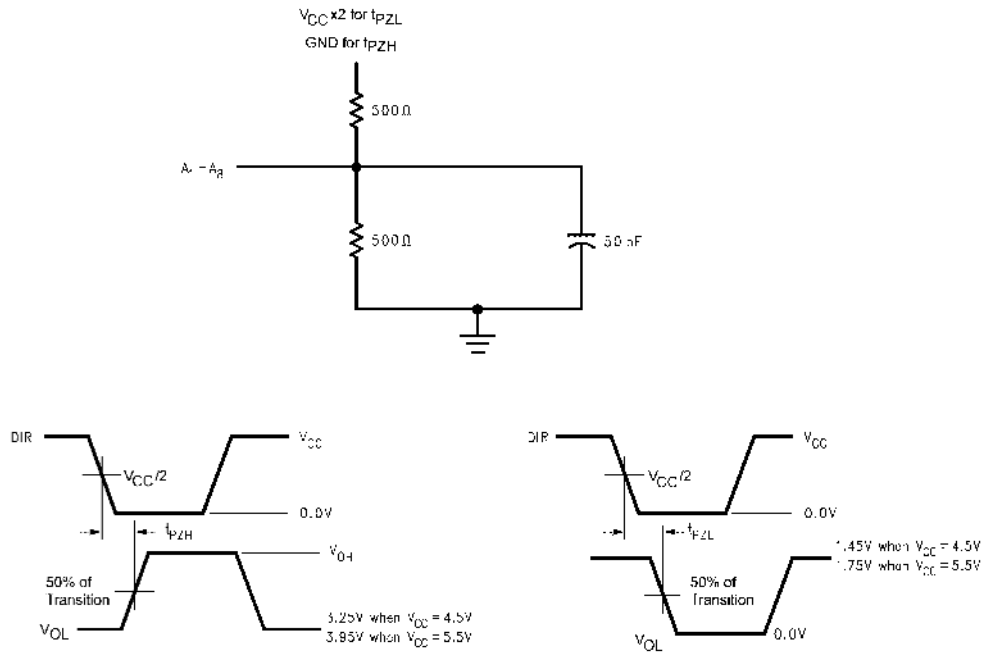
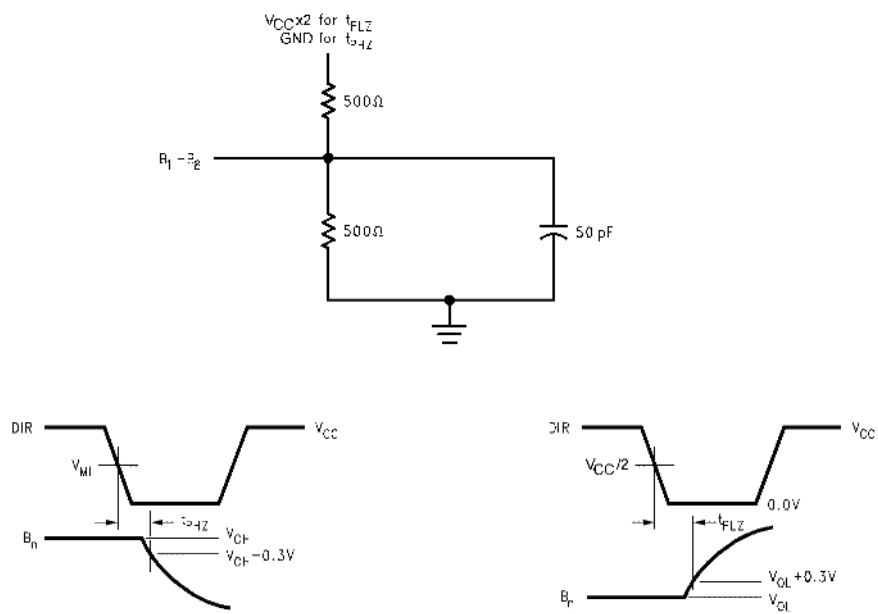


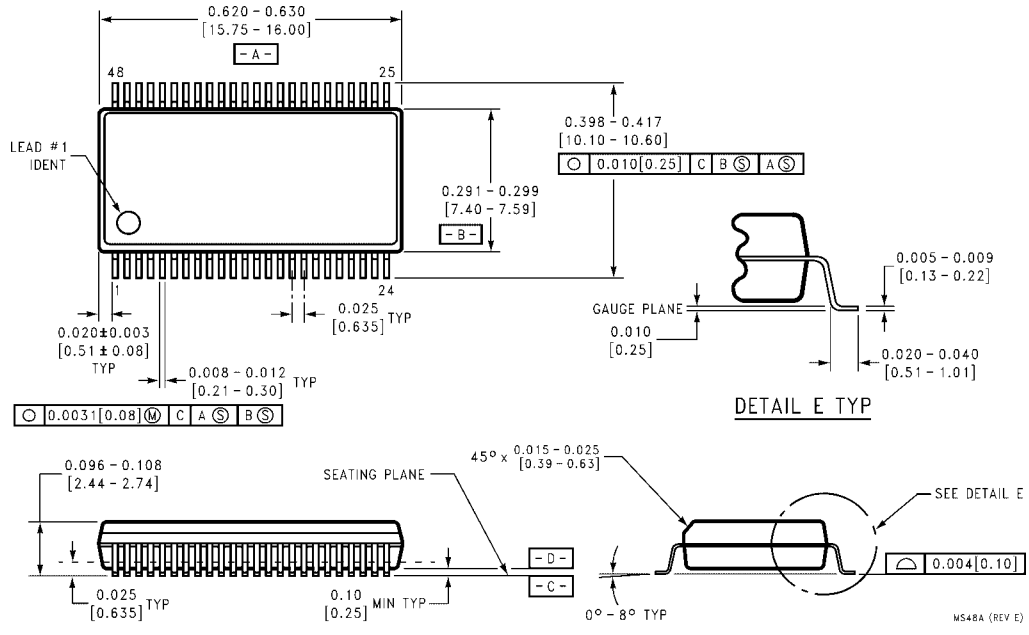
FIGURE 8. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to A_1-A_8

AC Loading and Waveforms (Continued)

FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to B_1 – B_8

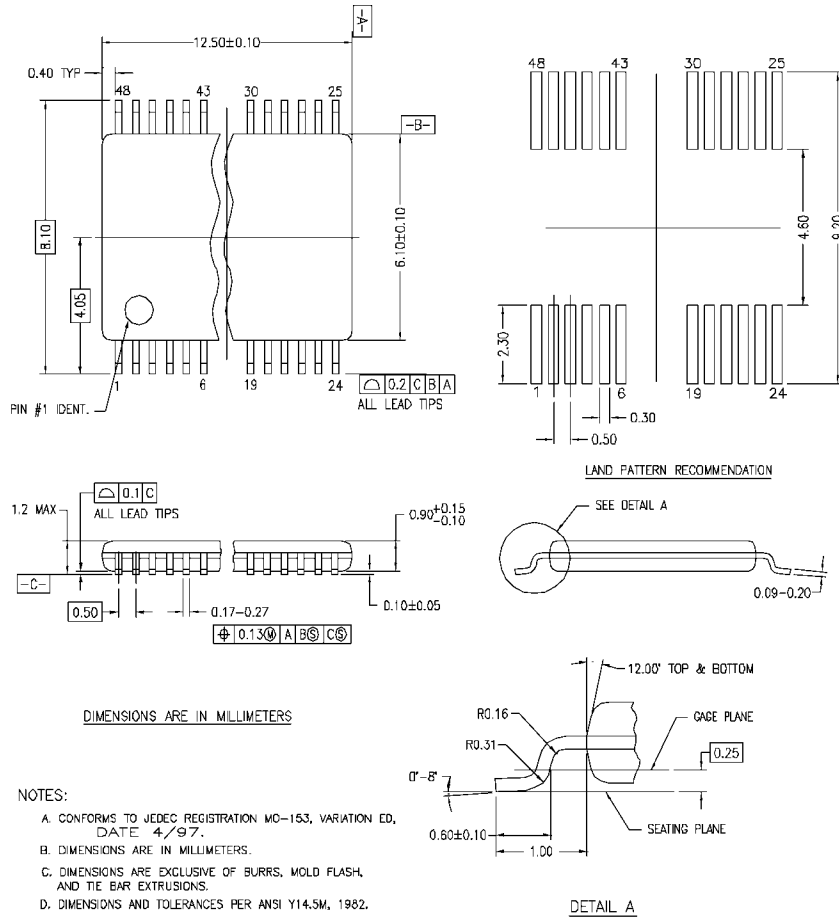
74VHC161284

Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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