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Core1553 Development Kit User's Guide

Actel
POWER MATTERS

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Printed in the United States of America

Part Number: 50200184-0

Release: August 2009

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Introduction

The Core1553 Development Kit demonstration enables users to evaluate the functionality of Actel's Core1553 Development Kit (Figure 1) without having to create a complete MIL-STD-1553B-compliant system. You can use the files included with the Core1553 Development Kit to program a Fusion Advanced Development Kit and create a 1553 bus controller, remote terminal, and bus monitor compliant with the MIL-STD-1553B standard. The targeted FPGA (M1AFS1500) is mounted on the Fusion Advanced Development Kit board and 1553 bus physical connections are included on the Core1553 Daughter Card, which plugs directly onto the Fusion Advanced Development Kit board. Once programmed, the development board provides the customer with a self-contained 1553 bus evaluation system.

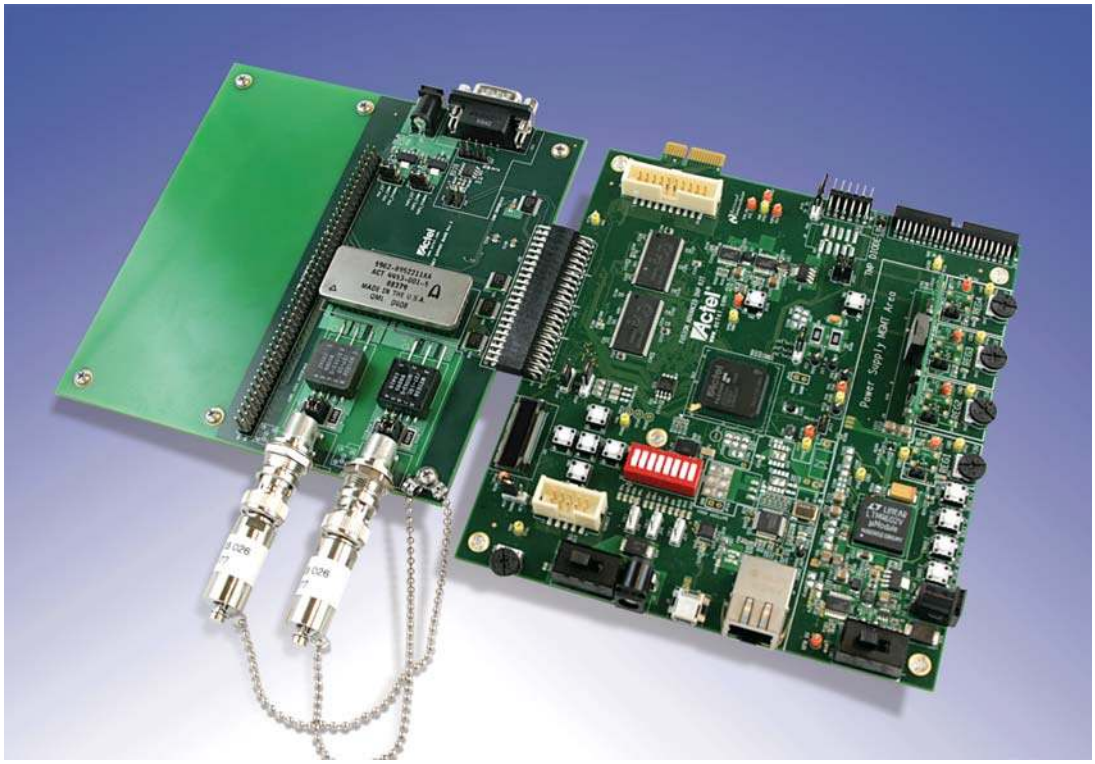

***Figure 1* • Core1553 Development Kit**

CORE1553 Development Kit Contents

The Core1553 Development Kit includes the following items:

***Table 1* • CORE1553-DEV-KIT Contents**

Ordering Code	Description
M1AFS-ADV-DEV-KIT-PWR	Fusion Advanced Development Kit with power supplies
CORE1553-SA	Core1553 Daughter Card

Note: You can order the full development kit or if you already have a Fusion Advanced Development Kit ,then order only the CORE1553-SA Daughter Card.

Core1553 Development Kit Web Resources

CORE1553-DEV-KIT Design Files

www.actel.com/download/rsc/?f=CORE1553_DEV_KIT_DF

CORE1553-DEV-KIT Schematics

www.actel.com/products/hardware/devkits_boards/core1553_fadk.aspx

Core1553BRM IP Handbook

www.actel.com/ipdocs/Core1553BRM_HB.pdf

Fusion Advanced Development Kit Documentation

www.actel.com/products/hardware/devkits_boards/fusion_adv.aspx#rsc

Core1553 Development Kit Design Files

Associated files for this demonstration can be downloaded from the Actel website: www.actel.com/download/rsc/?f=CORE1553_DEV_KIT_DF. These files include an Actel design example and programming files for the example design, and contain the following folders:

- Programming_File: Pdb programming files
- Driver: Contains the CP210x_Drivers.zip file, which has the driver for the USB-to-UART interface
- Script: Script file for testing the demo in script mode
- Designer_adb: ADB file for the demonstration design
- RTL: FPGA example design source files

Note: Core1553BRM source files are not provided in the CORE1553 Development Kit design files. Core1553BRM IP must be purchased separately.

User's Guide Contents

This user's guide describes the contents, architecture, and guidelines for working with the Core1553 Development Kit demonstration and the Core1553 Development Kit. This document provides the following:

- Detailed user information and description of the Core1553BRM demonstration design
- Detailed reference material to be used when implementing a new design using the Core1553 Development Kit

This user's guide covers these topics:

- Core1553 Development Kit overview
- Board description
- Core1553 Development Kit demonstration design
- Running the demonstration in script mode
- Running the demonstration in auto mode
- Modifying the demonstration script
- Programming the Fusion FPGA on M1AFS-ADV-DEV-KIT
- Communication from HyperTerminal to M1AFS-ADV-DEV-KIT

Required Items

The following items are required in order to run the Core1553 Development Kit demonstration:

- HyperTerminal or similar serial communication program
- PC system running Windows® XP operating system or later
- FlashPro software, v8.5 or later

Optional Items

- Core1553BRM obfuscated or RTL license
- Libero® Integrated Design Environment (IDE) v8.5 or later
- Silicon Explorer II or any signal analyzer
- Silicon Explorer v5.2 or later

1 – Core1553 Development Kit Hardware

Core1553BRM IP Core

Actel Core1553BRM provides a complete MIL-STD-1553B bus controller (BC), remote terminal (RT), or bus monitor terminal (BM or MT). Core1553BRM can be configured to provide all three 1553 functions or any combination thereof. The core is supported in all recent Actel flash, antifuse, and radiation-tolerant product families. A typical system implementation using Core1553BRM is shown in Figure 1-1.

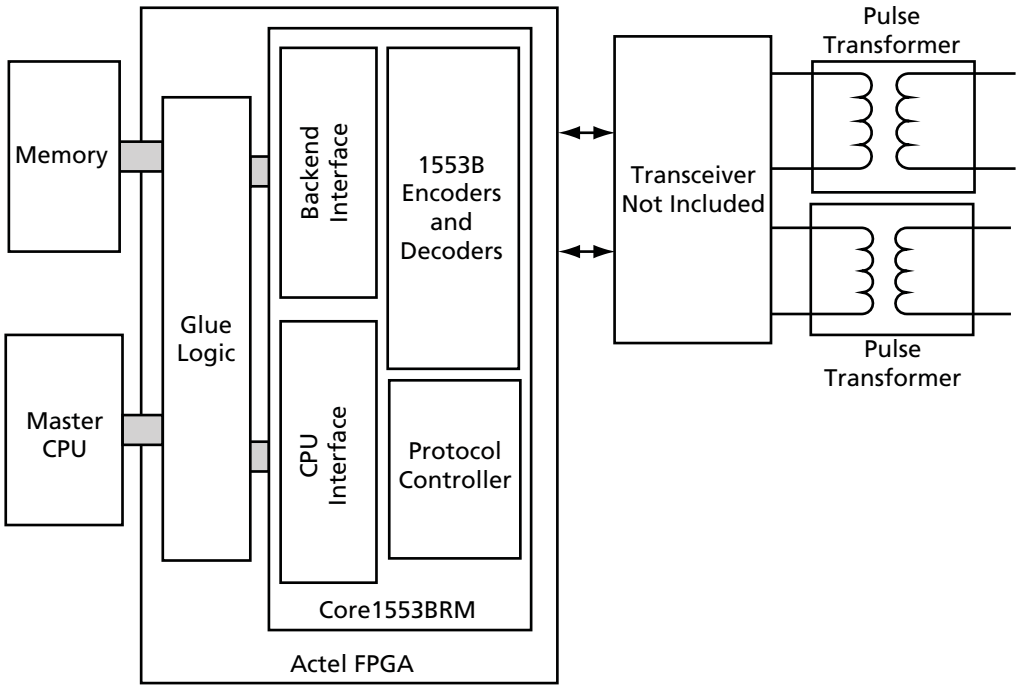

Figure 1-1 • **Typical Core1553 Application**

A typical Core1553BRM system requires a connection to an external CPU, used to set up the core registers and initialize the data tables in memory. To facilitate system integration, Core153BRM is register-compatible with the SUMMIT™ family of 1553B devices from Aeroflex®.

The external memory block is used to store the received and transmitted data. This memory can be internal or external to the FPGA, depending upon the family targeted. The core interfaces to the 1553 bus through an external 1553 transceiver and transformer.

Core1553BRM is available in the following versions:

- An evaluation version that allows core simulation with Actel Libero IDE or ModelSim®.
- An obfuscated version that provides obfuscated RTL and precompiled testbenches.
- An RTL version with full access to the source code.

Refer to the *Core1553BRM Handbook* for more information.

Core1553 Development Kit

The Core1553 Development Kit includes the Fusion Advanced Development Kit board and the Core1553 Daughter Card. This section describes the board components briefly. The CD contains the board schematic and other required files.

Fusion Advanced Development Kit Board Description

The Fusion Advanced Development Kit (Figure 1-2) provides a low-cost board for the system management platform, using Actel Fusion® FPGA. The evaluation board supports an ARM® Cortex™-M1 embedded processor on a Fusion device in the FGG484 package. The evaluation board includes the following:

- Ethernet and USB-to-UART interface for communication with the Fusion FPGA
- SRAM, parallel flash, and SPI flash
- I^2C interface, organic light-emitting diode (OLED)
- Temperature diode, potentiometer, and pulse-width modulation (PWM) circuit
- Mixed-signal header for several daughter boards to be attached for extended mixed-signal applications
- Programming stick header so the low-cost programming stick (LCPS) can be attached to the board for programming

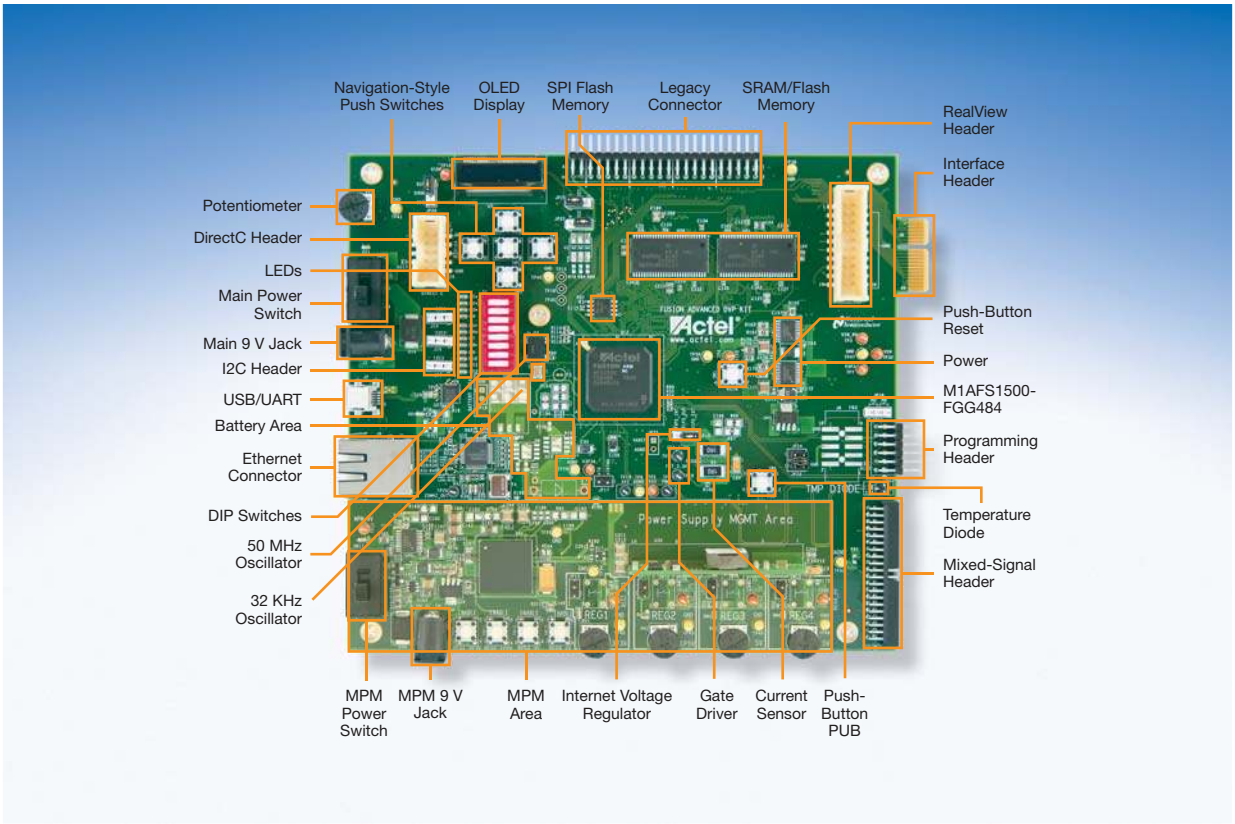

Figure 1-2 • **Fusion Advanced Development Kit**

Core1553 Daughter Card Description

The Core1553 Daughter Card (Figure 1-3) has 1553B bus components mounted. Table 1 lists the main 1553 components and their locations.

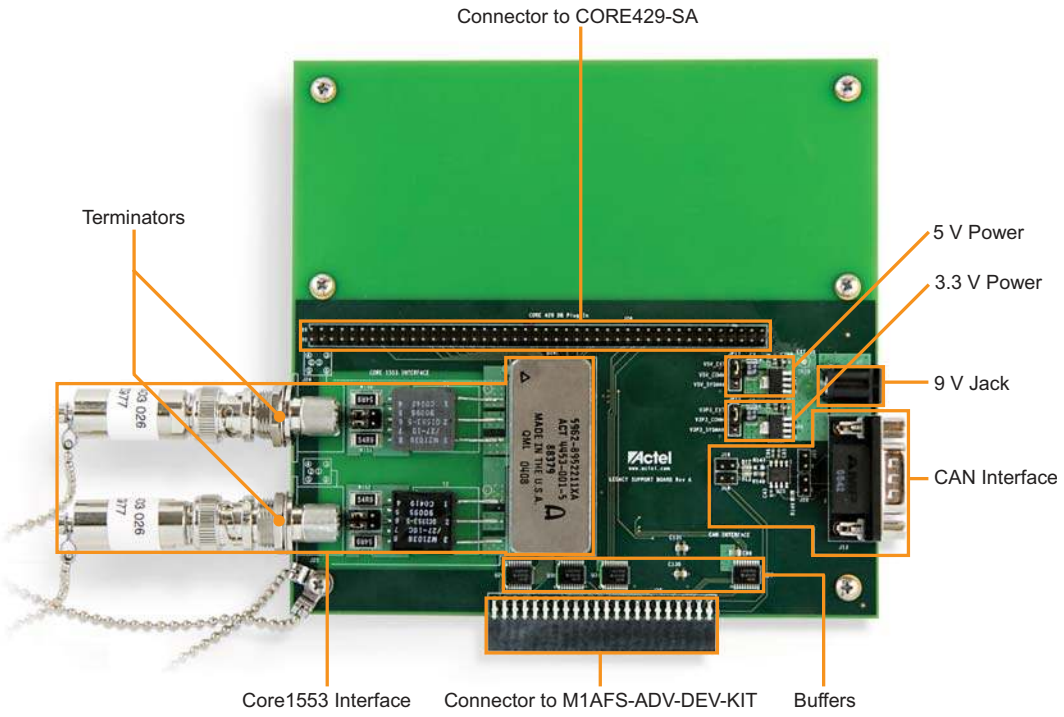

Figure 1-3 • **Core1553 Daughter Card**

Table 1 • **Core1553 Daughter Card Components**

Component	Part Number	Manufacturer	Location
1553B transceiver	BU-63147F3-320	Data Device Corporation	U26
1553B transformers	HLP600	Beta	T1 and T2
Triax sockets	CBBJR79	Trompeter	J24 and J25

Note: J24 is designated as Bus A and J25 as Bus B in this demonstration design.

Jumpers J22 and J23

Jumpers J22 and J23 are used to configure the type of coupling to be used when connecting to a 1553B bus—either Direct or Transformer Coupling (Figure 1-4 on page 1-12). Both Bus A and Bus B

can be configured independently, based upon your needs and the type of 1553B device to be attached.

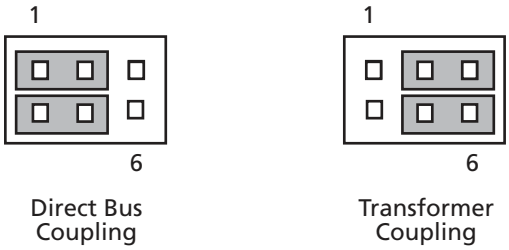

Figure 1-4 • **Jumpers J5 and J7 Settings**

Jumpers J11 and J17

The daughter card must be connected to an external 9 V supply. When using the external power supply, make sure that jumper JP11 and JP17 are properly installed as described in Table 1-1.

Table 1-1 • **Jumper JP11 and JP17 Settings**

Jumper	Function	Default Setting
JP11	Jumper to select either external 3.3 V or 3.3 V provided through connector	Pin 1–2
JP17	Jumper to select either external 5 V or 5 V provided through legacy connector	Pin 1–2

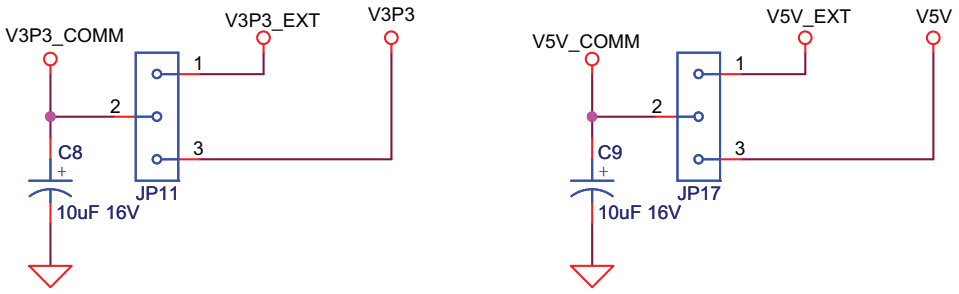

Figure 1-5 • **Core1553 Daughter Card**

2 – Core1553BRM Demonstration Design

The Core1553BRM demonstration design implements two complete Core1553BRM cores into a single M1AFS1500 FPGA and allows you to evaluate the 1553 bus controller, remote terminal, and bus monitor (monitor terminal) functions of the core (Figure 2-1). In addition, the design allows for the monitoring of 1553B bus activity using Actel Silicon Explorer II hardware.

FPGA Design

The demonstration design contained within the M1AFS1500 FPGA consists of the following blocks:

- Two complete Core1553BRM cores
- 1553B bus interface
- Memory interface
- Bus arbiter
- Control sequencer
- UART
- DIP switches
- LEDs
- Data generator
- External memory

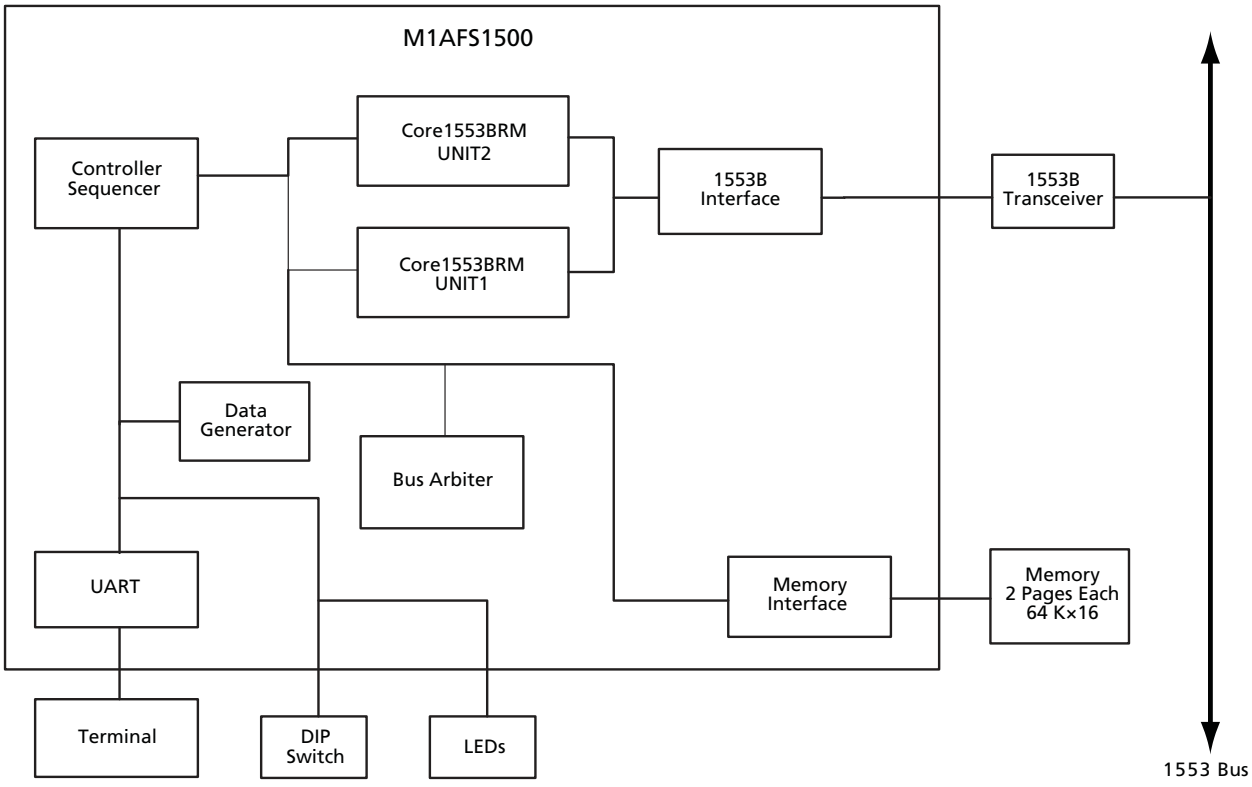

Figure 2-1 • **Core1553BRM Demo Design Architecture**

Core1553BRM

Each Core1553BRM block can be configured as a bus controller or a remote/monitor terminal and operates off 16 MHz clock. This 16 MHz clock is generated using a PLL from an on-board 50 MHz clock. The two blocks are configured to share CPU and memory busses. Each core has access to its own 64 K words of memory within the off-chip memory. The demo design allows configuring one core as a bus controller and the other as remote/monitor terminal, depending on dip switch settings.

1553B Bus Interface

The 1553B bus interface block allows the Core1553BRM blocks to be connected and form a complete 1553 bus without any external transceivers and transformers. This block also allows the Core1553BRM blocks to interface to an off-chip 1553B bus transceiver that is fitted on the Core1553 Daughter Card.

Memory Interface

The memory interface ties the internal data bus to the on-board external memories, allowing each core to interface its dedicated memory space.

Bus Arbiter

This block allows the control sequencer block and the two Core1553BRM cores to access the internal bus.

Control Sequencer

The control sequencer connects to the BRM CPU interfaces and replaces the CPU in a typical system. This block handles system interrupts and provides user interfaces via an external terminal over a serial interface.

UART

The UART block implements a simple RS-232 interface running at 115,200 baud, tied to the off-chip USB-to-UART interface. The USB-to-UART interface enables HyperTerminal on a PC to communicate with the Fusion FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows operating system. With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the Fusion FPGA device.

DIP Switches

Configuration of the demonstration design is handled by the 8-position DIP switch located at position S1. Setting the DIP switch controls the operating mode of each Core1553BRM, sets the remote terminal address, and can enable the bus loopback logic internal to the FPGA. Figure 2-2

shows DIP switch bank. These switches are wired to inputs of the FPGA so that open will correspond to logic 1 (4.7 K pull-up to 3.3 V) and closed will correspond to logic 0 (GND).

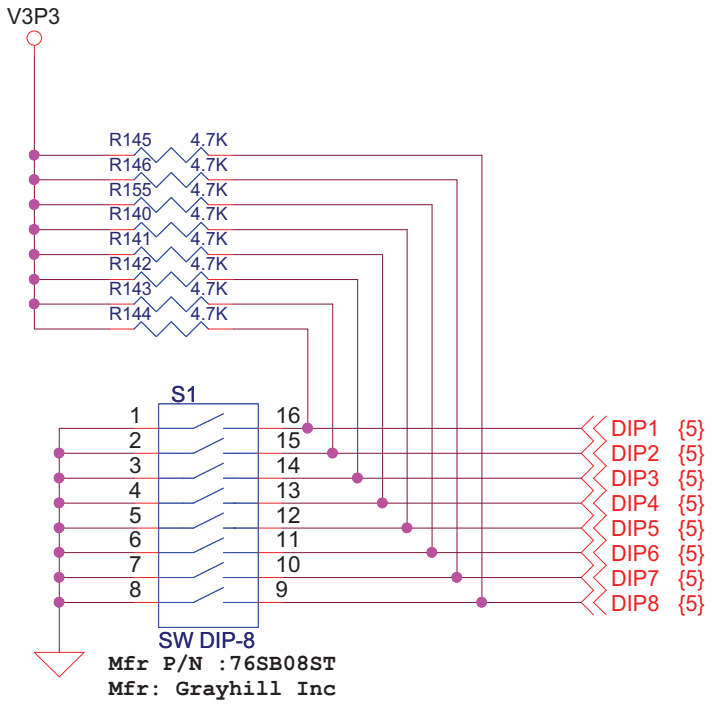

Figure 2-2 • **DIP Switch Schematic**

Switches 1 and 2

Switches 1 and 2 control the basic operating modes of the demonstration design.

00: Qualification testing mode. Not used for the demonstration design.

01: Script mode (non-initialization mode). The BRM core is not initialized. The core is set up via the UART interface.

10: Auto mode. Sets one Core1553BRM core as bus controller and the other as remote/monitor terminal and gets the data from internal data generator. Upon power-up, the state machine within the control sequencer steps through the following set of commands to be sent to the two BRM cores:

1. Sends configuration setting through UART.
2. Sets frame time to 0.75 seconds.
3. RT to BC transfer (SA = 25, WC = 9). RT to transmit the data from Data generator block.
4. BC generates an interrupt.
5. BC to RT transfer (SA = 2, WC = 9). BC will transmit its Data generator block data.
6. BC to RT transfer (SA = 1). BC transmits test data.
7. Waits for frame time to complete and then jumps to state 3.
8. End of frame

When the interrupt in state 4 occurs, the control sequencer increments the state 6 word count by 2. This should be observable on HyperTerminal and the bus traffic acquired by Silicon Explorer II or any logic analyzer. If a 1553 message fails, then the control sequencer will jump to state 8 and stop. SA stands for 1553B subaddress; WC stands for word count.

11: Reserved

Switches 3 and 4 (Auto Mode)

In Auto mode, switches 3 and 4 control which Core1553BRM core is the bus controller.

01: BRM 1 is the BC, BRM 2 is RT 2.

10: BRM 2 is the BC, BRM 1 is RT 1.

11: No BC, BRM 1 is RT1, and BRM 2 is RT 2.

00: No BC, BRM 1 is RT1, and BRM 2 is RT 2.

Switch 5 (Auto and Script Modes)

In Auto and Script modes, this switch sets the autobus/loopback feature.

1: 1553B buses are within the FPGA Loopback mode.

0: External 1553 transceiver is used.

Switches 6, 7, and 8 (Auto Mode)

In Auto mode, these switches set the remote terminal address to be used in the command words sent by the bus controller. Address values can be set in the range of 000 to 111. The demonstration configuration sets these switches to 010 (BRM core 2 is configured as remote terminal 2).

Switches 3 through 8 (Qualification Testing Mode)

In qualification testing mode, these switches set the RT address parity and RT address that the single active BRM core will use in Qualification mode. Switch 3 is the parity and 4 to 8 are the RT address.

LEDs

There are twelve LEDs (Figure 2-3) on the board used to indicate the status of the two BRM cores and the message traffic between them. Table 2-1 shows the LEDs board location and functions.

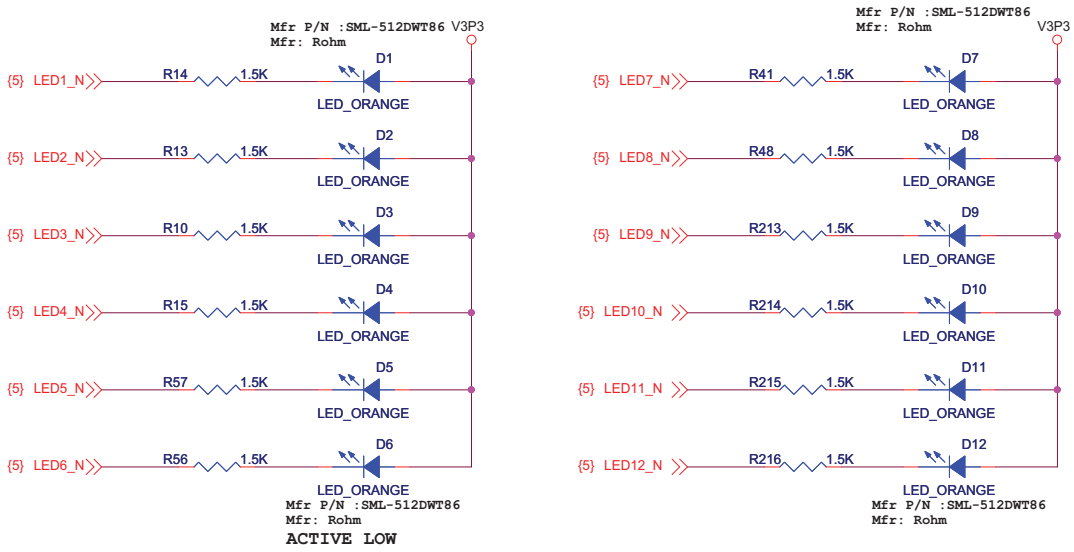

Figure 2-3 • **LEDs on M1AFS-ADV-DEV-KIT Board**

Table 2-1 • **Demonstration Board LEDs**

LED	Board Location	Function
1	D1	Heartbeat, flashes at 2 KHz
2	D2	Not used
3	D3	BRM core 1 busy
4	D4	BRM core 2 busy
5	D5	Data compare error
6	D6	Message of failure interrupt
7	D7	SRAM1 byte High enable
8	D8	SRAM1 byte Low enable
9	D9	SRAM2 byte High enable
10	D10	SRAM2 byte Low enable
11	D11	SRAM1 and SRAM2 output enable
12	D12	SRAM1 and SRAM2 write enable

Data Generator

The gata generator block generates data for 1553B messages within the demonstration design. This data are mainly used during Auto mode.

External Memory

Core1553BRM requires a connection memory interface. It supports up to 128 Kbytes of memory, but it mainly depends on the design. In the demonstration design, the bus arbiter allows the controller and two cores to access the memory, which provides 64 K words of memory for each of the cores. The two on-board SRAMs on the M1-embedded Fusion Advanced Development Kit board are used for that purpose.

Interpreting the HyperTerminal Display

Once programmed with the Core1553BRM demonstration design and the board is powered up, the HyperTerminal display will give information regarding the core configuration. This information is displayed in the following form:

```
Core1553BRM XYZZ
```

The meaning of these codes depends upon the mode in which the core was powered up.

Auto mode

While in Auto mode:

- X indicates which BRM core is configured as the bus controller.
- Y: L = Loopback mode; T = Transceiver mode.
- ZZ indicates the remote terminal address for the RT.

Example display: `Core1553BRM 1L02`

Script mode (Non-Initialization mode)

While in Non-Initialization mode:

- X: N indicates Non-Initialization mode.
- Y: L = Loopback mode; T = Transceiver mode.

- ZZ indicates the settings for switches 6 to 8, but does not affect operation.

Example display: `Core1553BRM NT00`

Qualification Testing mode

While in Qualification Testing mode:

- X: Q = Qual mode; P = Qual mode, RT address parity error detected
- Y: T = Transceiver mode (only)
- ZZ indicates the RT address

Example display: `Core1553BRM QT01`

HyperTerminal Commands

Table 2-2 lists the available commands for use in controlling the demonstration design via HyperTerminal.

Table 2-2 • **Core1553BRM Demonstration Terminal Commands**

Commands	Function	Format
1	Access BRM core 1	–
2	Access BRM core 2	–
#	Comment	–
[	Handle commands without full echoing, Command File mode	–
]	Use full echoing, Interactive mode	–
C	Compare memory	c 0a00 bcda
Esc	Exit back to main prompt	–
I	Clear interrupts	–
K	TCLK is 1 MHz	–
M	Display/set memory to hex value	m 0a00 [1234]
R	Display/set register to hex value	r 00 [1234]
T	Test register	t 00 1234
X	Clear compare fail LED and TCLK counts on 1553B syncs	–
Z	Stop interrupt logging	–

HyperTerminal Commands Examples

Display register at location 00:

```
BRM1> R 00 [RETURN]
```

Set the value of register 00 of BRM unit 1 to 1234h:

```
BRM1> R1:00=0000 1234 [RETURN]
```

Display memory at location 0a00:

```
BRM1> M 0a00 [RETURN]
```

Set memory at location 0a00 of BRM unit 1 to value 1234h:

```
BRM1> M1:0a00=0000 1234 [RETURN]
```

Note: The system does not support backspace/delete. Use ESC and re-enter the command if an error is made.

Script Mode Demonstration Design

The DIP switch setting allows setting the core in script mode. In this mode the BRM cores are not initialized. The core is set up via the UART interface.

Setting Up the Demonstration Design

The Core1553BRM Development Kit boards come preprogrammed with demonstration designs. If you want to reprogram the FPGA or if the FPGA is programmed with a different design, follow the steps in "Programming the Fusion FPGA on M1AFS-ADV-DEV-KIT" section on page A-29 to program the FPGA. Once the FPGA is programmed with the correct design, you need to set up the board according to the steps below:

1. Connect one end of the USB mini cable to USB port J2 on the M1AFS-ADV-DEV-KIT board (labeled USB2 in Figure 2-4) and connect the other end to the USB port on your PC.
2. Connect one end of a 9 V power supply to power input J3 on the M1AFS-ADV-DEV-KIT board (Figure 2-4) and plug the supply into an electrical outlet.

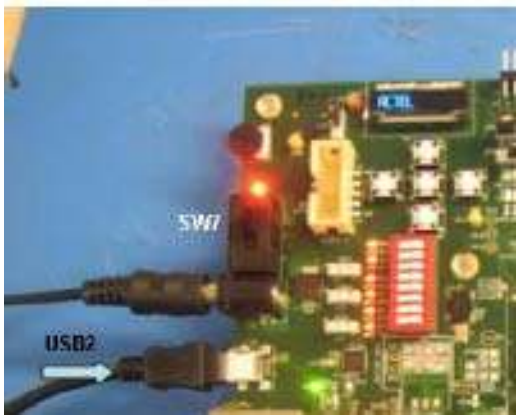

Figure 2-4 • **Connecting the USB and 9 V Power Supplies on the M1AFS-ADV-DEV-KIT Board**

3. Set the DIP switch at S1 to the default configuration of 00011010.

Note: These switches are wired to inputs of the FPGA so that open will correspond to logic 1 (4.7 K pull-up to 3.3 V) and closed will correspond to logic 0 GND.

4. Determine the COM port assigned to the USB interface. Open the Windows Control Panel and double-click the **System** icon. Click the **Hardware** tab and click the **Device Manager** button. Expand the **Ports (Com & LPT)** item in the Device Manager. Look for the CP2102 USB to UART Bridge Controller in the list of ports. The COM port in parentheses identifies the COM port assigned to this device (Figure 2-5). If you do not see CP2102, you need to install the CP210x_Drivers driver. Refer to "Installing the M1AFS-ADV-DEV-KIT Board USB Serial Driver" section on page B-31 for more information.

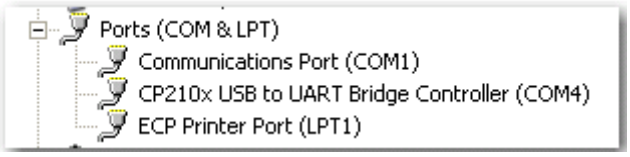

Figure 2-5 • **Determining the USB Serial Port's COM Port**

5. Open HyperTerminal and set the communications parameters as shown below. Set the COM port to match the USB serial port of the board, as shown in Step 4.

- 115,200 bits per second
- 8 data bit
- Parity set to none
- 1 stop bit
- Flow control set to none

Running the Demonstration Design in Script Mode

1. Turn the power switch SW7 on the board to the ON position.
2. Press RESET (RSTN) to restart the core. Once initialized, HyperTerminal will display the following:

```
Core1553BRM NL00 0409-1
```

   - N indicates the design is configured in Non-Initialization/Script mode.
   - L indicates that bus loopback is enabled.
   - 00 indicates the remote terminal address is set to 00.

Note: If the display shows any other message, check the DIP switch settings.

3. Press ESC to enter command mode (Figure 2-6).

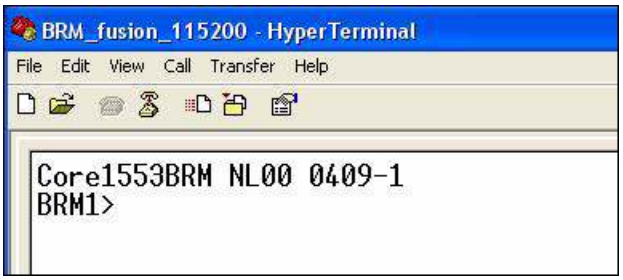

Figure 2-6 • **HyperTerminal Window in Command Mode**

4. From the **Transfer** menu, choose **Send Text File**. Browse to select the script file demo_log.txt (available in the script folder of the Core1553BRM_DEV_KIT_DS.zip file), and click **Open** to start the download.

   The demo_log.txt script programs one Core1553BRM as the BC and the other as RT 1, initializes the RT memory tables and sets up the BC to do a BC-to-RT, RT-to-BC, and RT

transmit vector commands. At the conclusion of the script, BC memory values are compared to verify that the three messages completed correctly (Figure 2-7).

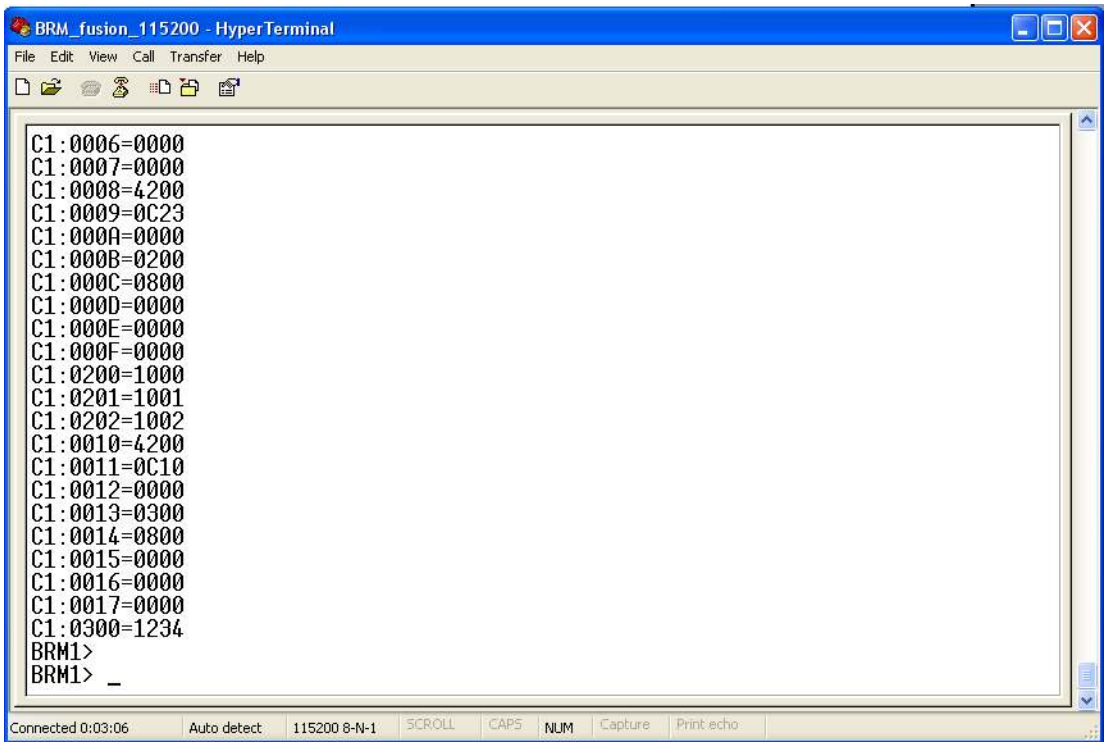

Figure 2-7 • **HyperTerminal Window – Success Message**

The HyperTerminal session will echo the commands sent to configure various register and memory settings. At the end of the download, the session will return to the prompt as shown in Figure 2-5. A question mark on the line above the prompt indicates that the script failed, or one of the

memory or register compare instructions failed (Figure 2-8). LED D5 will light to indicate a memory or register compare failure. Use RSTN and ESC to re-enter the command if an error is made.

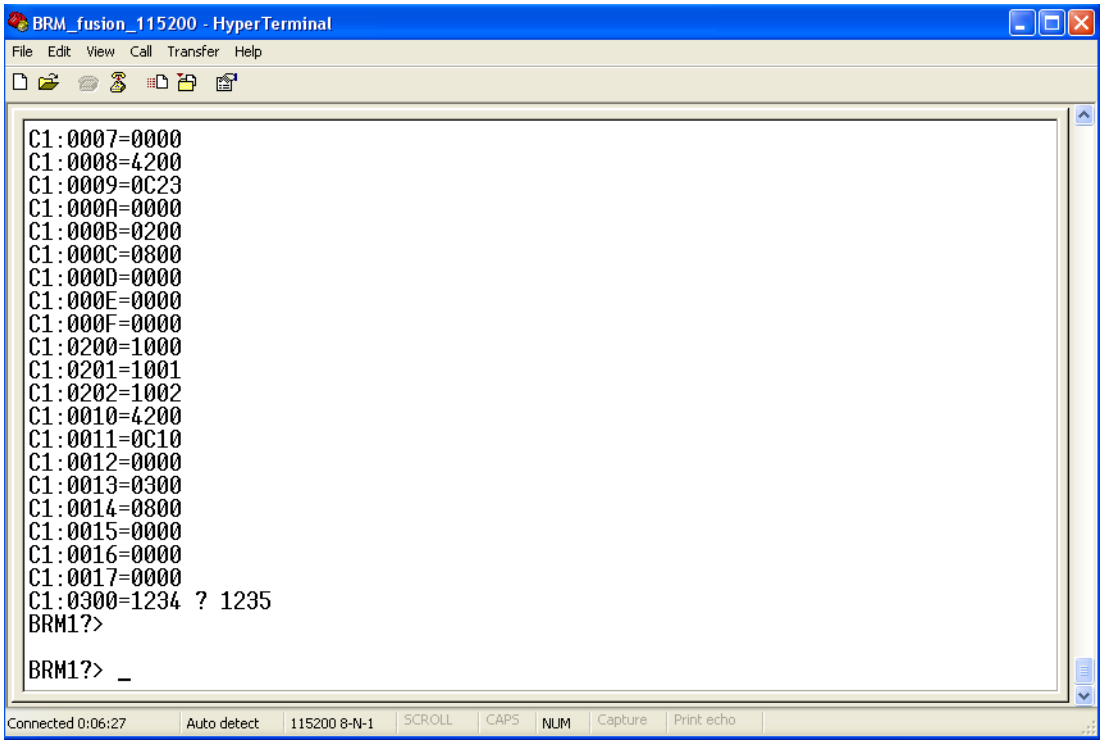

Figure 2-8 • **HyperTerminal Window – Failed Message**

Auto Mode Demonstration Design

The DIP switch setting enables you to set the core in Auto mode. In this mode and after power-up, the control sequencer will automatically configure one Core1553BRM as a bus controller and the other as a remote/monitor terminal (RT/MT). The BC is programmed to transmit data to and from the RT as specified by the control sequencer. These 1553B messages can be monitored using an external bus monitor on Silicon Explorer.

Setting Up the Demonstration Design

The Core1553BRM Development Kit boards come preprogrammed with demonstration designs. If you want to reprogram the FPGA or if the FPGA is reprogrammed with a different design, follow the steps in "Programming the Fusion FPGA on M1AFS-ADV-DEV-KIT" section on page A-29 to program the FPGA. Once the FPGA is programmed with the correct design, you need to set up the board according to the steps below:

1. Connect one end of the USB mini cable to USB port J2 on the M1AFS-ADV-DEV-KIT board (labeled USB2 in Figure 2-9) and connect the other end to the USB port on your PC.

2. Connect one end of a 9 V power supply to power input J3 on the M1AFS-ADV-DEV-KIT board (Figure 2-9) and plug the supply into an electrical outlet.

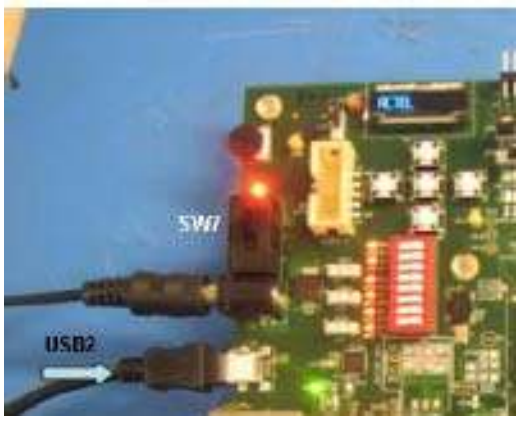

Figure 2-9 • **Connecting the USB and 9 V Power Supplies on the M1AFS-ADV-DEV-KIT Board**

3. Set the DIP switch at S1 to the default configuration of [8:1] = 01011001.

Note: These switches are wired to inputs of the FPGA so that open will correspond to logic 1 (4.6 k pull-up to 3.3 V) and closed will correspond to logic 0 GND.

4. Determine the COM port assigned to the USB interface. Open the Windows Control Panel and double-click the **System** icon. Click the **Hardware** tab and click the **Device Manager** button. Expand the **Ports (Com & LPT)** item in the Device Manager. Look for the CP2102 USB to UART Bridge Controller in the list of ports. The COM port in parentheses identifies the COM port assigned to this device (Figure 2-10). If you do not see CP2102, you need to install the CP210x_Drivers driver. Refer to "Installing the M1AFS-ADV-DEV-KIT Board USB Serial Driver" section on page B-31 for more information.

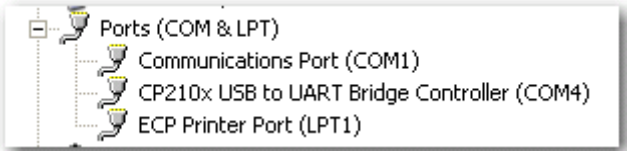

Figure 2-10 • **Determining the USB Serial Port's COM Port**

5. Open HyperTerminal and set the communications parameters as shown below. Set the COM port to match the USB serial port of the board, as shown in Step 4.
   - 115,200 bits per second
   - 8 data bit
   - Parity set to none
   - 1 stop bit
   - Flow control set to none

Running the Demonstration Design in Auto Mode

1. Turn the power switch on the board, SW7, to the ON position. Once initialized, HyperTerminal will display the following:

```
Core1553BRM 1L02
```

   - 1 indicates BRM core 1 is configured as the bus controller.
   - L indicates that bus loopback is enabled.

– 02 indicates the remote terminal address is set to 2. If the display shows other than 1L02, check the DIP switch settings.

Interrupt status messages will begin scrolling across the terminal window:

```
2.80E4.0400.4A00
1.0018.0002
2.8008.0400.4A00
2.8004.0400.1200
2.80E4.0400.4A00
1.0018.0002
2.8008.0400.4A00
2.8004.0400.2200
2.80E4.0400.4A00
1.0018.0002
2.8008.0400.4A00
2.8004.0400.3200
:
```

Monitoring 1553B Message Traffic Using Silicon Explorer II

At this point, the demonstration design will begin passing 1553B messages between the two Core1553BRM cores. You can monitor the message traffic using Silicon Explorer II or any logic analyzer. The next section will describes monitoring 1553B message using Silicon Explorer II, but you can follow the similar steps when using the logic analyzer.

To monitor message traffic:

1. If you do not have the latest version of Silicon Explorer, download the software from the Actel website (www.actel.com/download/program_debug/se/default.aspx) and install it.
2. Connect Silicon Explorer II to your PC using a serial cable.
3. Connect the 22-pin cable supplied with Silicon Explorer II (for 18 channels, a clock, V_{CC}, GND, and clock GND) to the Silicon Explorer II hardware, and connect the first 4 channels to the pins in the J5 connector (Table 2-3 and Figure 2-11).

Table 2-3 • **Silicon Explorer II Connections to M1AFS-ADV-DEV-KIT**

Silicon Explorer II Lead	M1AFS-ADV-DEV-KIT Board	Signal
CH0	Pin 1 (top) on J5	Bus A
CH1	Pin 3 on J5	Bus B
CH2	Pin 5 on J5	MSGINT
GND	Pin 7 on J5	GND

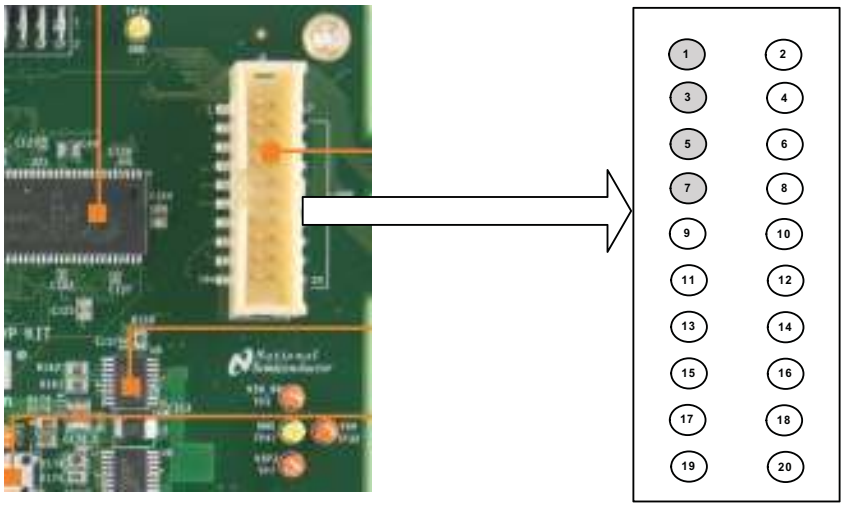

Figure 2-11 • **J5 Connector on M1AFS-ADV-DEV-KIT Board**

4. Power up Silicon Explorer and start the Silicon Explorer software. In the Silicon Explorer software, set Silicon Explorer to sample at 33 MHz, Center (50/50%), and trigger on falling edge on Ch2. Click the falling edge icon under column P1 next to Channel 2 or MSGINT if you named the channels (Figure 2-12).

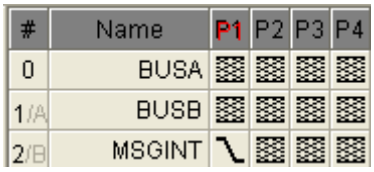

Figure 2-12 • **Trigger on Falling Edge on Channel 2**

Note: To gain more area for viewing signals, from the **View** menu, uncheck **Probe Window**.

5. Press the **RSTN** button on the board, then click the **acquire** icon from the Silicon Explorer software. You should see Bus Activity on Bus A (Figure 2-13).

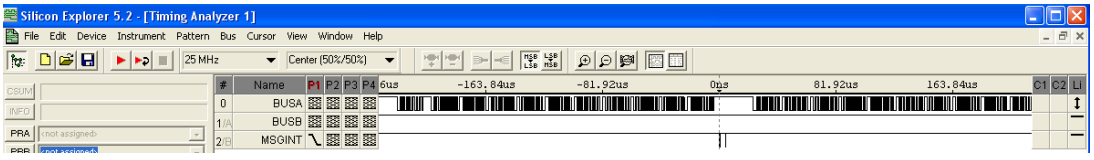

Figure 2-13 • **Bus Activity**

Interrupt Status Messages

Core1553BRM will generate status messages of the format `N.IAW.IIW.MIW` on HyperTerminal:

- N: Indicates which BRM generates the interrupt
- AW: Interrupt Address Word
- IIW: Interrupt Identification Word
- MIW: Message Information Word (RT interrupts only)

These messages will be displayed on the RS-232 interface to HyperTerminal. Refer to the *Core1553BRM Handbook* for more information about these messages.

Interpreting Interrupt Status Messages

The meaning of each of the first four interrupt messages is given below:

`2.80E4.0400.4A00`

- 2.80e4: IAW = RT SA25 RX
- 0400: IIW = Sub address accessed
- 4A00 : 9 words bus A
- 1.0018: IAW = BC MSG Block 3
- 0002: IIW = CBA interrupt

`2.8008.0400.4A00`

- 2.8008: IAW = RT SA 2 RX
- 0400: IIW = Sub address accessed
- 4A00: 9 words bus A

`2.8004.0400.1200`

- 2.8004: IAW = RT SA1 RX
- 0400: IIW = Sub address accessed
- 1200: 2 words bus A

This pattern repeats, with the word count increasing on the third message. Refer to the *Interrupts* section of the *Core1553BRM Handbook* for more information.

Subaddresses

Subaddressing enables designers to create custom bus control or system functions within MIL-STD-1553B standard. The Core1553BRM demonstration design makes use of custom subaddresses to control the operation of the remote terminal (Table 2-4).

Table 2-4 • **Core1553BRM Demonstration Design Subaddressing**

Subaddress	Function
25	RT receive disabled. RT sends data.
26	RT transmit disabled. Received data sent to the UART.
27	Both RT receive and transmit disabled
30	Loopback subaddress

3 – Modifying the Demonstration Design Through Script

Core1553BRM Verification Testbench

Actel has developed a Core1553BRM verification testbench to verify the core performance per the MIL-STD-1553B specification. The testbench is coded in VHDL and includes several Core1553BRM cores connected to a 1553 bus and backend interfaces. A procedural testbench controls the various blocks and implements various test protocols.

The Core1553BRM verification testbench uses a command interpreter to apply high-level stimulus to Core1553BRM. This allows you to directly set the Core1553BRM memory and registers through command files and thus control operation of the core. You can create the script file using Core1553BRM verification testbench and then apply it to the Core1553 development system. Refer to the *Core1553BRM Handbook* for more information.

Scripting

High-level command files created to control the core operation can be converted into log files by the verification testbench. These log files can then be downloaded to the Core1553BRM demonstration design to change its operation and test various scenarios. The demonstration CD contains two files in the release\scripts\ directory: demo.txt and demo_log.txt. Demo_log.txt was generated by the verification testbench from the command file demo.txt.

The demo_log.txt script programs one BRM as the BC and the other as RT 1, initializes the RT memory tables, and sets up the BC to do BC-to-RT, RT-to-BC, and RT transmit vector commands. At the conclusion of the script, BC memory values are compared to verify that the three messages completed correctly. Demo.txt is fully annotated and shows the exact sequences of operations used to generate the script file. Demo_log.txt is used to verify the operation of the demonstration design.

A – Programming the Fusion FPGA on M1AFS-ADV-DEV-KIT

Follow these steps to program a design into the Fusion FPGA.

1. Connect the J1 pins on the Actel M1AFS-ADV-DEV-KIT board to the Actel low-cost programming stick (Figure A-1).

Figure A-1 • **Connect J1 Pins on M1AFS-ADV-DEV-KIT Board**

2. Connect one end of the USB mini B cable to the Actel programming stick and the other end to the PC.
3. Connect one end of a 9 V power supply to the power input (Power1) on the M1AFS-ADV-DEV-KIT board. Plug the supply into an electrical outlet.

   Once the LCPS is recognized, the yellow ON LED will be solidly lit. If the PC prompts for the location of the FlashPro3 drivers, browse to the FlashPro software installation folder <FlashPro_Install_Loacation>/Drivers. Use the fp3b-cyusb.inf file if available (or fp3bload.inf if not).
4. Launch the Actel FlashPro programming software. When using the FlashPro programming software, the programmer selects FlashPro3. The programming stick is functionally equivalent to a FlashPro programmer, but designed specifically for use with this Fusion Embedded Development Kit.
5. Click the **New Project** button to create a new project. Set a user define project name and location.
6. Click the **Configure Device** button.
7. In the **Device Configuration** window, browse and select the programming database (PDB) file or STAPL (STP) file.
8. Once the programming database file is loaded, click the **PROGRAM** button to start programming the Fusion FPGA. After successful programming, the programmer will show the RUN PASSED message.
9. When the programming successfully completes, remove the LCPS, and press the system reset button, **RSTN**, on the M1AFS-ADV-DEV-KIT to reset the system.
10. Verify that your design is working.

B – Communication from HyperTerminal to M1AFS-ADV-DEV-KIT

The M1AFS-ADV-DEV-KIT board does not have a standard serial interface. Instead, it has a USB-to-UART interface with ESD protection. You will need to install the M1AFS-ADV-DEV-KIT board USB serial driver, which enables the PC to communicate with the FPGA in M1AFS-ADV-DEV-KIT board through the USB-to-UART bridge controller.

The USB-to-UART bridge controller (U6) provides a standard UART connection with the Fusion FPGA. Any standard UART controller can be implemented in the Fusion FPGA to allow access with this interface. Figure B-1 shows the USB-to-UART interface schematic on the M1AFS-ADV-DEV-KIT board.

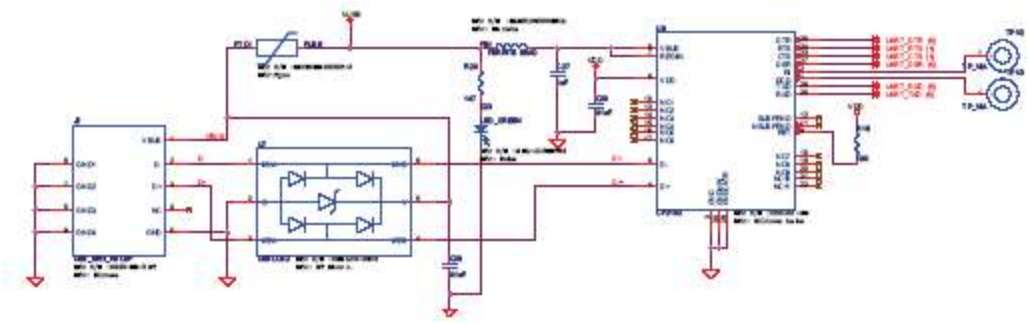

Figure B-1 • **USB-to-UART Interface Schematic**

With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the Fusion FPGA device. For more information about the USB-to-UART bridge and device drivers, refer to the Fusion Embedded Development Kit page:
www.actel.com/products/hardware/devkits_boards/fusion_embedded.aspx.

Installing the M1AFS-ADV-DEV-KIT Board USB Serial Driver

1. Use WinZip to extract all files stored in the CP210x_Drivers.zip archive.
2. Double-click **CP210x_Drivers.exe**.
3. Choose the **Install** option in the Install Wizard and select **Yes** for the licensing agreement.
4. Restart your computer on which the driver was installed.

C – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
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From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
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Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. The Technical Support numbers are:

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800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

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