Data Sheet

32

V850E/Dx3 - DJ3/DL3

32-bit Single-Chip Microcontroller

μPD70F3421
μPD70F3422
μPD70F3423
μPD70F3424
μPD70F3425
μPD70F3426A
μPD70F3427

Renesas Electronics
www.renesas.com

R01DS0049ED0210, Rev. 2.10
Jun 1, 2011

Table of Contents

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

1. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

2. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

3. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

4. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

5. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

6. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics.

The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

“Standard”:	Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
“High Quality”:	Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
“Specific”:	Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

7. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
8. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
9. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
10. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
11. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1)	“Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
(Note 2)	“Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   – The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Chapter 1 Overview

The V850E/Dx3 - DJ3/DL3 is a product in Renesas Electronics V850 family of single-chip microcontrollers designed for Automotive applications.

1.1 General

The V850E/Dx3 - DJ3/DL3 single-chip microcontroller is a member of Renesas Electronics V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.

The V850E/Dx3 - DJ3/DL3 provides an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), Timers and measurement inputs (A/D converter), with dedicated CAN network support. Control and driver for 6 stepper motors are included.

The device offers power-saving modes to manage the power consumption effectively under varying conditions.

Thus equipped, the V850E/Dx3 - DJ3/DL3 is ideally suited for automotive applications, like dashboard or body. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

This specification covers the following devices of the family:

Family Code	Product Code	Internal Flash	Internal RAM	LCD Control	Other Peripherals
DL3	µPD70F3427GD(A)-LML-QS-AX	1024 KB	60 KB	LCD I/F	Full set + ext. Mem I/F
DJ3	µPD70F3426AGJ(A)-GAE-QS-AX	2048 KB	84 KB	LCD I/F	Full set
DJ3	µPD70F3425GJ(A)-GAE-QS-AX	1024 KB	32 KB	LCD I/F	Full set
DJ3	µPD70F3424GJ(A)-GAE-QS-AX	512 KB	24 KB	LCD I/F	Full set
DJ3	µPD70F3423GJ(A)-GAE-QS-AX	512 KB	20 KB	LCD I/F, LCD C/D	Reduced set
DJ3	µPD70F3422GJ(A)-GAE-QS-AX	384 KB	20 KB	LCD I/F, LCD C/D	Reduced set
DJ3	µPD70F3421GJ(A)-GAE-QS-AX	256 KB	12 KB	LCD I/F, LCD C/D	Reduced set

The following table gives a more detailed overview of the different derivates and their major features.

Series name		V850E/DL3	V850E/DJ3					
Part Number		uDP70F3427	uDP70F3426A	uDP70F3425	uDP70F3424	uDP70F3423	uDP70F3422	uPD70F3421
Technology		MF2 (Flash)						
Internal memory	Flash	1 MB	2 MB [a]	1 MB	512 KB		384 KB	256 KB
	RAM	60 KB	84 KB[b]	32 KB	24 KB	20 KB	20 KB	12 KB
DMA		4 ch						
Operating Clock	Main (internal)	64 MHz typ.				32 MHz typ.		
	Ring-OSC	240 kHz typ.						
	Subclock	32 kHz typ.						
I/O ports		101	98					
Input ports		16						
A/D converter		16 ch				12 ch		
Timers	TMY	1 ch						
	TMZ	10 ch				6 ch		
	TMP	4 ch						
	TMG	3 ch						
	WDT	provided						
	Watch	provided						
	Watch calibration	provided						
Serial interfaces	AFCAN	3 ch	2 ch	3 ch				
	UARTA	2 ch						
Serial interfaces	CSIB	3 ch				2 ch		
	IIC	2 ch						
Interrupts	External	8				7		
	Internal	95				76		
	NMI	2 ch						

Series name		V850E/DL3	V850E/DJ3					
Part Number		uDP70F3427	uDP70F3426A	uDP70F3425	uDP70F3424	uDP70F3423	uDP70F3422	uPD70F3421
Other functions	ROM correction	8ch (DBTRAP)						
	POC	Provided						
	Voltage comparator	2 ch						
	Clock supervision	Provided						
	Sound generator	1 ch						
	Stepper motor C/D	6 ch						
	LCD C/D	none				40 x 4		
	LCD I/F	Provided						
	Auxilliary frequency output	Provided						
	On-Chip debug	Provided						
	External Mem I/F	Provided	none					
Operating voltage		3.2v to 5.5V for core functions, ADC and StepperMotor C/D, 3.0V to 5.5V for all other I/O Full operation in range from 4.0V to 5.5V due to POC function (*8.2 on page 81*)						
Package		208-pin QFP	144-pin QFP					

a) For the DJ3 derivative µPD70F3426A, the upper 1MB of the flash memory is connected to the internal system bus (VSB). In case of performing consecutive accesses to that part of the flash-memory, a 32-bit data access requires two cycles.
In case a random access is applied to that part of the flash-memory, this access requires four cycles.

b) For the DJ3 derivative µPD70F3426A, the upper 24kB of the internal RAM is connected to the internal system bus (VSB). In case of performing consecutive accesses to that part of the internal RAM, a 32-bit data access requires two cycles.
In case a random access is applied to that part of the internal RAM area that access requires two cycles.

Chapter 2 Pinout Information

2.1 Pin configuration µPD70F3427

- µPD70F3427GD

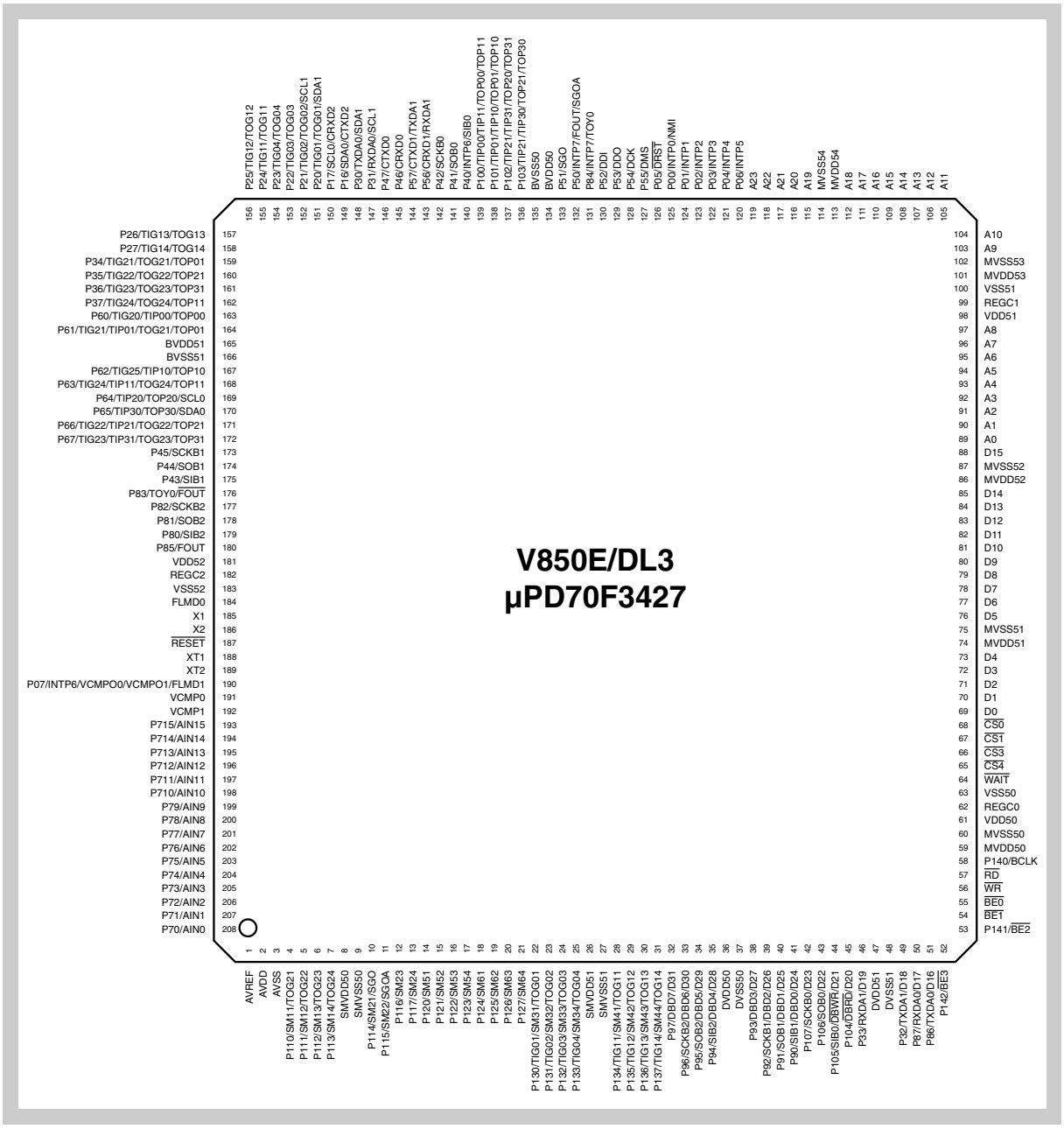


Figure 2-1 Pin Configuration µPD70F3427

2.2 Pin configuration µPD70F3426A, µPD70F3425, µPD70F3424

- µPD70F3426AGJ
- µPD70F3425GJ
- µPD70F3424GJ

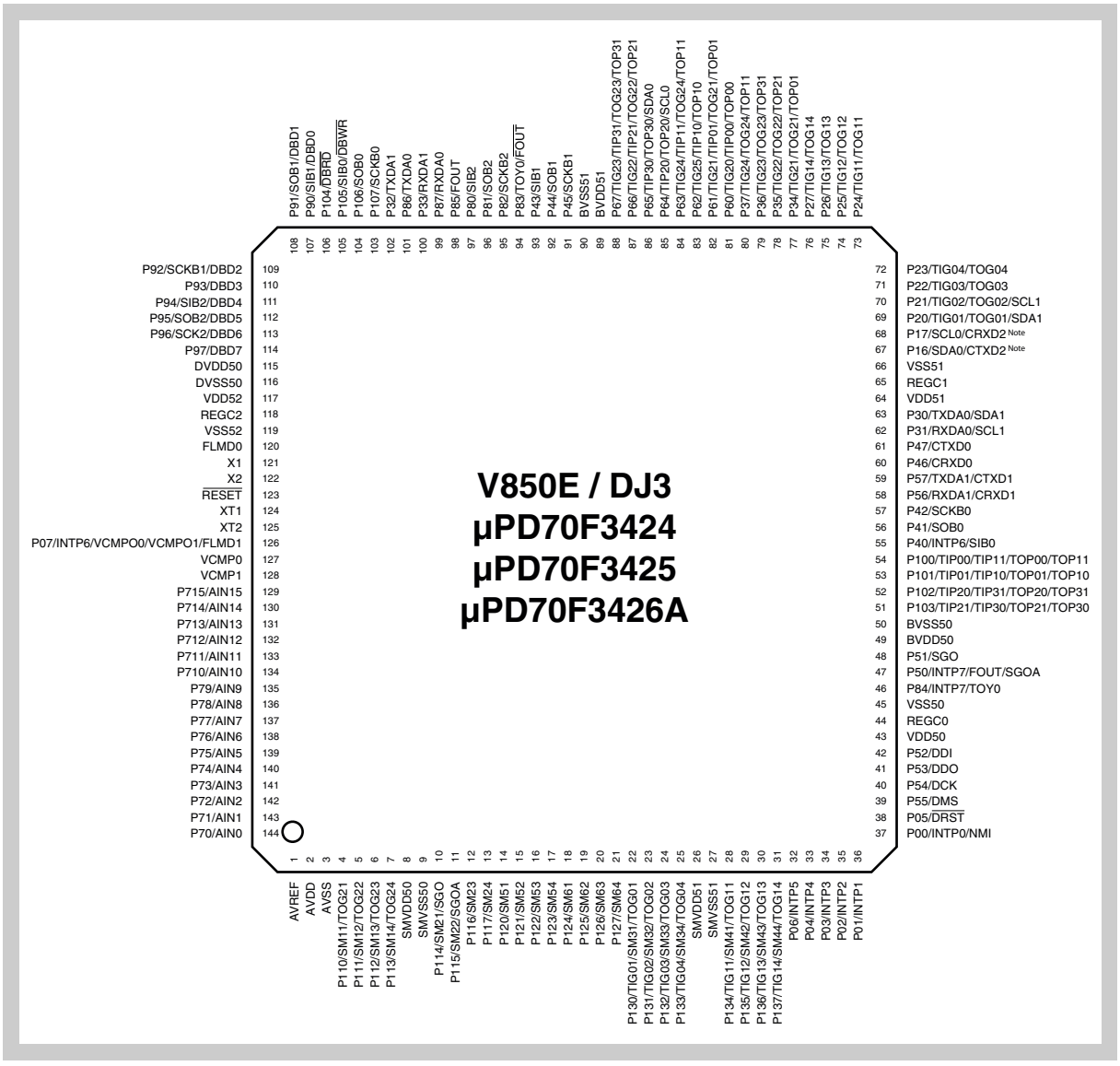


Figure 2-2 Pin Configuration µPD70F3426A, µPD70F3425, µPD70F3424

Note CRXD2, CTXD2 not available on µPD70F3426A.

2.3 Pin configuration µPD70F3423, µPD70F3422, µPD70F3421

- µPD70F3423GJ
- µPD70F3422GJ
- µPD70F3421GJ

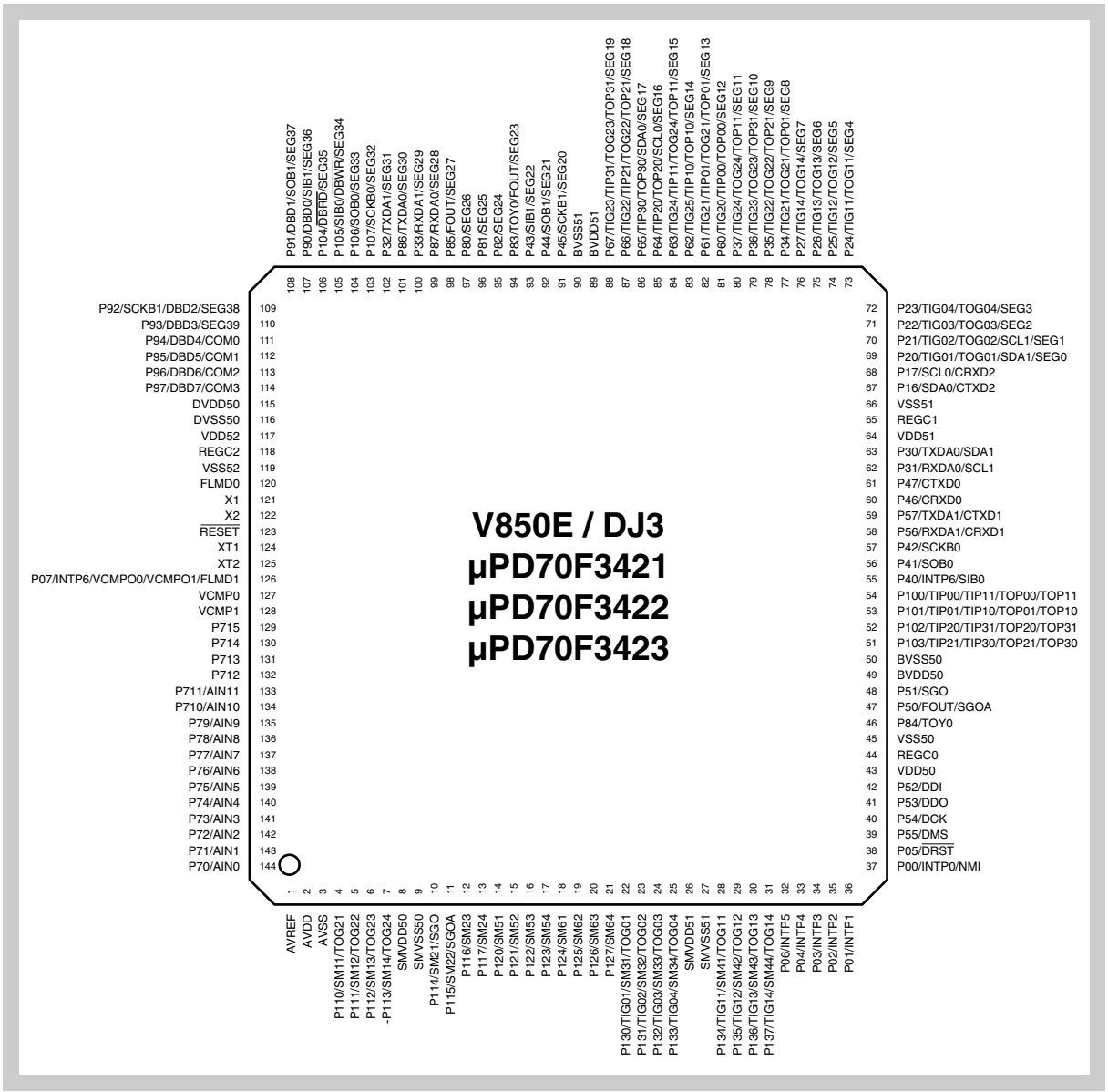


Figure 2-3 Pin Configuration µPD70F3423, µPD70F3422, µPD70F3421

2.4 Pin Group information

- Pin Groups 1x: Pins supplied by BV_{DD5}[Note1]
  1A: (P00-06, P50-55, P84)
  1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
  1C: (P20-27, P34-37, P60-67)
  1D: (P43-45, P80-83, P85)
- Pin Groups 1x: Pins supplied by BV_{DD5}[Note2]
  1A: (P00-06, P50-55, P84)
  1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
  1C: (P20-27, P34-37, P60-61)
  1D: (P62-67, P43-45, P80-83, P85)
- Pin Group 2: Pins supplied by V_{DD5}
  2: ($\overline{\text{RESET}}$, FLMD0, P07)
- Pin Group 3[Note1]: GPIO and LCD Bus interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107)
- Pin Group 3[Note2]: GPIO and LCD Bus and external memory interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107, P141-142)
  3A: (P94-97)
  3B: (P90-93)
  3C: (P33, P104-107)
  3D: (P32, P86-87, P141-142)
- Pin Group 4: Stepper Motor outputs supplied by SMV_{DD5}
  4A: (P110-117, P120-123)
  4B: (P124-127, P130-137)
- Pin Group 5: ADC Inputs supplied by AV_{DD}
  5: (P70…P715)
- Pin Group 6[Note2]: External memory Interface supplied by MV_{DD5}
  6: (A0-23, D0-15, $\overline{\text{CS}}$0-1, $\overline{\text{CS}}$3-4, $\overline{\text{WAIT}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BE}}$0-1, P140)
  6A: ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BE}}$0-1 , P140)
  6B: ($\overline{\text{CS}}$0-1, $\overline{\text{CS}}$3-4 , $\overline{\text{WAIT}}$)
  6C: (D0-4)
  6D: (D5-9)
  6E: (D10-14)
  6F: (D15, A0-3)
  6G: (A4-18)
  6H: (A9-13)
  6I: (A14-18)
  6J: (A19-23)
- Pin Group 8: Voltage Comparator Inputs supplied by AV_{DD}
  8: (VCMP0-1)

Note 1. µPD70F3426A, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD70F3421

2. µPD70F3427

Chapter 3 Absolute Maximum Ratings

Condition 1: T_A = -40°C ~ +85°C,

Operation Modes: RUN, HALT, IDLE

Power dissipation: < 1.3W (μPD70F3427)

< 1.2W (μPD70F3426A, μPD70F3425, μPD70F3424)

< 1.0W (μPD70F3423, μPD70F3422, μPD70F3421)

Duration: 15000 hours

V_{SS5} = 0V

Condition 2: T_A = -40°C ~ +85°C,

Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation

Power dissipation: < 0.5W

Duration: 15 years

V_{SS5} = 0V

Table 3-1 Absolute maximum ratings

Parameter		Symbol	Test Conditions	Ratings [a]	Unit
Supply voltage		V_{DD5}		-0.5 ~ +6.5	V
		AV_{DD}		-0.5 ~ +6.5	V
		AV_{REF}		-0.5 ~ +6.5	V
		BV_{DD5}		-0.5 ~ +6.5	V
		DV_{DD5}		-0.5 ~ +6.5	V
		SMV_{DD5}		-0.5 ~ +6.5	V
		MV_{DD5} [b]		-0.5 ~ +6.5	V
		AV_{SS}		-0.5 ~ +0.5	V
		BV_{SS5}		-0.5 ~ +0.5	V
		DV_{SS5}		-0.5 ~ +0.5	V
		SMV_{SS5}		-0.5 ~ +0.5	V
		MV_{SS5} [b]		-0.5 ~ +0.5	V
Input voltage	Group 1	V_{I1}	$V_{I1} < BV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 2	V_{I2}	$V_{I2} < V_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 3	V_{I3}	$V_{I3} < DV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 4	V_{I4}	$V_{I4} < SMV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 5, 8 AVREF	V_{IA}	$V_{IA} < AV_{DD} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 6 [b]	V_{I6}	$V_{IM} < MV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
Special [c]	X1, X2, XT1, XT2, REGC0-2	V_{IS}		-0.5 ~ + 3.6	V

Table 3-1 Absolute maximum ratings (Continued)

Parameter	Symbol	Test Conditions	Ratings [a]	Unit
Output voltage	V_O		-0.5 ~ +6.5	V
Operating temperature (ambient)	T_{OPR}		-40 ~ +85	°C
Storage temperature	T_{STGB}		-40 ~ +150	°C

a) Currents are average current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.
b) xxx µPD70F3427 only
c) These pins are for special use only and should not be used for other connections than specified. Pins operate with the internal generated core voltage.

Note Refer to *"Pinout Information" on page 9* for pin to group association.

- V_{DD5} is the supply voltage for the internal voltage regulators applied to pins V_{DD5x}.
- V_{SS5} is the ground for the internal logic applied to pins V_{SS5x}.
- A_{VDD} is the supply for analog part of the A/D converter.
- A_{VSS} is the ground for the analog part of the A/D converter.
- BV_{DD5} is the supply voltage for the I/O buffers applied to pins BV_{DD5x}.
- BV_{SS5} is the ground for the I/O buffers applied to pins BV_{SS5x}.
- DV_{DD5} is the supply voltage for the I/O buffers that support the LCD bus I/F applied to pins DV_{DD5x}.
- DV_{SS5} is the ground for the I/O buffers that support the LCD bus I/F applied to pins DV_{SS5x}.
- SMV_{DD5} is the supply voltage for the I/O buffers of the stepper motor drivers applied to pins SMV_{DD5x}.
- SMV_{SS5} is the ground for the I/O buffers of the stepper motor drivers applied to pins SMV_{SS5x}.
- µPD70F3427 only:
- MV_{DD5} is the supply voltage for the I/O buffers of the external memory interface applied to pins MV_{DD5x}.
- MV_{SS5} is the ground for the I/O buffers of the external memory interface applied to pins MV_{SS5x}.

Table 3-2 Absolute maximum ratings currents

Parameter		Symbol	Test Conditions	Ratings average [a]	Ratings peak [b]	Unit
Output current low	1 pin	I_{OL1}	Groups 1A, 1B, 1C, 1D	30	50	mA
	All pins	I_{OLA1A}	Group 1A	50	100	mA
	All pins	I_{OLA1B}	Group 1B	50	100	mA
	All pins	$I_{OLA1SAB}$	Sum of Groups 1A, 1B	100	200	mA
	All pins	I_{OLA1C}	Group 1C	50	100	mA
	All pins	I_{OLA1D}	Group 1D	50	100	mA
	All pins	$I_{OLA1SCD}$	Sum of Groups 1C, 1D	100	200	mA
	1 pin	I_{OL3}	Group 3 [c]	30	50	mA
	All pins	I_{OLA3}		50	100	mA
	1 pin	I_{OL3}	Groups 3A, 3B, 3C, 3D [d]	30	50	mA
	All pins	I_{OLA3}		50	100	mA
	All pins	$I_{OLA3SAB}$	Sum of Groups 3A, 3B [d]	100	200	mA
	All pins	$I_{OLA3SCD}$	Sum of Groups 3C, 3D [d]	100	200	mA
	1 pin	I_{OL4A}	Group 4A	45	55	mA
	All pins	I_{OLA4A}		200	270	mA
	1 pin	I_{OL4B}	Group 4B	45	55	mA
	All pins	I_{OLA4B}		200	270	mA
	All pins	I_{OL5}	Group 5 [e]	32	32	
	1 pin	I_{OL6}	Group 6 [d]	30	50	mA
	All pins	I_{OLA6}		70	300	mA
	All pins	I_{OL8}	Group 8 [e]	4	4	mA
Output current high	1 pin	I_{OH1}	Groups 1A, 1B, 1C, 1D	-30	-50	mA
	All pins	I_{OHA1A}	Group 1A	-50	-100	mA
	All pins	I_{OHA1B}	Group 1B	-50	-100	mA
	All pins	$I_{OHA1SAB}$	Sum of Groups 1A, 1B	-100	-200	mA
	All pins	I_{OHA1C}	Group 1C	-50	-100	mA
	All pins	I_{OHA1D}	Group 1D	-50	-100	mA
	All pins	$I_{OHA1SCD}$	Sum of Groups 1C, 1D	-100	-200	mA
	1 pin	I_{OH3}	Group 3 [c]	-30	-50	mA
	All pins	I_{OHA3}		-50	-100	mA
	1 pin	I_{OH3}	Groups 3A, 3B, 3C, 3D [d]	-30	-50	mA
	All pins	I_{OHA3}		-50	-100	mA
	All pins	$I_{OHA3SAB}$	Sum of Groups 3A, 3B [d]	-100	-200	mA
	All pins	$I_{OHA3SCD}$	Sum of Groups 3C, 3D [d]	-100	-200	mA
	1 pin	I_{OH4A}	Group 4A	-45	-55	mA
	All pins	I_{OHA4A}		-200	-270	mA
	1 pin	I_{OH4B}	Group 4B	-45	-55	mA
	All pins	I_{OHA4B}		-200	-270	mA

Table 3-2 Absolute maximum ratings currents (Continued)

Parameter		Symbol	Test Conditions	Ratings average [a]	Ratings peak [b]	Unit
Output current high	All pins	I_{OH5}	Group 5 [e]	-32	-32	mA
	1 pin	I_{OH6}	Group 6 [d]	-30	-50	mA
	All pins	I_{OHA6}		-70	-300	mA
	All pins	I_{OH8}	Group 8 [e]	-4	-4	mA

a) Average currents are average current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.
b) The peak current sets the limit for short term current flows.
c) µPD70F3426A, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD70F3421
d) µPD70F3427 only
e) Group 5 and group 8 have no output capability. This value is needed as reference, because injected current can influence the device in the same way as an output stage.
Injected currents that may flow through any or both input pins of the Voltage-Comparators VCMP0, VCMP1 are included within the given parameter.

Table 3-3 Power Supply Restrictions

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply voltage up/ down ramp [a]	V_{DDRAMP}		≤ 50	V/ms
Low voltage duration [b]	$t_{VDD5Low}$	V_{DD5} < 3.2V, AV_{DD5} < 3.2V, SMV_{DD5} < 3.2V, DV_{DD5} < 3.0V, BV_{DD5} < 3.0V, MV_{DD5} < 3.0V [c]	indefinite	s

a) Not tested in production
b) No device damage and no flash data loss.
c) (µPD70F3427).

Note 1. A low resistive connection of all VSS pins on the PCB has to be ensured. This specification denotes this as:
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5}$ (µPD70F3427) = 0 V

2. A low resistive connection of all V_{DD5x} pins among each other has to be ensured.

Chapter 4 General Characteristics

4.1 Requirements for external connections

A low resistive connection of all VSS pins on the PCB has to be ensured.
In the following this specification denotes this as:

$$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = MV_{SS5}\ ^{Note} = AV_{SS} = 0\ V$$

A low resistive connection of the following supply pins hast to be ensured:

- all V_{DD5x} pins among each other
- all BV_{DD5x} pins among each other
- all SMV_{DD5x} pins among each other
- all DV_{DD5x} pins among each other
- all MV_{DD5x} pins among each other **Note**

Note µPD70F3427 only

4.2 Capacitance connected to REGCx

The device requires to connect capacitors with the following parameters to each of the pins REGC0, REGC1 and REGC2 individually.

The pins REGC0, REGC1, REGC2 must not be connected externally.

Table 4-1 External Capacitance Requirement

Parameter	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Capacitance	C_{REG}		3.3	4.7	10	µF
ESR of capacitance	C_{ESR}	F0 = 100kHz			0.6	Ω

4.3 Main Oscillator Characteristics

Conditions

T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5}$ (µPD70F3427 only) = 0 V

A ceramic or crystal resonator has to be connected to the main clock input pins as shown in *Figure 4-1*.

Note

1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. Values of C_1, C_2 and R depend on the used crystal or resonator and must be specified in cooperation with crystal/resonator manufacturer.

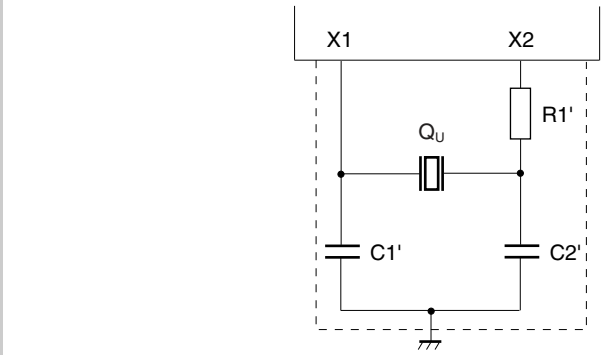


Figure 4-1 Recommended Main Oscillator Circuit

Caution

1. External clock input is prohibited.
2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with the other signal lines.
   - Do not route the wiring near a signal line through which a high fluctuating current flows.
   - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
   - Do not ground the capacitor to a ground pattern through which a high current flows.
   - Do not fetch signals from the oscillator.

Table 4-2 Main Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			16 [a]	ms
X1, X2 Oscillator Frequency	f_{OSC}		3.6	4.0	4.4	MHz

a) T_{OST} depends on the external crystal. Value might be improved after evaluation

Remark These values are valid only for crystal operation.

Table 4-3 Main Oscillator Characteristics - Crystal Type NDK LN-G8-1404

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			10 [a]	ms
X1, X2 Oscillator Frequency	f_{OSC}		3.6	4.0	4.4	MHz

a) The given oscillation stabilization time is valid exclusively in case the below mentioned crystal-type from the manufacturer NDK is used for the main-oscillator operation. Beside the application of this specific crystal type, the PCB-design and capacitance configuration must ensure proper operation of the crystal enbling a load capacitance of about C_L=12 pF. This parameter has to be verified by a dedicated crystal-evaluation based on the final PCB.

NDK Spec. No.: LN-G8-1404
Holder: AT-51GW
Frequency: 4.000 MHz

4.4 Sub-Oscillator Characteristics

Conditions

T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

A crystal resonator has to be connected to the sub clock input pins as shown in *Figure 4-2*.

Note

1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. Values of C_{S1}, C_{S2} and R_S depend on the used crystal and must be specified in cooperation with crystal manufacturer.

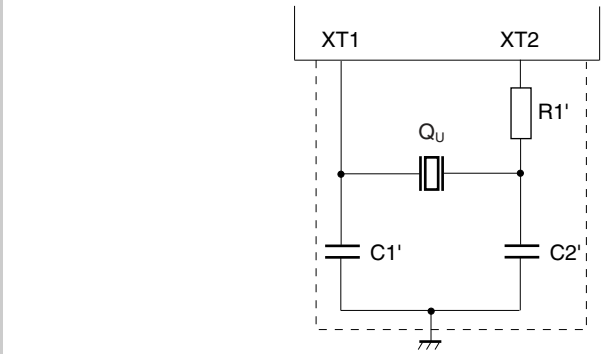


Figure 4-2 Recommended Sub Oscillator Circuit

Caution

1. External clock input is prohibited.
2. When using the sub system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with the other signal lines.
   - Do not route the wiring near a signal line through which a high fluctuating current flows.
   - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
   - Do not ground the capacitor to a ground pattern through which a high current flows.
   - Do not fetch signals from the oscillator.

Table 4-4 Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
XT1,XT2 Oscillator Frequency	f_{SOSC}		32	32.768	35	KHz
Sub oscillator stabilization time	T_{SOST}				5 [a]	s

a) T_{SOST} depends on the external crystal. Value might be improved after evaluation

Remark These values are valid only for crystal operation.

4.5 Peripheral PLL Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 4-5 Peripheral PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL Startup Time	T_{PST}	OSC MODE			1.2	ms
PLL Output period jitter [a]	T_{PJ}	Peak to peak			1	ns
PLL Long term jitter [a]	T_{LJ}	Time = 20µs			2	ns

a) Not tested in production. Specified by design.

4.6 Spread Spectrum PLL Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 4-6 Spread Spectrum PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SSCG Startup Time	T_{SSCGST}	OSC MODE			1.2	ms
SSCG Frequency modulation range [a]	DITHER	OSC MODE, dither setting: 3%	0		±4.2	%
		OSC MODE, dither setting: 5%			±6.8	%
SSCG center frequency during dithering [a]	f_{DITHER}			1.0 * $f_{nominal}$		
SSCG modulation frequency [a]	f_{Mod}	SCFMC1-0 = [b] 00 01 10	 35 41 49	 40 50 60	 46 55 63	kHz

a) Not tested in production. Specified by design.
b) The typical modulation frequency can be selected by register SCFMC.

4.7 Ring Oscillator Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 4-7 Ring Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
Ring Oscillator Frequency	f_{RING}		200	240	300	KHz
Ring oscillator Stabilization Time [a]	T_{ROST}				20	µs

a) Not tested in production. Specified by design.

4.8 I/O Capacitances

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 4-8 I/O Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Input/output capacitance, all I/O pins except group 4	C_{IO}				15	pF
Input/output capacitance Group 4	C_{IO4}				30	pF

Chapter 5 Operation Conditions

5.1 CPU Clock

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 5-1 CPU Clock Frequencies

Clock Mode	Prescale	Operation Mode	Device	CPU Operation Clock Frequency [MHz]
OSC mode	n/a	all modes	all	4
OSC mode, PLL x8	1/2			16
OSC mode, PLL x8	n/a			32
OSC mode, SSCG x12	1/6			8
OSC mode, SSCG x16	1/4			16
OSC mode, SSCG x12	1/2			24
OSC mode, SSCG x16	1/2			32
OSC mode, SSCG x12	1/1		µPD70F3427, µPD70F3426A, µPD70F3425, µPD70F3424	48
OSC mode, SSCG x16	1/1			64
OSC mode, Ring OSC	n/a		all	0.2
OSC mode, Sub OSC	n/a			0.032

5.2 Peripheral Clock

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 5-2 Peripheral Clock Frequencies

Clock	Clock Source	Max	Unit
PCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x 8	16, 8	MHz
PCLK2 - 15	Main OSC	4, 2, ... , 1/2048	MHz
IICLK	Main OSC	4	MHz
	Main OSC, PLL x8	32[a]	MHz
	Main OSC, SSCG		
SPCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x8	16, 8[b]	MHz
	Main OSC, SSCG		
SPCLK2 - 15	Main OSC	4, 2 ... 1/2048	MHz
	Main OSC, SSCG		
FOUT (CLKOUT)	Main OSC, PLL x8	32	MHz
	Main OSC, SSCG	32[c]	MHz
	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
LCDCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WDTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WCTCLK	Main OSC	4	MHz
	PCLK1	see PCLK1	MHz

a) needs to be ensured by proper configuration of the IICLK divider.
b) needs to be ensured by proper configuration of the SPCLK divider.
c) needs to be ensured by proper configuration of the FOUT (CLKOUT) divider.

5.3 AC Load Condition - Single Pin Switching

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = (µPD70F3427 only) = 0 V

Note Full device operation is only available, when the supply voltage V_{DD5} is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage dropps below the given max threshold voltage. Refer to *"Power On Clear" on page 81*.on page 95 for further details.

5.3.1 Output Pins - Single Pin Switching

Note
1. Not tested in production. Specified by design.
2. Special care must be taken for the power supply when high capacitive loads are switched. The buffers change from limited to unlimited mode when the output voltage is near to the supply or ground. At that time a current peak is driven to the load thus drawing a peak current on the supply. This will generate noise and may deteriorate the observed slopes at neighbor pins in the same pin group, when they switch at the same time.

Table 5-3 AC Load Condition - Single Pin Switching

Parameter	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Capacitive load per pin (Single pin)[a]	1, 2[b], 3, 4, 6[c]	C_{LS}	f_{switch} < 100 kHz			1	nF
Capacitive load per pin (Multiple pins)[d]		C_{LM}	f_{switch} < 1 MHz			300	pF

a) The specified parameter does represent the maximum capacitive load one pin of one pin group is able to drive in case only that single pin is driving the specified capacitive load by switching its output level.
In case more than one pin within one pin group need to drive that capacitive load dynamically they must be switched consecutively. Do not switch more than one port-pin at a given time.
The given specification is valid for the condition the concerned pin is operating in Limit2 drive-strength-control-mode (5mA. Except Pin Group 4).

b) The condition is only valid for pin P07 of pin group 2.

c) Pin group 6 exists for the derivative µPD70F3427 only.

d) Multiple pins may switch simultanously.

5.3.2 Input Pins - Capacitive Loading

Note The maximum capacitive load that is allowed to be applied to a single ADC-Input channel, a voltage comparator input or a single port-input can be derived by examining the given parameters of:

- Injected Current
- Supply Voltage ramp down (refer to *“Power Supply Restrictions“ on page 16*)
- Absolute Maximum Ratings

Caution When determining the maximum capacitive load according to the given parameters mentioned above, it must be secured that a possible back current being supplied by the external capacitor must never exceed the given maximum ratings.

Chapter 6 DC Characteristics

6.1 General DC Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-1 Input Leakage Current

Parameter	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input leakage	1[a]	I_{LI1}	0 <= V_I <= BV_{DD5}	-1		+1	µA
	2	I_{LI2}	0 <= V_I <= V_{DD52}	-1		+1	µA
	3	I_{LI3}	0 <= V_I <= DV_{DD5}	-1		+1	µA
	5	I_{LIA}	0 <= V_I <= AV_{DD}	-0.2		+0.2	µA
	6	I_{LI6}	0 <= V_I <= MV_{DD5}	-1		+1	µA
	8	I_{LIAD}	0 <= V_I <= AV_{DD}	-2		+1	µA
	4	I_{LIS}	0 <= V_I <= SMV_{DD5}	-10		+10	µA
Injected Current per pin [b, c]	All	I_{INJ}		-2		+2	mA
Injected Current All pins [b, c]	5	I_{INJ}		-15		+32	mA

a) The pull-down resistor of P05 is active during RESET and must be switched-off during input leakage current measurement. Otherwise the pull-down resistor cause unintended current flow.

b) The injected current will not be tested during production. Value will be verified by evaluation.
The total current per pin group (injected plus operating) has to be in the limits of the absolute maximum ratings for output currents (values for output current low and output current high).
The operation voltage must stay in the limits of the operating conditions. The user has to make sure that the injected current does not pull the supplied voltage outside of the operating conditions.

c) The accuracy of the ADC specified in this document is only valid when the sum of all curents of pin group 5 is in the range of -15 mA to +32 mA.

6.2 Pin Group 1

Pin Groups 1x: Pins supplied by BV_{DD5}

- 1A: (P00-06, P50-55, P84)
- 1B: (P16-17, P30-31, P40-42, P46-47, P56-57, P100-103)
- 1C: (P20-27, P34-37, P60-67)
- 1D: (P43-45, P80-83, P85)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 4.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-2 Pin Group 1 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2	1	V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2	1	V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2	1	V_{IL2}		0		0.4 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2	1	V_{IL4}		0		0.4 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		150			mV
	Schmitt2	1	V_{HY2}		150			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
	Limit2	1	V_{OH}	I_{OH} = -5.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2	1	V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 4.0 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-3 Pin Group 1 Low Voltage Operating Range

Parameter	Pin mode [a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2	1	V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2	1	V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2	1	V_{IL2}		0		0.35 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2	1	V_{IL4}		0		0.4 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		100			mV
	Schmitt2	1	V_{HY2}		100			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -1.0 mA	BV_{DD5} - 0.45			V
	Limit2	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2		I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	1			mA
	Limit2		I_{OLM2}		2			mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-4 Pin P05 pulldown resistor

Parameter	Pin mode	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Pull down resistor		P05	V_{PD}		14	28	56	kΩ

6.3 Pin group 2: $\overline{\text{RESET}}$ and FLMD0

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-5 Pin Group 2 (except P07) Normal Operating Range

Parameter	Pin mode	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	2	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
Input voltage low	Schmitt1	2	V_{IL1}		0		0.3 V_{DD52}	V

6.4 Pin group 2: P07

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-6 P07 Normal Voltage Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
	Schmitt2	V_{IH2}		0.8 V_{DD52}		V_{DD52}	V
	CMOS1	V_{IH3}		0.7 V_{DD52}		V_{DD52}	V
	CMOS2	V_{IH4}		0.8 V_{DD52}		V_{DD52}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 V_{DD52}	V
	Schmitt2	V_{IL2}		0		0.5 V_{DD52}	
	CMOS1	V_{IL3}		0		0.3 V_{DD52}	V
	CMOS2	V_{IL4}		0		0.5 V_{DD52}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{HI2}		150			mV
Output voltage high	Limit1	V_{OH}	I_{OH} = -2.0 mA	V_{DD52} - 0.45			V
	Limit2	V_{OH}	I_{OH} = -5.0 mA	V_{DD52} - 0.45			V
Output voltage low	Limit1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2	V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	I_{OHM1}	V_{OH} = 0 V	-2			mA
	Limit2	I_{OHM2}		-5			mA
Maximum output short circuit current low	Limit1	I_{OLM1}	V_{OL} = V_{DD52}	2			mA
	Limit2	I_{OLM2}		5			mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt 2 denote the non-schmitt trigger and the schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 4.0 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-7 P07 Low Voltage Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 V_{DD52}		V_{DD52}	V
	Schmitt2	V_{IH2}		0.8 V_{DD52}			
	CMOS1	V_{IH3}		0.7 V_{DD52}			
	CMOS2	V_{IH4}		0.8 V_{DD52}			
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 V_{DD52}	V
	Schmitt2	V_{IL2}		0		0.35 V_{DD52}	V
	CMOS1	V_{IL3}				0.3 V_{DD52}	
	CMOS2	V_{IL4}				0.5 V_{DD52}	
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		100			mV
	Schmitt2	V_{HI2}		100			mV
Output voltage high	Limit1	V_{OH}	I_{OH} = -1.0 mA	V_{DD52} - 0.45			V
	Limit2	V_{OH}	I_{OH} = -2.0 mA	V_{DD52} - 0.45			V
Output voltage low	Limit1	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2	I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1	I_{OLM1}	V_{OL} = V_{DD52}	1			mA
	Limit2	I_{OLM2}		2			mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt trigger and the schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

6.5 Analog Input

This chapter describes the digital functions available at the pins supplied by AVDD. The number of available analog conversion channels differ between the devices. VCMP0/1 have no digital function.

- Pin Group 5: Pins supplied by AV_{DD}
  5: (P70 .. P715)
  Digital buffer function is only available for P70..P715.

- Pin Group 8: Pins supplied by AV_{DD}
  8: (VCMP0, VCMP1)
  VCMP0 and VCMP1 have only analog comparator function.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-8 Pin Group 5 Normal Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 AV_{DD5}		AV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 AV_{DD5}		AV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 AV_{DD5}	V
	Schmitt2	V_{IH2}		0		0.5 AV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{IH2}		150			mV

a) Schmitt1 and Schmitt2 denote the schmitt trigger input characteristics of the device pins.
b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 4.0 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} (µPD70F3427 only) = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-9 Pin Group 5 Low Voltage Operating Range

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 AV_{DD5}		AV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 AV_{DD5}		AV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 AV_{DD5}	V
	Schmitt2	V_{IH2}		0		0.35 AV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{IH2}		150			mV

a) Schmitt1 and Schmitt2 denote the schmitt trigger input characteristics of the device pins.
b) Not tested in production. Specified by design.

6.6 Pin Group 3: GPIO and LCD Bus Interface (µPD70F3426A, µPD70F3425, µPD70F3424, µPD70F3423, µPD70F3422, µPD70F3421)

- Pin Group 3: GPIO and LCD Bus interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107)

Note LCD bus function on these pins is not available in µPD70F3423, µPD70F3422 and µPD70F3421.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 4.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-10 Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 DV_{DD5}		DV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 DV_{DD5}		DV_{DD5}	V
	CMOS1		V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
	CMOS 2		V_{IH4}		0.8 DV_{DD5}		DV_{DD5}	V
Input voltage low	Schmitt1		V_{IL1}		0		0.3 DV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.4 DV_{DD5}	V
	CMOS1		V_{IL3}		0		0.3 DV_{DD5}	V
	CMOS2		V_{IL4}		0		0.4 DV_{DD5}	V
Input hysteresis [b]	Schmitt1		V_{HY1}		150			mV
	Schmitt2		V_{HY2}		150			mV
Output voltage high	Limit1		V_{OH}	I_{OH} = -2.0 mA	DV_{DD5} - 0.45			V
	Limit2		V_{OH}	I_{OH} = -5.0 mA	DV_{DD5} - 0.45			V
Output voltage low	Limit1		V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2		V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1		I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	$V_{OL} = DV_{DD5}$	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software. CMOS2 and SCHMITT2 are only available on Port P8.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 4.0 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-11 Pin Group 3 Low Voltage Operating Range

Parameter	Pin mode [a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 DV_{DD5}		DV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 DV_{DD5}		DV_{DD5}	V
	CMOS1		V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
	CMOS2		V_{IH4}		0.8 DV_{DD5}		DV_{DD5}	V
Input voltage low	Schmitt1		V_{IL1}		0		0.3 DV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.35 DV_{DD5}	V
	CMOS1		V_{IL3}		0		0.3 DV_{DD5}	V
	CMOS2		V_{IL4}		0		0.4 DV_{DD5}	V
Input hysteresis [b]	Schmitt1		V_{HY1}		100			mV
	Schmitt2		V_{HY2}		100			mV
Output voltage high	Limit1		V_{OH}	I_{OH} = -1.0 mA	DV_{DD5} - 0.45			V
	Limit2		V_{OH}	I_{OH} = -2.0 mA	DV_{DD5} - 0.45			V
Output voltage low	Limit1		V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2		V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1		I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2		I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = DV_{DD5}	1			mA
	Limit2		I_{OLM2}		2			mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Caution Do not operate buffers of pin group 3 in current limit state, when the LCD function is used. Failing to do so may lead to a decreased accuracy of the LCD waveforms.

6.7 Pin Group 3: GPIO and LCD Bus and external Memory Interface (µPD70F3427)

- Pin Group 3: GPIO and LCD Bus interface and external memory interface supplied by DV_{DD5}
  3: (P32-33, P86-87, P90-97, P104-107, P141-142)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V,
MV_{SS5} = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-12 Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	CMOS1	3	V_{IH3}		0.7 DV_{DD5}		DV_{DD5}	V
Input voltage low	CMOS1		V_{IL3}		0		0.3 DV_{DD5}	V
Output voltage high	No Limit		V_{OH}	I_{OH} = -5.0 mA	DV_{DD5} - 0.45			V
Output voltage low	No Limit		V_{OL}	I_{OL} = 5.0 mA			0.45	V

a) CMOS1 denotes the fixed non-schmitt input characteristics of these device pins. This pin group does not support current limitation.

6.8 Pin Group 6: External Memory Interface (µPD70F3427)

- Pin Group 6: External Memory Interface supplied by MV_{DD5}
  6: (A0-23, D0-15, $\overline{CS0\text{-}1}$, $\overline{CS3\text{-}4}$, $\overline{WAIT}$, $\overline{RD}$, $\overline{WR}$, $\overline{BE0\text{-}1}$, P140)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 4.0 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5}$ = 0 V

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-13 Pin Group 3 Normal Operating Range

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	CMOS1	6	V_{IH6}		0.7 MV_{DD5}		MV_{DD5}	V
Input voltage low	CMOS1		V_{IL6}		0		0.3 MV_{DD5}	V
Output voltage high	No Limit		V_{OH}	I_{OH} = -5.0 mA	MV_{DD5} - 0.45			V
Output voltage low	No Limit		V_{OL}	I_{OL} = 5.0 mA			0.45	V

a) CMOS1 denotes the fixed non-schmitt input characteristics of the device pins. This pin group does not support current limitation.

6.9 LCD Common and Segment Lines

Note The LCD common and segment function is only available in µPD70F3423, µPD70F3422 and µPD70F3421.

Conditions T_A = -40°C ~ +85°C,
$DV_{DD5} = BV_{DD5}$ = 4.5 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 4.0 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note
1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. The power supply configuration is restricted, when the LCD is used. The LCD voltages are generated centrally. Since the LCD output buffers are supplied by different supplies (BV_{DD5} and DV_{DD5}) it is necessary that BV_{DD5} is equal to DV_{DD5}.

Table 6-14 DC Characteristics LCD Common and Segment Lines

Parameter	Symbol	TestConditions	Min.	Typ	Max	Unit
LCD Segment Output Voltage (unloaded)	V_{ODS}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}[a]	V_{LCDn} + 0.2	V
LCD Common Output Voltage (unloaded)	V_{ODC}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}	V_{LCDn} + 0.2	V
LCD split voltage [b]	V_{LC0}	IO = ±1.5 mA	V_{LCD0} - 0.1	V_{LCD0}	V_{LCD0} + 0.1	V
	V_{LC1}	IO = ±1.0 mA	V_{LCD1} - 0.1	V_{LCD1}	V_{LCD1} + 0.1	V
	V_{LC2}	IO = ±1.0 mA	V_{LCD2} - 0.1	V_{LCD2}	V_{LCD2} + 0.1	V
	V_{LC3}	IO = ±1.5 mA	V_{LCD3} - 0.1	V_{LCD3}	V_{LCD3} + 0.1	V
LCD Series resistance[c]	R_{LCDS}	Segment lines, V_{LCDn} to pin			1.8	kΩ
	R_{LCDC}	Common lines, V_{LCDn} to pin			1.8	kΩ
LCD operation current	IDD_{LCD}	Frame frequency 244Hz, all segment and common lines set to LCD mode and open.			280	µA

a) VLCDn (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.
b) The split voltage is an internal design value. Direct measurement is not possible.
c) The series resistance is an internal design value. Direct measurement is not possible.

Caution Do not operate buffers of pin group 3 in current limit state, when the LCD function is used. Failing to do so may lead to a decreased accuracy of the LCD waveforms.

Table 6-15 Definitions for V_{LCD}

Parameter	Voltage[a]
VLCD0	DV_{DD5}
VLCD1	2/3 x DV_{DD5}
VLCD2	1/3 x DV_{DD5}
VLCD3	0 x DV_{DD5} = DV_{SS5}

a) The LCD voltage is always derived from one central supply DV_{DD5}, even when the pin is supplied by a di fe-rent supply in port or special function mode.

6.10 Stepper Motor Driver IO

- Pin Group 4: Stepper Motor outputs supplied by SMV_{DD5}
  4A: (P110-117, P120-123)
  4B: (P124-127, P130-137)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 4.0 V, SMV_{DD5} = 4.0 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-16 DC Characteristics Stepper Motor Driver Input Normal Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 SMV_{DD5}		SMV_{DD5}	V
	CMOS1	V_{IH3}		0.7 SMV_{DD5}		SMV_{DD5}	V
	CMOS2	V_{IH4}		0.8 SMV_{DD5}		SMV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	Schmitt2	V_{IL2}		0		0.5 SMV_{DD5}	V
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
	CMOS2	V_{IL4}		0		0.5 SMV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{HI2}		150			mV

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.0 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-17 DC Characteristics Stepper Motor Driver Input Low Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 SMV_{DD5}			
	CMOS1	V_{IH3}		0.7 SMV_{DD5}			
	CMOS2	V_{IH4}		0.8 SMV_{DD5}			
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	Schmitt2	V_{IL2}		0		0.35 SMV_{DD5}	V
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
	CMOS2	V_{IL4}		0		0.35 SMV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		100			mV
	Schmitt2	V_{HI2}		100			mV

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
b) Not tested in production. Specified by design.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 4.75 V ~ 5.25 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note
1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. The stepper output drivers have no current limitation and are not protected regarding short circuit.

Table 6-18 DC Characteristics Stepper Motor Driver Output Normal Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -40 mA, T_A= -40°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -30 mA, T_A= +25°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -27 mA, T_A= +85°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = 40 mA, T_A= -40°C	0		0.5	V
		V_{OL}	I_{OL} = 30 mA, T_A= +25°C	0		0.5	V
		V_{OL}	I_{OL} = 27 mA, T_A= +85°C	0		0.5	V
Output voltage deviation [a]		V_{DEV}		0		50	mV
Output Slew rate [b]		t_{RF}	10% - 90%	12	25	70	ns
Peak Cross Current[c]		I_{CROSS}				50	mA
Output Pulse width[d]		t_{MO}		125			ns
Output Pulse length deviation[e]		t_{SMDEV}		-10	+5	+45	ns

a) Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (| V_{OHx} - V_{OHy} | , | V_{OLx} - V_{OLy} |) @ I_{OHx} = I_{OHy}, I_{OLx}=I_{OLy}.
x and y denote any combination of two pins of the following pin groups: (P110-P113, P114-117, P120-123, P124-P127, P130-P133, P134-P137)
The output voltage deviation is not tested, but specified by design.

b) The slew rate is not tested, but derived from simulation.

c) The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transistion time t_{RF}. It flows in addition to the output current. The cross current is not tested, but derived from simulation.

d) The output buffer can not generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested, but derived from simulation.

e) The slew rate control function causes a deviation of output pulse time compared to the ideal selected output pulse setting. This value is not tested, but derived from simulation.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4-75 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-19 DC Characteristics Stepper Motor Driver Output Low Voltage Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -5 mA,	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = +5 mA,	0		0.5	V

- Pin Group 7: All pins supplied with Zero Point detection function
  This group is a subset of group 4
  7: (P113, P117, P120-127, P133, P137)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.0 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-20 DC Characteristics Stepper Motor Driver Zeropoint Detection

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold voltage	V_{IL1}		1/9 SMV_{DD5} - 70mV		1/9 SMV_{DD5} + 70mV	V
Detection delay	t_{ZPDD}	100mV Step, 50mV overdrive			100 [a]	ns

a) Not tested in production. Specified by design.

6.11 Current Limit Function of I/O buffers

The output buffers of following pin groups incorporate a current limiting function:

- μPD70F3426A, μPD70F3425, μPD70F3424, μPD70F3423, μPD70F3422, μPD70F3421:
  pin groups 1, 3 and P07 of pin group 2
- μPD70F3427: pin group 1 and P07 of pin group 2

This function limits the output current of the buffer to a certain value during output signal switching.

The limit is disabled when the buffer output voltage is near to its target voltage, thus providing full drivability. During full drivability the current may reach values given in absolute maximum ratings for a single pin.

The user can select different limit ranges by software (refer to User's Manual for details).

The limit function is independant from the operation mode of the device.

A permanent short circuit of these outputs is not permitted.

The stepper motor driver outputs do not support a current limiting function.

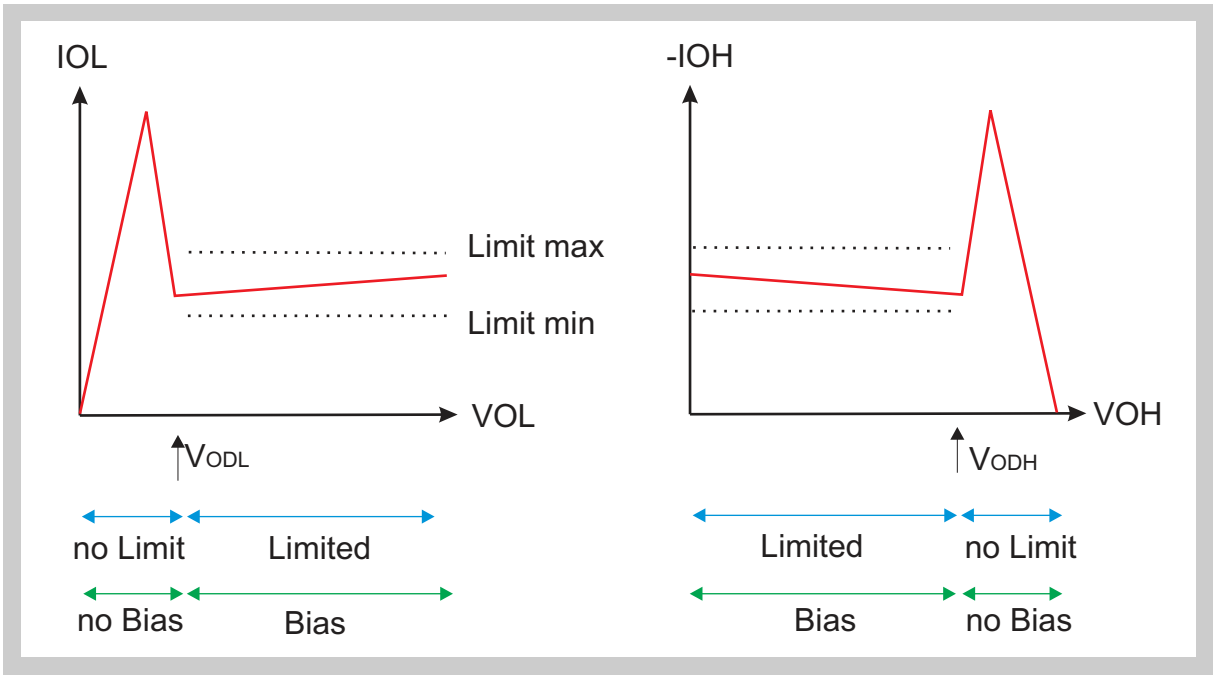


Figure 6-1 Current Limit Function Principle

Note The current limit function of the I/O buffers needs additional bias current to control the output stage. The additional bias current depend on the status of each buffer. Each buffer with either high or low output and in the stage of current limiting will draw this bias current.

Table 6-21 Buffer status for bias current

Intended Output	Current limit	additional current
L	No	No
L	Yes	Yes
H	No	No
H	Yes	Yes

Conditions

T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note

1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. The function of the current limiting operation is sensitive against inductive loads under a certain condition:
   - The load of the pin is below the selected current limit and the device could reach a sufficient output voltage. The device changed to full drivability.
   - The external circuitry sinks/sources more and more current.
   - The current creates an increasing voltage drop in the output stage of the device.
   - The increasing voltage drop enables the current limiting function.
   - The enabling of the current limit together with an external inductance may lead to an oscillation of the output between the limited and unlimited state. The external inductance creates voltage peaks that change the state of the output buffers current limiting function.
   - Recommendation: keep external inductance small (keep external wiring short).
3. The pin group 3 of the derivative µPD70F3427 does not include a current limit function.

Table 6-22 DC Characteristics of Current Limiting Function [a]

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Limit disable threshold voltage for V_{OH}		V_{ODH}		VDDx[b] - 1.6		VDDx - 1.1	V
Limit disable threshold voltage for V_{OL}		V_{ODL}		1.1		1.6	V
Supply Current per buffer for current limitation [c]	Limit1	I_{DDCL1}				0.8	mA
	Limit2	I_{DDCL2}				1.7	mA

a) These values are not tested. They are given based on design simulation.
b) VDDx denotes the corresponding voltage supply of the pin.
c) This current need not be considered during absolute maximum current calculation.

6.12 Supply Current

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 6-23 DC Characteristics Supply Current µPD70F3426A [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64 MHz; SSCG,PLL: on)		100	130	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		77	100	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		57	75	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		46	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		35	45	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	30	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		15	19	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		1	1.3	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		8.1	11	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		48	65	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		39	50	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		5	7	mA

Table 6-23 DC Characteristics Supply Current µPD70F3426A [a] (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		190	390	µA
	I_{DD6A}	WATCH Monitored		205	430	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-Osc		65	215	µA

a) These values are target values without current consumption due to external circuitry at the IO-pins.

Caution Valid for all devices:
In case any flash-self-programming library function is executed during any operating condition mentioned above the current consumption of the concerned operating condition may increase.
The additional current consumption that may arise during the execution of any flash-self-programming library function is specified in the table below.

Table 6-24 Additional Supply Current (Operating) during Self-Flash-Programming

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Additional supply current	I_{DD1x}	Any Operating		1	3	mA

Table 6-25 DC Characteristics Supply Current µPD70F3427 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64 MHz; SSCG,PLL: on)		82	123	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		65	98	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	36	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		6	9	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		150	350	µA
	I_{DD6A}	WATCH Monitored		165	390	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-OSC		65	215	µA

a) These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-26 DC Characteristics Supply Current µPD70F3425, µPD70F3424 [a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD10}	Operating (f_{CPU} = 64MHz; SSCG,PLL: on)		82	123	mA
	I_{DD11}	Operating (f_{CPU} = 48 MHz; SSCG,PLL: on)		65	98	mA
	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD21}	HALT Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 64 MHz; SSCG,PLL: on)		6	9	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 48 MHz; SSCG,PLL: on)		5	7.5	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		150	350	µA
	I_{DD6A}	WATCH Monitored		165	390	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-OSC		65	215	µA

a) These values are target values without current consumption due to external circuitry at the IO-pins.

Table 6-27 DC Characteristics Supply Current µPD70F3423, µPD70F3422, µPD70F3421[a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD12}	Operating (f_{CPU} = 32 MHz; SSCG,PLL: on)		48	72	mA
	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	60	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		32	48	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		10	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.2	1.2	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC = 300 kHz; SSCG,PLL: off)		3.3	6	mA
	I_{DD20}	HALT Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		24	36	mA
	I_{DD20}	HALT Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		20	30	mA
	I_{DD21}	HALT Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		16	24	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 32 MHz; SSCG,PLL: on)		3.8	5.7	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 24 MHz; SSCG,PLL: on)		3.5	5.3	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		3.2	4.8	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		150	350	µA
	I_{DD6A}	WATCH Monitored		165	390	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on Ring-OSC		65	215	µA

a) These values are target values without current consumption due to external circuitry at the IO-pins.

Note The low current modes (STOP, WATCH, SUB WATCH) are tested under the following conditions:

- Operation modes setting as described in table below.
- All functional pins with output possibility are set to output with alternating high and low output levels.
- Testequipment is disconnected from output pins.
- IDD is the total sum of currents to the device supply pins V_{DD5}, BV_{DD5}, DV_{DD5}, SMV_{DD5}, AV_{DD}
- Device drives its own leakage currents by its output stages.
- The leakage current is included in the given IDD values.

Table 6-28 Operational Conditions for Measurement

Unit	Watch	Watch monitored	Sub Watch	Sub Watch on Ring-OSC	Sub Watch monitored	STOP
Main-oscillator	running	running	stopped	stopped	stopped	stopped
Sub-oscillator	stopped (XT1 clamped)	stopped (XT1 clamped)	running	stopped (XT1 clamped)	running	stopped
Ring-oscillator	stopped	running	stopped	running	running	stopped
SSCG	stopped	stopped	stopped	stopped	stopped	stopped
PLL	stopped	stopped	stopped	stopped	stopped	stopped
CPU system	stopped	stopped	stopped	stopped	stopped	stopped
IICCLK	stopped	stopped	stopped	stopped	stopped	stopped
PCLK0, PCLK1	stopped	stopped	stopped	stopped	stopped	stopped
PCLK2…PCLK15	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK0, SPCLK1	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK2…SPCLK15	stopped	stopped	stopped	stopped	stopped	stopped
FOUT	stopped	stopped	stopped	stopped	stopped	stopped
WTCLK	running	running	running	running	running	stopped
WDTCLK	stopped	stopped	stopped	stopped	stopped	stopped
TM0CLK	stopped	stopped	stopped	stopped	stopped	stopped
LCD	disabled	disabled	disabled	disabled	disabled	disabled
ADC	disabled	disabled	disabled	disabled	disabled	disabled
VCOMP	disabled	disabled	disabled	disabled	disabled	disabled
Regulator[a]	Standby	Standby	Standby	Standby	Standby	Standby

a) Regulator in standby: STBCTL = 0x03

Chapter 7 AC Characteristics

7.1 AC Test Input/Output Waveform

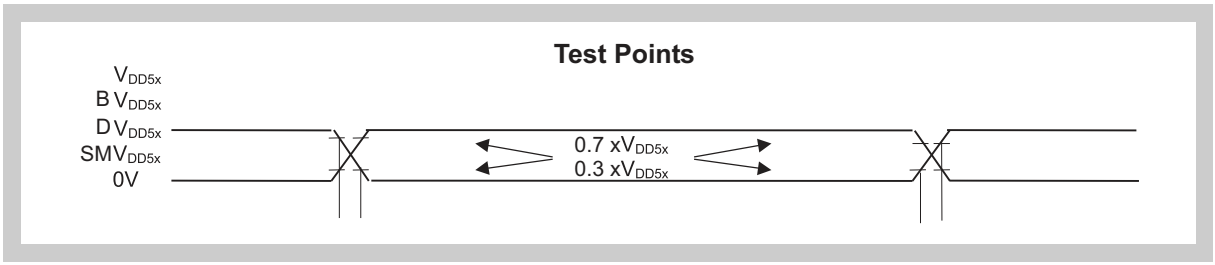


Figure 7-1 AC Test Input/Output Waveform

7.2 AC Test Load Condition

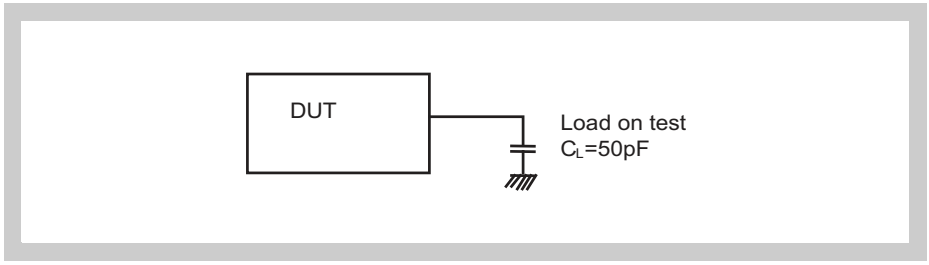


Figure 7-2 AC Test Load Condition

7.3 Reset

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 7-1 Reset AC Characteristics

Parameter	Symbol	Test Conditions	MIN.		MAX.	Unit
$\overline{\text{RESET}}$ high-level width [a]	t_{WRSH}		500			ns
$\overline{\text{RESET}}$ low-level width [b]	t_{WRSL}		500			ns
$\overline{\text{RESET}}$ Pulse rejection [c]	t_{WRRJ}		50			ns

a) This signal high time is needed to ensure that the internal $\overline{\text{RESET}}$ release operation starts.
b) This signal low time is needed to ensure that the internal $\overline{\text{RESET}}$ is activated.
c) The $\overline{\text{RESET}}$ input incorporates an analog filter. Pulses shorter than this minimum will be ignored. Not tested in production.

Note Reset pulses shorter than the given value may not be recognized by the device, they do not cause undefined states of the device.

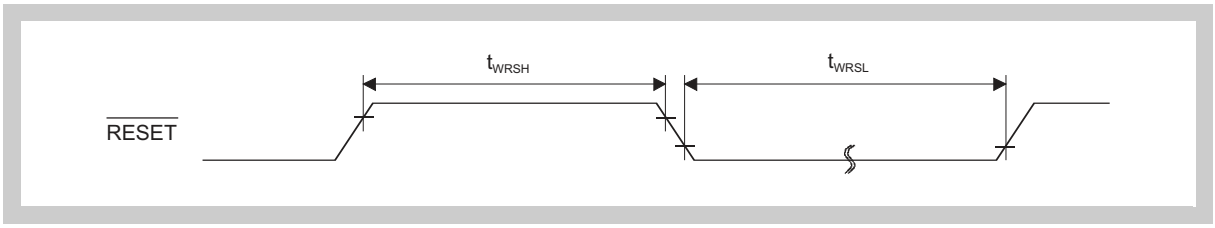


Figure 7-3 Reset Timing

7.4 Interrupt Timing

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 7-2 Interrupt AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NMI high-level width [a]	t_{NIH}		360			ns
NMI low-level width [a]	t_{NIL}		360			ns
NMI pulse rejection [b]	t_{NIRJ}		50		360	ns
INTPn[c] high-level width [a]	t_{ITH}		360			ns
INTPn[c] low-level width [a]	t_{ITL}		360			ns
INTPn[c] pulse rejection [b]	t_{ITRJ}		50		360	ns

a) Pulses longer than this value will pass the input filter.
b) Pulses shorter than this value do not pass the input filters. not tested in production.
c) n = 0 to 7

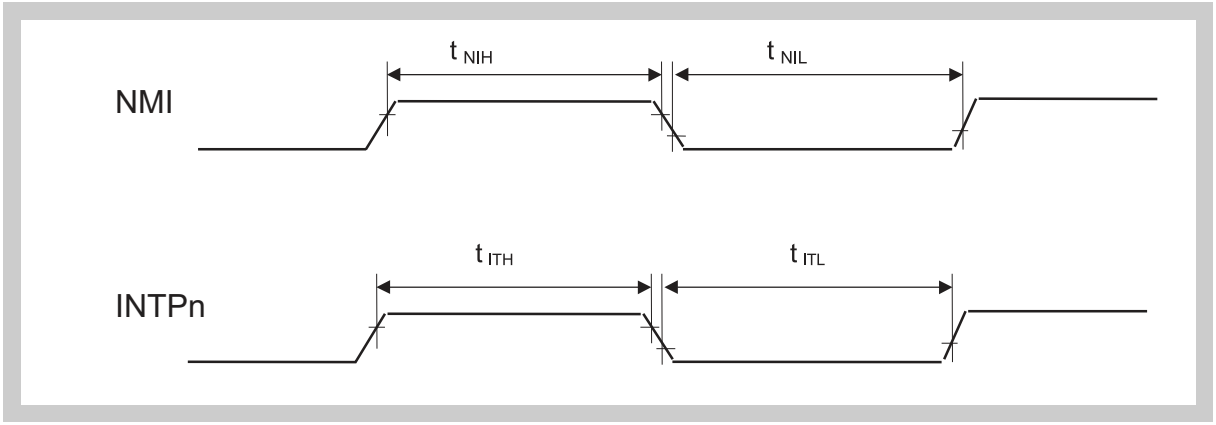


Figure 7-4 Interrupt Timing

Note Interrupt timing is generated by analog delay elements. Delay characteristics have a wide range in production.

7.5 Peripheral Function Characteristics

The following conditions are valid for all peripheral function characteristics unless otherwise noted.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

7.5.1 Timer P

Table 7-3 Timer P AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIPmn[a] high-level width	t_{TIPHD}	Digital filter	45 +3/f_{PCLK0}[b]			ns
	t_{TIPHNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPHNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns
TIPmn [a] low-level width	t_{TIPL}	Digital filter	45 +3/f_{PCLK0}			ns
	t_{TIPLNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPLNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns

a) m = 3…0, n = 1…0
b) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

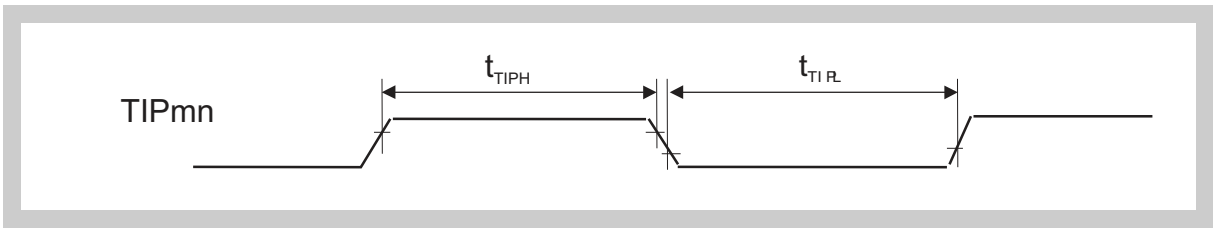


Figure 7-5 Timer P Input Timing

7.5.2 Timer G

Table 7-4 Timer G Input Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIGmn[a] high-level width	t_{TIGH1}	Digital filter, f_{PCLK0}[b] = f_{CCLK}[c]	$45 + 3/f_{PCLK0}$			ns
	t_{TIGH2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	$45 + 2/f_{CCLK}$			ns
	t_{TIGH0}	No digital filter	$45 + 2/f_{CCLK}$			ns
TIGmn[a] low-level width	t_{TIGL1}	Digital filter, $f_{PCLK0} = f_{CCLK}$	$45 + 3/f_{PCLK0}$			ns
	t_{TIGL2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	$45 + 2/f_{CCLK}$			ns
	t_{TIGL0}	No digital filter	$45 + 2/f_{CCLK}$			ns

a) m = 0…1: n = 1…4; m = 2: n = 0...5
b) f_{SPCLK0} is the clock frequency of the digital filter connected to the input pin.
c) f_{CCLK} is the count clock frequency of the Timer G.

7.5.3 UARTA

Table 7-5 UARTA AC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Transfer rate	T_{UARTA}		0.3	1000	Kbps

7.5.4 CAN

Table 7-6 CAN AC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Transfer rate	T_{FCAN}	f_{CAN}[a] ≥ 8 MHz		1	Mbps

a) f_{CAN} is the CAN macro clock frequency. For CAN clock selection refer to User's Manual of the CAN.

7.5.5 CSIB (High Voltage Operation)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 4.5 V ~ 5.5 V, BV_{DD5} = 4.5 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 3.6 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note
1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. n = 0 to 2

(1) CSIB Master Mode

(a) With Digital Filter

Table 7-7 CSIB Master Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		50 + $4/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-31 - $4/f_{PCLK0}$		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			6	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-8 CSIB Master Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		50		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-31		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			6	ns

(2) CSIB Slave Mode

(a) With Digital Filter

Table 7-9 CSIB Slave Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		$4/f_{PCLK0}$ - 5		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		$4/f_{PCLK0}$ - 5		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$[a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			$45 + 3/f_{PCLK0}$	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-10 CSIB Slave Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		50		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		5		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			45	ns

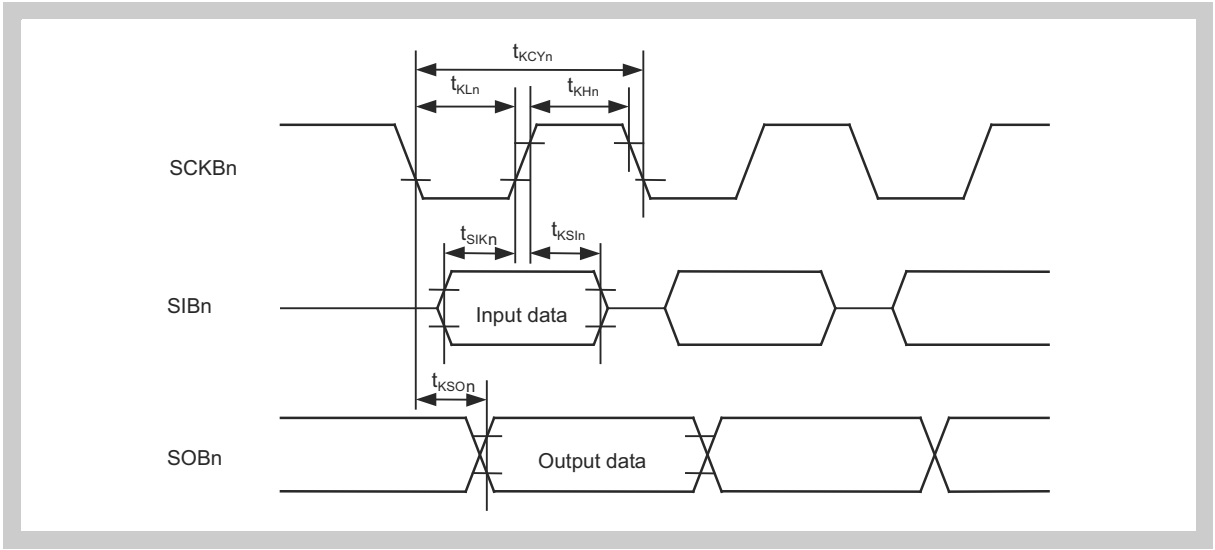


Figure 7-6 CSI Master/Slave Mode Timing

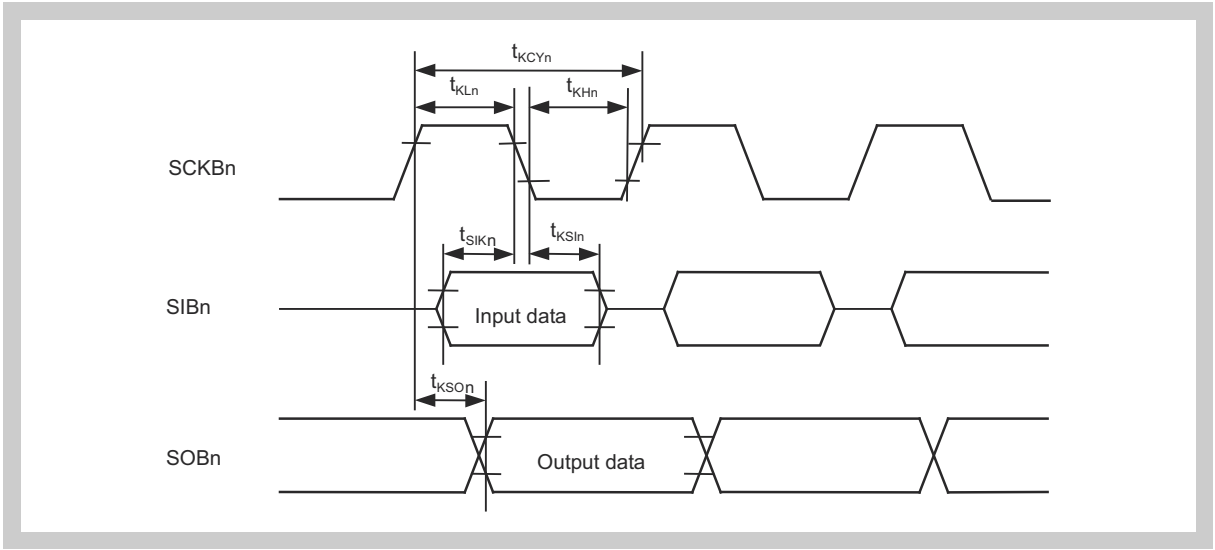


Figure 7-7 CSI Master/Slave Mode Timing Inverted Clock

7.5.6 CSIB (Low Voltage Operation)

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 4.5 V, BV_{DD5} = 3.0 V ~ 4.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 3.6 V (μPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (μPD70F3427 only)

Note
1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. n = 0 to 2

(1) CSIB Master Mode

(a) With Digital Filter

Table 7-11 CSIB Master Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		93 + $4/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-49 - $4/f_{PCLK0}$		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			45	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-12 CSIB Master Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 80		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 80		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		93		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-49		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			45	ns

(2) CSIB Slave Mode

(a) With Digital Filter

Table 7-13 CSIB Slave Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		$4/f_{PCLK0}$ - 5		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		$4/f_{PCLK0}$ - 5		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$[a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			$100 + 3/f_{PCLK0}$	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-14 CSIB Slave Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		50		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		5		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			100	ns

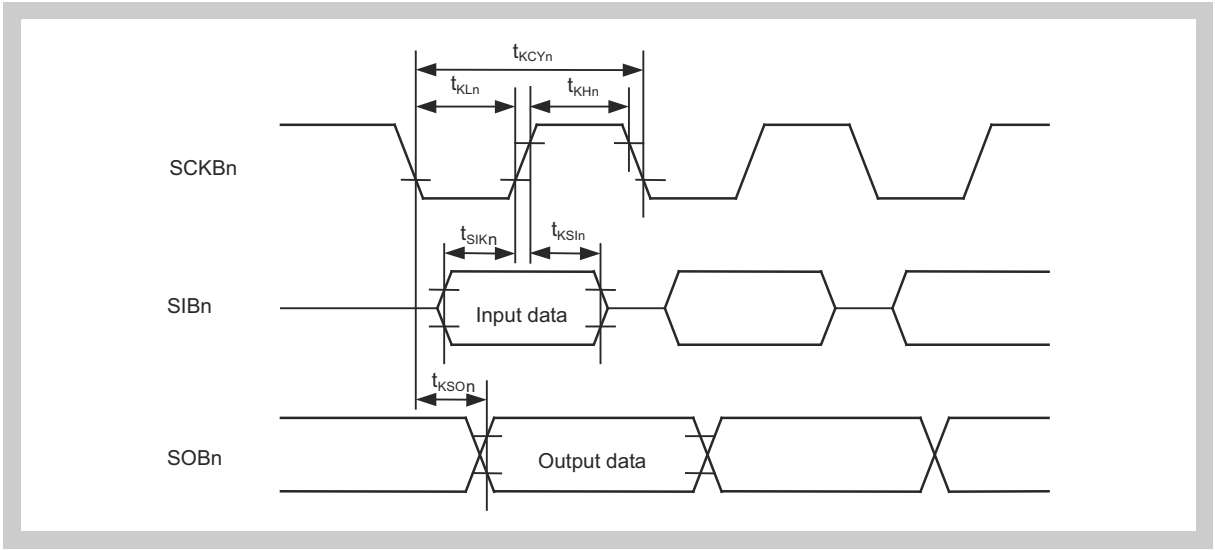


Figure 7-8 CSI Master/Slave Mode Timing

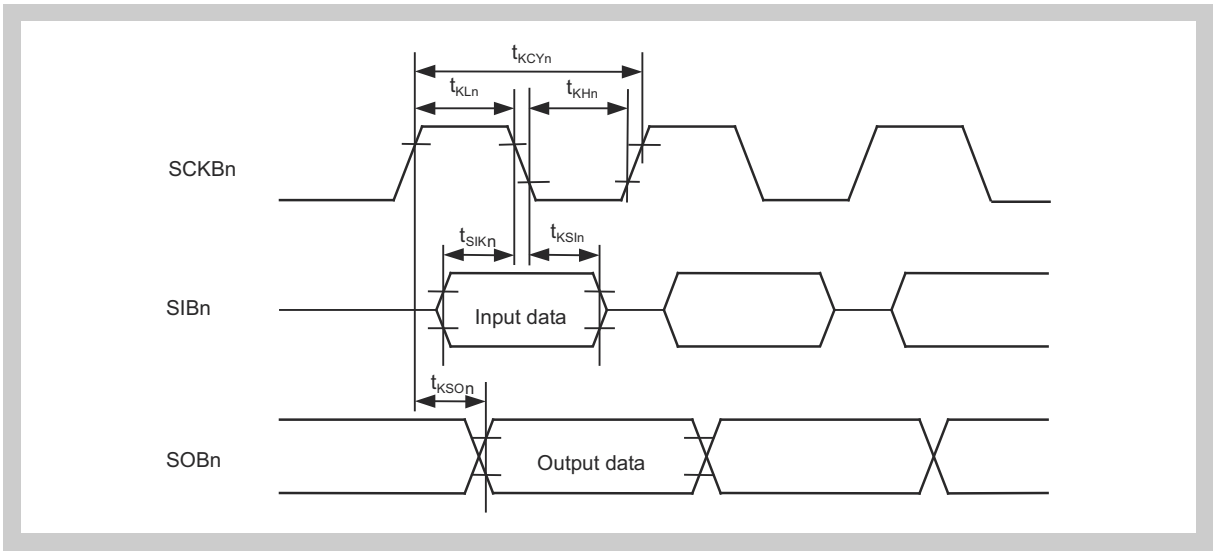


Figure 7-9 CSI Master/Slave Mode Timing Inverted Clock

7.5.7 I²C

Table 7-15: I²C AC Characteristics

Parameter		Symbol	Normal Mode		Fast-speed Mode		Unit
			min	max	min	max	
SCLn clock frequency		f_{CLK}	0	100	0	380	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	µs
Hold time[a]		$t_{HD:STA}$	4.0	—	0.6	—	µs
SCLn clock low-level width		t_{LOW}	4.7	—	1.3	—	µs
SCLn clock high-level width		t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	µs
	I²C mode		0[b]	3.45 [c]	0[Note b]	0.9[c]	µs
Data setup time		$t_{SU:DAT}$	250	—	100[d]	—	ns
STOP condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	µs
Noise suppression [e]		t_{SP}				t_{IICLK}[f]	ns
Capacitive load of each bus line		C_b	—	400	—	400	pF

a) At the start condition, the first clock pulse is generated after the hold time

b) The system requires a minimum of 300ns hold time Internally for the SDAn signal (at V_{IHmin} of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

c) If the system does not extend the SCLn signal low hold time (t_{low}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

d) The fast-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the fast-speed-mode IIC bus so that It meets the following conditions:
- If the system does not extend the SCLnn signal's low state hold time: $t_{SU:DAT}$>/=250ns
- If the system extends the SCLn signal's low state hold time:
Transmit the following data bit to the SDAn line prior to releasing the SCLn line (t_{Rmax}.+$t_{SU:DAT}$=1000+250=1250ns: Normal mode IIC bus specification).

e) Noise suppression is only available in Fast-speed mode.

f) t_{IICLK} is the period of the IICLK supplied by the clock controller.

Note n = 0, 1

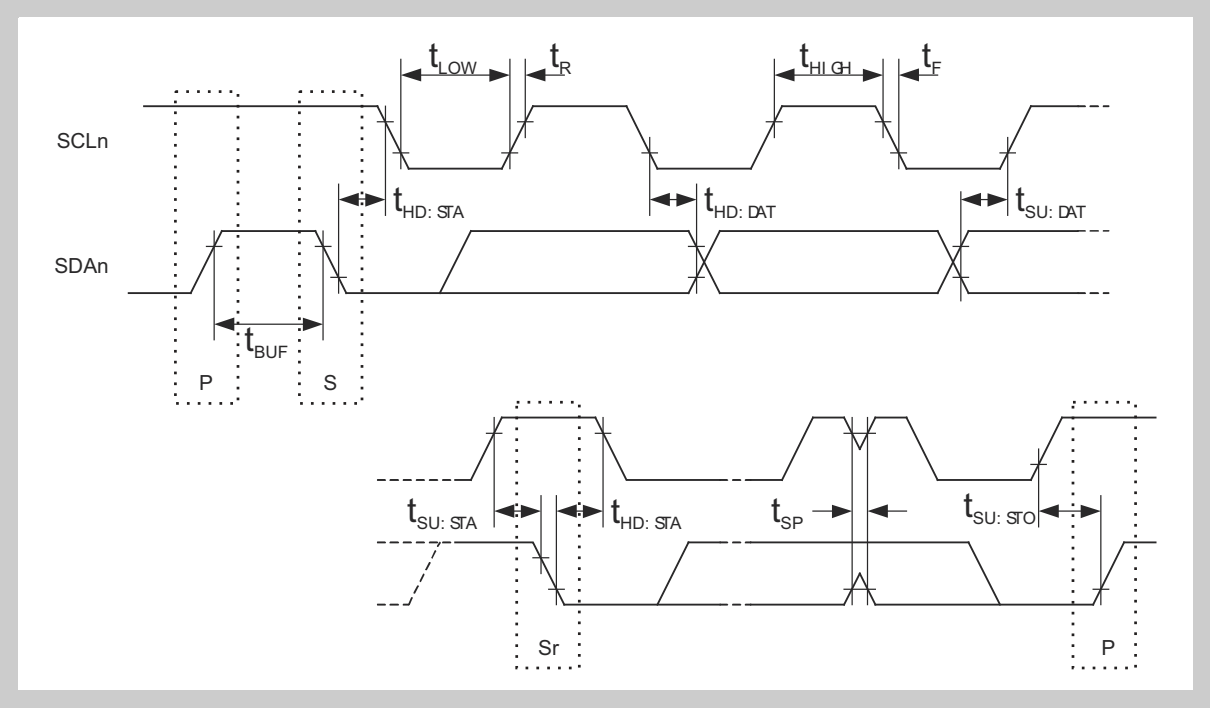


Figure 7-10 I^2C Timing

Remarks

1. P: Stop condition
2. S: Start condition
3. Sr: Restart condition
4. Rise and Fall time depend on the actual load of the signal and the selected output current limit. For a capacitive load the time can be roughly calculated from:
   ($t_R = V_{OH} / I_{OH} * C_L$),
   ($t_F = V_{OH} / I_{OL} * C_L$)

7.6 LCD Bus Interface

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.15 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

The following tables shows the timing of pin group 3 used as LCD bus interface with Schmitt1 input characteristic and unlimited output current.

Table 7-16 LCD Bus Interface AC Characteristics

Parameter	Symbol	Cond.	Min.[a]	Max.	Unit
Cycle Time	t_{CYC}		CYC x T - 5	-	ns
Control LOW-Pulse Width	t_{CL}		(WST+1)T - 50	-	ns
Enable Active Pulse Width	t_{ELH}		(WST+1)T - 35	-	ns
Control Setup Time	t_{RWS}		0.5 T + 2	-	ns
Control Hold Time	t_{RWH}		0.5 T	-	ns
Data Output Setup Time	t_{DOS}		0.5 T - 20	0.5 T + 12	ns
Data output Hold Time	t_{DOH}		[CYC-(WST+1.5)] T - 88	-	ns
Data Input Setup Time	t_{DIS}		117	-	ns
Data Input Hold Time	t_{DIH}		0	-	ns
Output Disable Time	t_{OD}		0.5 T + 5	-	ns

a) T: $1/f_{LCD}$ (LCD Bus Interface macro clock frequency)
For clock selection refer to functional specification of the LCD Bus Interface
Always keep CYC $\geq$ 2
Always keep WST $\leq$ (CYC-2)

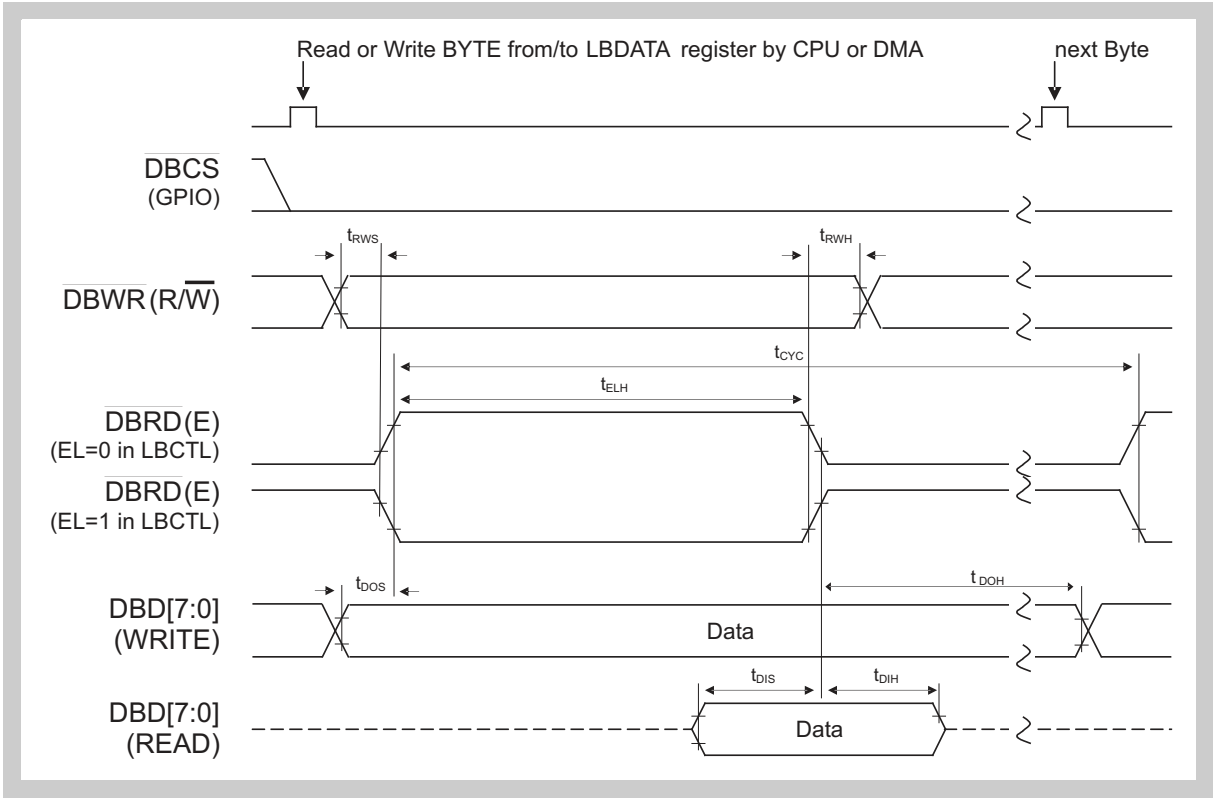


Figure 7-11 LCD Bus Interface mod68 Mode Timing

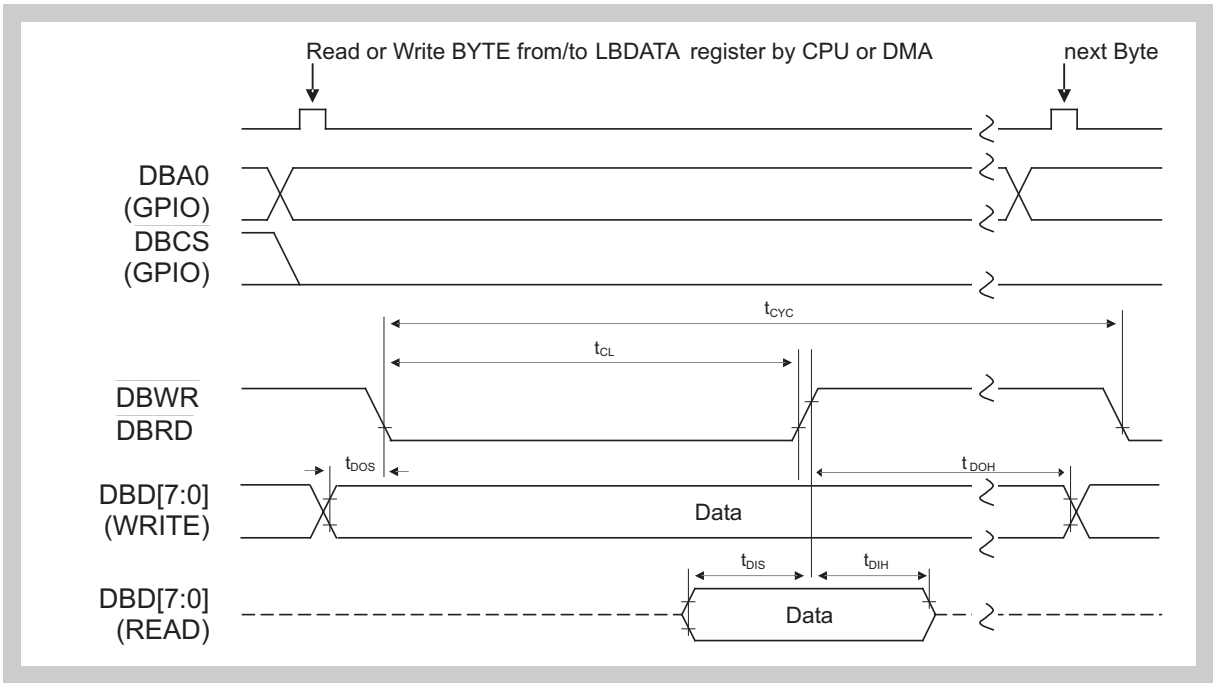


Figure 7-12 LCD Bus Interface mod80 Mode Timing

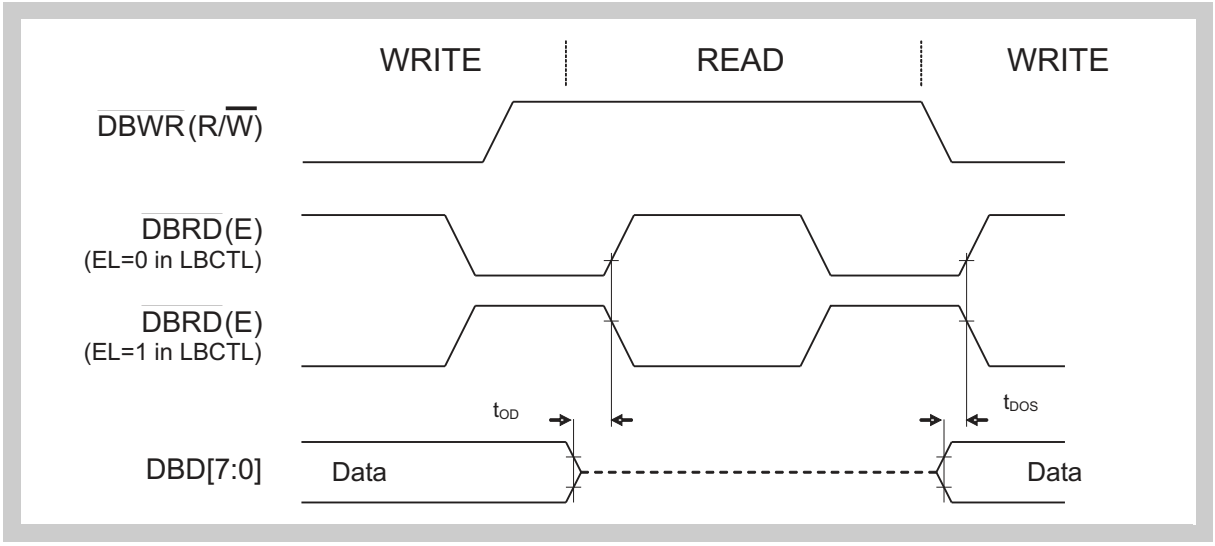


Figure 7-13 LCD Bus Interface mod68 Mode Turnaround Timing

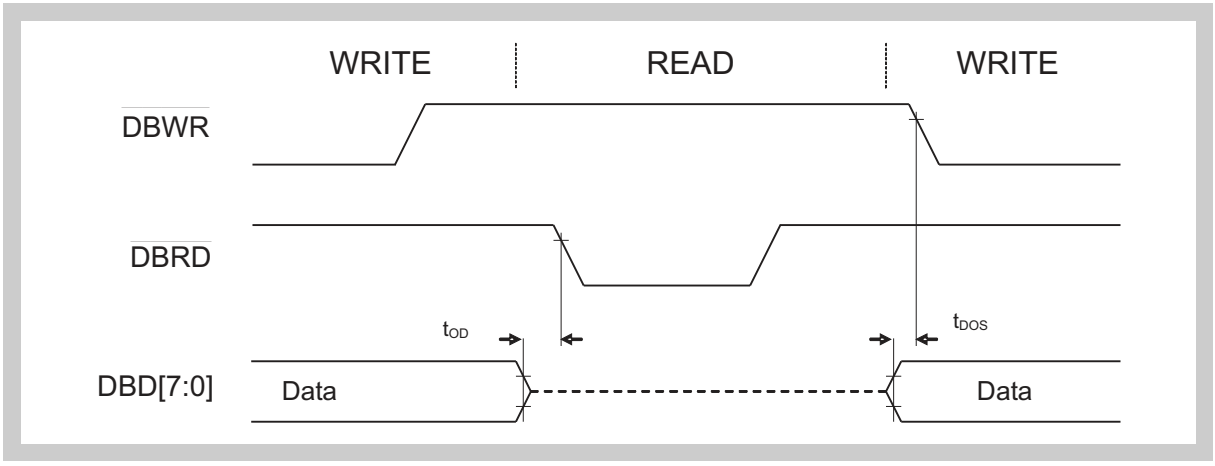


Figure 7-14 LCD Bus Interface mod80 Mode Turnaround Timing

7.7 External Memory Access (µPD70F3427)

7.7.1 Asynchronous bus timing

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V (if used as ext. mem. I/F, DV_{DD5} = 3.0 V ~ 5.5 V otherwise),
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 3.6 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = 0 V
Output pin load capacitance: C_L= 50pF

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 7-17 External Memory Access Asynchronous Read Timing

Parameter	Symbol		Conditions	Min	Max	Unit
Data input set up time D0-D15 (vs.address)	<10>	T_{SAID}			$(2.0+W_T)T - 22$	ns
Data input set up time D0-D15 (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}			$(1.5+W_D)T - 21$	ns
Data input set up time D16-D31 (vs.address)	<10>	T_{SAID}			$(2.0+W_T)T - 27$	ns
Data input set up time D16-D31 (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}			$(1.5+W_D)T - 26$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}		$(1.5+W_D)T - 12$		ns
$\overline{RD}$ Low level width (delayed RD)	<12a>	T_{WRDL}		$(2+W_D)T - 12$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}		$(1.5+W_{AS}+i)T - 12$		ns
$\overline{RD}$ High level width (delayed RD)	<13a>	T_{WRDH}		$(1+W_{AS}+i)T - 12$		ns
Address to $\overline{RD}$ delay time	<14>	T_{DARD}		$(0.5+W_{AS)}T - 5$		ns
$\overline{CSn}$ to $\overline{RD}$ delay time	<14a>	T_{DCRD}		$(0.5+W_{AS})T - 5$		ns
$\overline{BEn}$ to $\overline{RD}$ delay time	<14b>	T_{DCRD}		$(0.5+W_{AS})T - 5$		ns
$\overline{RD}$ address delay time	<15>	T_{DRDA}		iT - 7		ns
$\overline{RD}$ address delay time (delayed RD)	<15a>	T_{DRDA}		(-0.5+i)T - 7		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}		-11		ns
Data input hold time (vs. delayed $\overline{RD}\uparrow$)	<16a>	T_{HRDID}		-0.5T - 11		ns
Write data output delay time after $\overline{RD}\uparrow$	<17>	T_{DRDOD}		(1+i)T - 12		ns
Write data output delay time after delayed $\overline{RD}\uparrow$	<17a>	T_{DRDOD}		(0.5+i)T - 12		ns

Note T: $1 / f_{CPU}$ (= frequency of system clock)
i: Number of idle states specified by BCC register
W_T: Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS}: Number of waits specified by ASC register
W_D: Number of waits specified by DWC0, DWC1 register in SRAM mode and during off-page access in page mode. PRC register during on-page access in page mode.

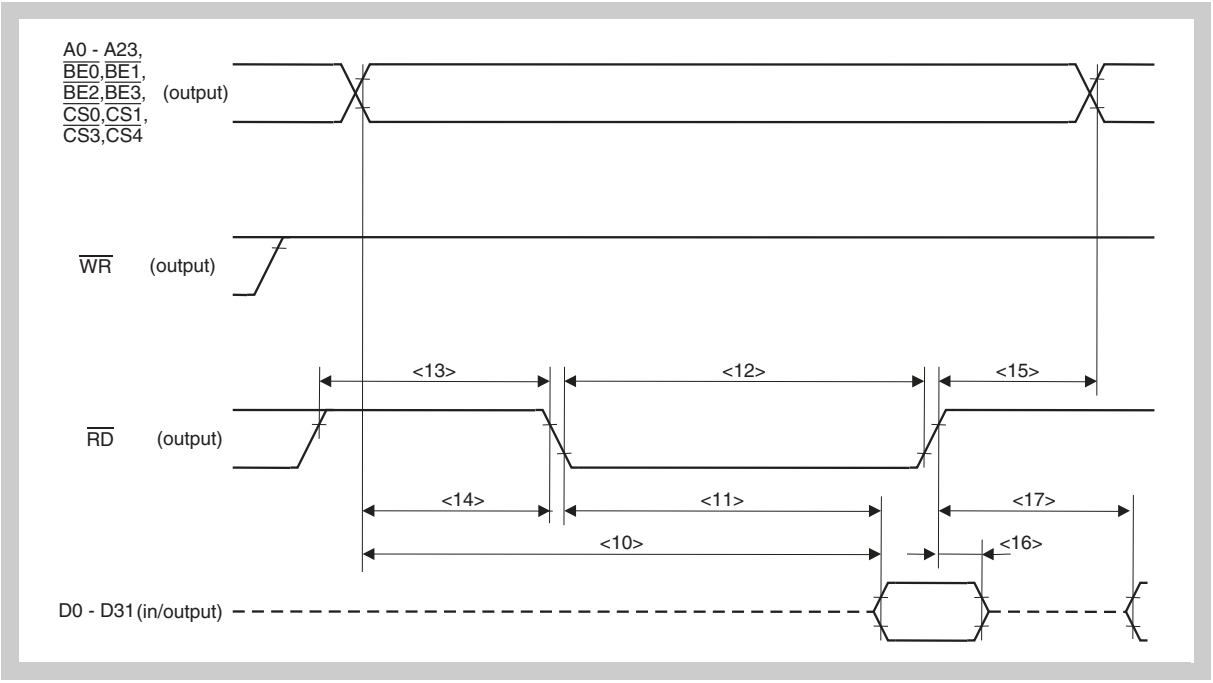


Figure 7-15 SRAM Asynchronous Read Timing

Table 7-18 External Memory Access Asynchronous Write Timing

Parameter	Symbol		Conditions	Min	Max	Unit
Address, $\overline{WR}$ delay time	<20>	T_{DAWR}		$(0.5+W_{AS})T - 4$		ns
$\overline{CSn}$, $\overline{WR}$ delay time	<20a>	T_{DAWR}		$(0.5+W_{AS})T - 4$		ns
$\overline{BEn}$, $\overline{WR}$ delay time	<20b>	T_{DAWR}		$(0.5+W_{AS})T - 4$		ns
Address set up (vs. $\overline{WR}\uparrow$)	<21>	T_{SAWR}		$(1.5+W_T)T - 4$		ns
$\overline{WR}$ address delay time	<22>	T_{DWRA}		$(0.5+i)T - 8$		ns
$\overline{WR}$ $\overline{CSn}$ delay time	<22a>	T_{DWRA}		$(0.5+i)T - 8$		ns
$\overline{WR}$ High level width	<23>	T_{WWRH}		$(1+ i +W_{AS})T - 12$		ns
$\overline{WR}$ Low level width	<24>	T_{WWRL}		$(1+W_D)T - 8$		ns
Data output set up time D0-15 (vs. $\overline{WR}\uparrow$)	<25>	T_{SODWR}		$(1.5+W_T)T - 10$		ns
Data output hold time D0-D15 (vs. $\overline{WR}\uparrow$)	<26>	T_{HWROD}		0.5iT + 2		ns
Data output set up time D16-31 (vs. $\overline{WR}\uparrow$)	<25>	T_{SODWR}		$(1.5+W_T)T - 15$		ns
Data output hold time D16-D31 (vs. $\overline{WR}\uparrow$)	<26>	T_{HWROD}		0.5iT + 2		ns

Note T: $1 / f_{CPU}$ (= frequency of system clock)
i: Number of idle states specified by BCC register
W_T: Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS}: Number of waits specified by ASC register
W_D: Number of waits specified by DWC1, DWC2 register

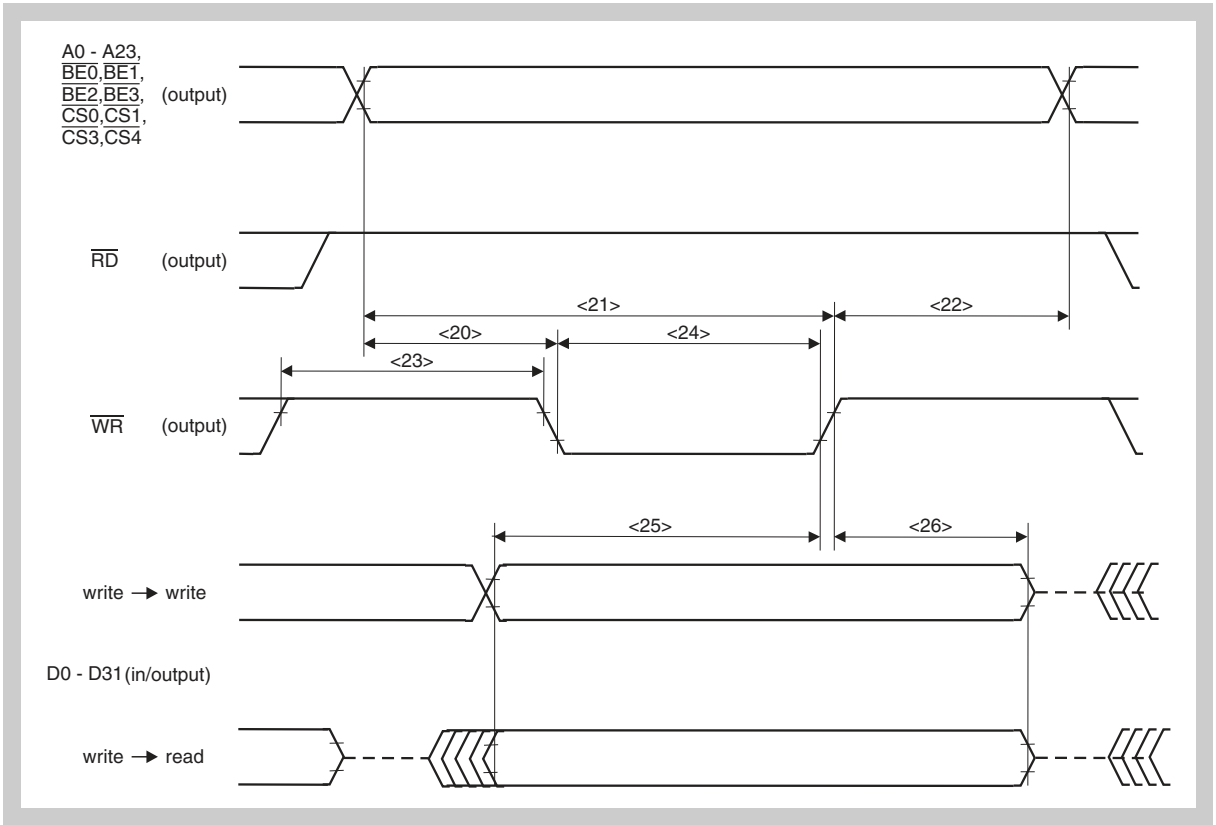


Figure 7-16 SRAM Asynchronous Write Timing

7.7.2 Synchronous Bus Timing

Conditions

T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V (if used as ext. mem. I/F, DV_{DD5} = 3.0 V ~ 5.5 V otherwise),
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 3.6 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = MV_{SS5} = 0 V
Output pin load capacitance: C_L = 50pF

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 7-19 External Memory Access Synchronous Read Timing

Parameter	Symbol		Conditions	Min	Max	Unit
BCLK cycle time	<90>	T_{BCYC}		28		ns
BCLK low	<91>	T_{BH}		7.1		ns
BCLK high	<92>	T_{BL}		7.1		ns
A0-23 Hold time from BCLK↓	<93>	T_{HAD}		5		ns
A0-23 Setup time to BCLK↓	<94>	T_{HSAD}		8		ns
CSx Hold time from BCLK↓	<95>	T_{HCS}		5		ns
CSx Setup time to BCLK↓	<96>	T_{SCS}		8		ns
RD↓ after BLCK↑ Hold	<97>	T_{HRDF}		5		ns
RD↓ to BLCK↑ setup	<98>	T_{SRDF}		6		ns
RD↑ after BLCK↓ Hold	<99>	T_{HRDR}		5		ns
RD↑to BLCK↓ setup	<100>	T_{SRDR}		6		ns
Delayed RD↑ after BLCK↑ Hold	<99a>	T_{HRDRD}		5		ns
Delayed RD↑ to BLCK↑ setup	<100a>	T_{SRDRD}		6		ns
Data input set up time D0-15 (vs. BCLK↑)	<101>	T_{SRDID}		26		ns
Data input set up time D16-31 (vs. BCLK↑)	<101a>	T_{SRDIDa}		31		ns
Data input hold time D0-15 (vs. BCLK↑)	<102>	T_{HRDID}		-11		ns
Data input hold time D16-31 (vs. BCLK↑)	<102a>	T_{HRDIDa}		-11		ns
WAIT input set up time [a] (vs. BCLK↑)	<103>	T_{SWK}		26		ns
WAIT input hold time (vs. BCLK↑)	<104>	T_{HWK}		-11		ns

a) The setup and hold time for WAIT may be violated, but if the device reacts with an additional wait state is than not defined.

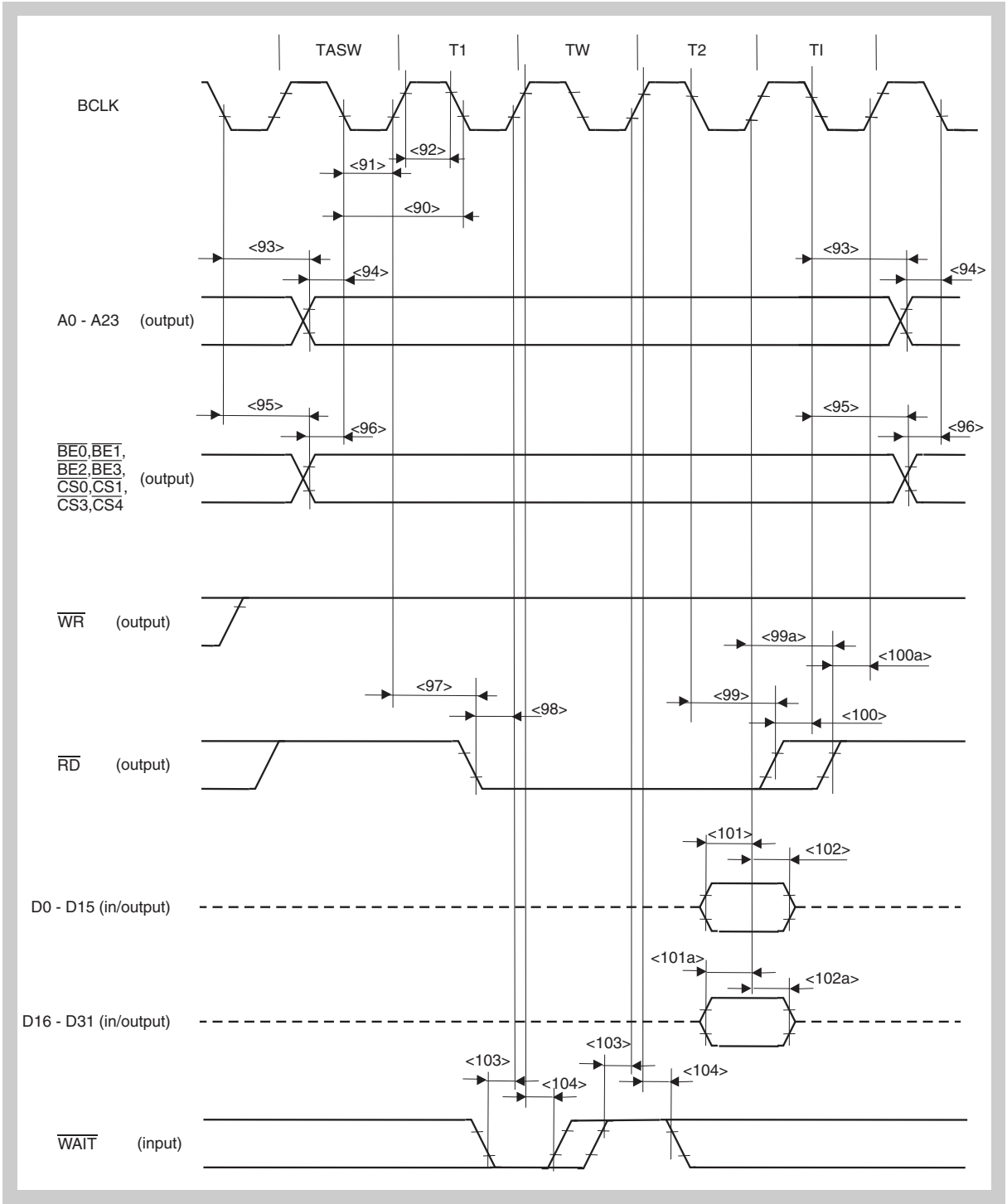


Figure 7-17 External Memory Access Synchronous Read Timing

Table 7-20 External Memory Access Synchronous Write Timing

Parameter	Symbol		Conditions	Min	Max	Unit
BCLK cycle time	<110>	T_{BCYC}		28		ns
BCLK low	<111>	T_{BH}		7.1		ns
BCLK high	<112>	T_{BL}		7.1		ns
A0-23 Hold time from BCLK↓	<113>	T_{HAD}		5		ns
A0-23 Setup time to BCLK↓	<114>	T_{HSAD}		8		ns
CSx, BEx Hold time from BCLK↓	<115>	T_{HCS}		5		ns
CSx, BEx Setup time to BCLK↓	<116>	T_{SCS}		8		ns
WR↓ after BLCK↑ Hold	<117>	T_{HWRF}		5		ns
WR↓ to BLCK↑ setup	<118>	T_{SWRF}		8		ns
WR↑ after BLCK↓ Hold	<119>	T_{HWRR}		5		ns
WR↑ to BLCK↓ setup	<120>	T_{SWRR}		8		ns
Data output set up time D0-15 (vs. BCLK↑)	<121>	T_{SWDO}		-7	7	ns
Data output set up time D16-31 (vs. BCLK↑)	<121a>	T_{SWDOa}		-7	11	ns
Data output hold time D0-15 (vs. BCLK↑)	<122>	T_{HWDO}		-7	7	ns
Data output hold time D16-31 (vs. BCLK↑)	<122a>	T_{HWDOa}		-7	11	ns
WAIT input set up time[a] (vs. BCLK↑)	<123>	T_{SWK}		26		ns
WAIT input hold time (vs. BCLK↑)	<124>	T_{HWK}		-11		ns

a) The setup and hold time for WAIT may be violated, but if the device reacts with an additional wait state is than not defined.

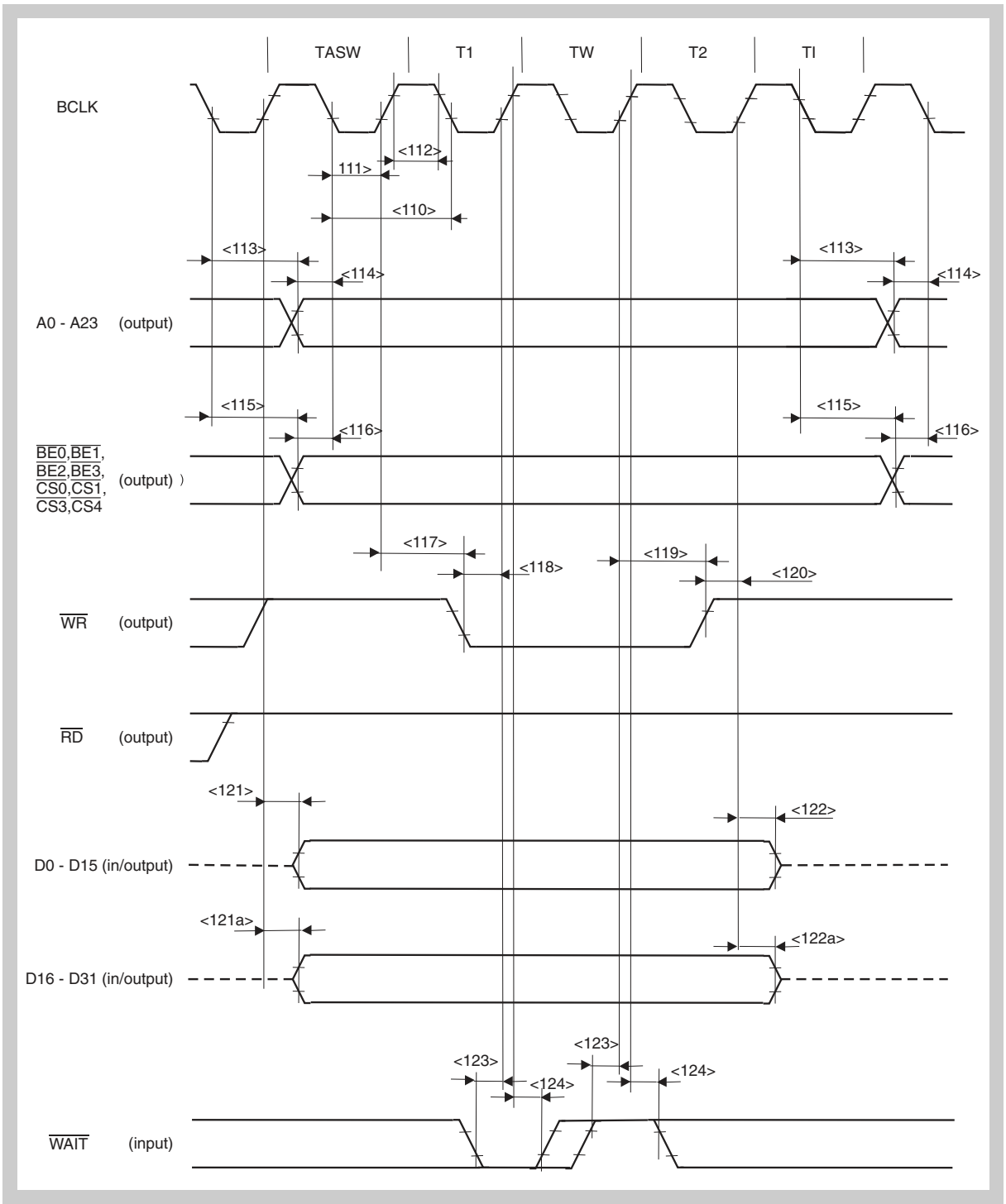


Figure 7-18 External Memory Access Synchronous Write Timing

Chapter 8 Analog Functions

8.1 A/D Converter

The number of available analog input channels depends on the device:

- µPD70F3427, µPD70F3426A, µPD70F3425, µPD70F3424: 16 channels input P70..P715.
- µPD70F3423, µPD70F3422, µPD70F3421: 12 channels input P70..P711.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 8-1 A/D Converter Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution	-			10		Bit
Reference voltage	AVREF		AV_{SS}		AV_{DD}	V
Overall error [a]	-	$AV_{SS} \le AIN \le AV_{REF}$, $4.5V \le (AV_{REF} = AV_{DD}) \le 5.5V$			+/- 3.5	LSB
	-	$AV_{SS} \le AIN \le AV_{REF}$, $3.5V = AV_{REF}$, $4.0V \le AV_{DD} \le 5.5V$			+/- 10	LSB
Integral non linearity error	INL	$AV_{SS} \le AIN \le AV_{REF}$, AV_{DD} - 0.5 V $\le AV_{REF}$, 4.0 V $\le AV_{REF}$, $4.0V \le AV_{DD} \le 5.5V$			2	LSB
Additional error due to disturbance by digital read of P70..P715 [b]	DRERR				1	LSB
Conversion time [c]	T_{CONV}		3.88		15.50	µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analogue supply current	I_{AVDD}				10	mA
Analog input equivalent circuit resistanceb)	R_{INA}		0.3		2.55	kΩ
Analog input equivalent circuit capacitanceb)	C_{INA}		4.0		8.0	pF

Table 8-1 A/D Converter Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analogue supply current	I_{AVDD}				10	mA
Reference voltage supply current [d]	I_{AVREF}				350	µA

a) Quantization error of ±0.5 LSB is not included
b) This value is not tested during production.
c) T_{CONV} depends on register setting
d) The reference current is mainly a transient current that is influenced by the conversion time. The given value is the maximum value. Value is not tested during production.

8.2 Power On Clear

Conditions T_A = -40°C ~ +85°C,
V_{DD5} = 0 ~ 5.5 V,
V_{SS} = 0 V

Table 8-2 Power On Clear Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Voltage	V_{IP}		3.2	3.35	3.5	V
Detection time [a]	T_{DETP}	V_{DD5} slope > 25mV/µs			2	µs

a) Not tested in production.

Note
1. The POC ensures that the devices stops operation (RESET condition) when the device is outside the operation voltage range, under the condition that the supply voltage slope on V_{DD5} is ≤ 25mV/µs.
2. Full device operation is only available, when the supply voltage is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage dropps below the given max threshold voltage.

8.3 Voltage Comparator

The voltage comparator is supplied by A_{VDD}.

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 8-3 Voltage Comparator Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Voltage (calibrated)	V_{IV}		1.73 -0.065	1.73	1.73 +0.065	V
Detection Time [a]	T_{DETV1}	slope = 50mV/µs			2	µs
	T_{DETV2}	step = 100mV, overdrive = 5mV			2	µs
Power-On Stabilization Time[b]	T_S				2	ms

a) Not tested in production.
b) That time must be passed after having enabled a voltage-comparator (Set VCEn bit) and before being able to read the correct status of the concerned voltage-comparator status flag (VCFn).

Chapter 9 Flash Memory

9.1 Basic Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 9-1 Memory Operation Characteristics

Parameter	Symbol	Device	Min	Typ	Max [a]	Unit
Operation Frequency	f_{CPU}	µPD70F3427, µPD70F3426A, µPD70F3425, µPD70F3424	32k		64M	Hz
		µPD70F3423, µPD70F3422, µPD70F3421	32k		24M	Hz

a) The above maximum operation frequency specification lists the center frequency of the SSCG. The maximum dithering range of the SSCG is assured for this center frequency.

9.2 Flash Memory Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 4.5 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note
1. Refer to *"Power On Clear" on page 81* for further functional restriction.
2. The values given in Table 9-2 are valid for a CPU frequency of 24MHz and 32MHz.

Table 9-2 Flash Memory Selfprogramming Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Number of Rewrites	C_{WRT}					1000	times
Data retention	t_{RET}			15			years
Blank Check Time[a]	t_{IVBL}		f_{CPU} = 24MHz		570	570	µs
			f_{CPU} = 32MHz		450	450	µs
Erase Time	t_{IERT4k}	One memory block (4k)[b]	f_{CPU} = 24MHz		13	130	ms
			f_{CPU} = 32MHz				ms
	$t_{IERT256k}$	64 memory blocks (256k)	f_{CPU} = 24MHz		29	290	ms
			f_{CPU} = 32MHz				ms
Write Time	t_{IWRT}	Write two words[c]	f_{CPU} = 24MHz		520	1120	µs
			f_{CPU} = 32MHz		300	900	µs
	t_{IWRT4k}	One memory block (4k)[d]	f_{CPU} = 24MHz		48	348	ms
			f_{CPU} = 32MHz		45	345	ms
Verify Time	t_{IVRT4k}	One memory block (4k)	f_{CPU} = 24MHz		16	20	ms
			f_{CPU} = 32MHz				ms
	$t_{IVRT256k}$	64 memory block (256k)	f_{CPU} = 24MHz		1.1	1.3	s
			f_{CPU} = 32MHz				
Erase/Write Current [e]	I_{DDFL}				1	3	mA
Programming Temperature[f]	t_{PRG}			-40		+65	°C
		maximum power dissipation 0.8W		-40		+85	°C

a) Blank check of one memory block (4 kB).
b) Erase of one memory block (4kB).
c) The corresponding library call is configured for 2 word-write per call.
d) The corresponding library call uses a 4kB source buffer.
e) Additional current that is only needed during erase or write of flash.
f) The power dissipation may be reduced by disabling some functionality or reducing the CPU operation speed.

9.3 Special Conditions for End-of-Line Programming

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 4.8 V ~ 5.15 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

(1) Flash Memory End-of-Line Programming Characteristics (PG-FP4)

Table 9-3 Flash Memory End-of-Line Programming Characteristics (PG-FP4: CSI)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	All	W/E cycles ≤ 5		1	1	s
Erase Time [a]	t_{IERT}				1	1	s
Write Time [b]	t_{IWRT}	µPD70F3427, µPD70F3426A, µPD70F3425			20	32	s
		µPD70F3424, µPD70F3423			10	16	s
		µPD70F3421			5	8	s
Verify Time	t_{IVRT}	µPD70F3427, µPD70F3426A, µPD70F3425			16	20	s
		µPD70F3424, µPD70F3423			8	10	s
		µPD70F3421			5	7	s

a) Erase of all flash-memory blocks (0 .. 255)
b) Write of complete flash area.

Table 9-4 Flash Memory End-of-Line Programming Characteristics (PG-FP4: UART)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	All	W/E cycles ≤ 5		1	1	s
Erase Time [a]	t_{IERT}				1	1	s
Write Time [b]	t_{IWRT}	µPD70F3426A			230	300	s
		µPD70F3427, µPD70F3425			115	150	s
		µPD70F3424, µPD70F3423			60	80	s
		µPD70F3421			30	40	s
Verify Time	t_{IVRT}	µPD70F3426A			230	300	s
		µPD70F3427, µPD70F3425			115	150	s
		µPD70F3424, µPD70F3423			60	80	s
		µPD70F3421			30	40	s

a) Erase of all flash-memory blocks (0 .. 255)
b) Write of complete flash area.

(2) Flash Memory End-of-Line Programming Characteristic (Flash-Selfprogramming)

Note The values given in Table 9-5 are valid for a CPU frequency of 24MHz and 32MHz.

Table 9-5 Flash Memory End-of-Line Programming Characteristics (Flash-Selfprogramming)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Blank Check[a]	t_{IVBL}	W/E cycles ≤ 5	f_{CPU} = 24MHz		570	570	µs
			f_{CPU} = 32MHz		450	450	µs
Erase Time one memory block (4k)	t_{IERT4k}		f_{CPU} = 24MHz		13	52	ms
			f_{CPU} = 32MHz				
Erase Time 64 memory blocks (256k)	$t_{IERT256k}$		f_{CPU} = 24MHz		29	116	ms
			f_{CPU} = 32MHz				
Write Time (Write two words)[b]	t_{IWRT}		f_{CPU} = 24MHz		520	1120	µs
			f_{CPU} = 32MHz		300	900	µs
Write Time (One memory block 4k)[c]	t_{IWRT4k}		f_{CPU} = 24MHz		48	198	ms
			f_{CPU} = 32MHz		45	195	ms
Verify Time (One memory block 4k)	t_{IVRT4k}		f_{CPU} = 24MHz		16	20	ms
			f_{CPU} = 32MHz				
Verify Time (64 memory blocks 256k)	$t_{IVRT256k}$		f_{CPU} = 24MHz		1.1	1.3	s
			f_{CPU} = 32MHz				

a) Blank check of one memory block (4kB).
b) The corresponding library call is configured for 2 word per call.
c) The corresponding library call uses a 4kB source buffer.

9.4 Serial Write Operation Characteristics

Conditions T_A = -40°C ~ +85°C,
DV_{DD5} = 3.0 V ~ 5.5 V, BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
MV_{DD5} = 3.0 V ~ 5.5 V (µPD70F3427 only),
V_{DD5} = 4.5 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = DV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V
MV_{SS5} = 0 V (µPD70F3427 only)

Note Refer to *"Power On Clear" on page 81* for further functional restriction.

Table 9-6 Flash Memory AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FLMD0 setup time to rising edge of $\overline{\text{RESET}}$	t_{MDSET}		2			ms
Count start time from rising edge of $\overline{\text{RESET}}$ to FLMD0	t_{RFCF}		0.8			ms
Count ending time from end of t_{RFCF} to FLMD0	t_{COUNT}		20			ms
FLMD0 counter High/Low level width	t_{CH},t_{CL}		10		100	µs
FLMD0 counter rise/fall time	t_R,t_F				50	ns

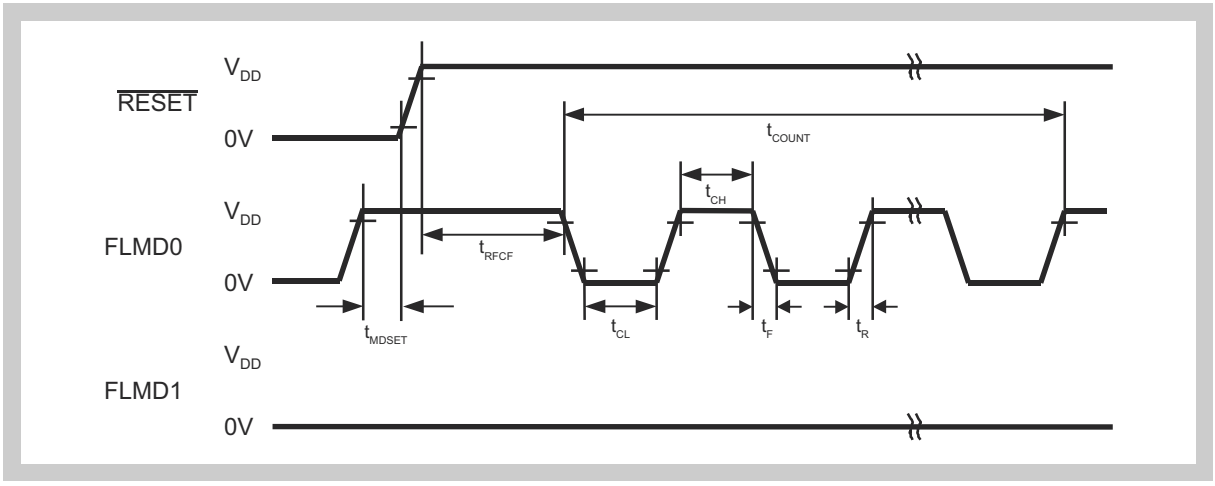


Figure 9-1 Flash Memory Timing

Note FLMD1 is a shared function of the P07 pin.

Chapter 10 Special Conditions for Device Operation at extended Operating Temperature Range

Condition **T_A = -40°C ~ +105°C**

Caution For any device's operation within the extended operating temperature range (T_A = -40°C ~ +105°C), the device's total power consumption must be reduced. The following tables within this chapter describe additional device conditions securing the requested decrease of the device's power consumption.

In case any device may operate within the extended operating temperature range (T_A = -40°C ~ +105°C) all of the below mentioned conditions must never be exceeded at any time.

All of the below mentioned device conditions must be applied in addition to any other parameter that is described within this document.

Note The operation conditions for an extended temperature range (T_A = -40°C ~ +105°C) mentioned in this chapter are valid for all parameters which were described within this document.
In all conditions in this document the normal temperature range (T_A = -40°C ~ +85°C) is replaced by the extended temperature range of T_A = -40°C ~ +105°C in case the operating conditions mentioned in this chapter are applied.

(1) µPD70F3427

Condition 1 T_A = -40°C ~ +105°C
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 1.0 W
Duration: 15000 hours
V_{SS5} = 0V

Condition 2 T_A = -40°C ~ +105°C
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-1 Absolute maximum ratings currents for special conditions (µPD70F3427)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 48 MHz	70	mA
Output current high		I_{OHA}			-70	mA
Number of active stepper motor drivers					4	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 6, 7, 8	f_{SYS}= 24 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper motor drivers					6	

(2) µPD70F3426A

Condition 1 T_A = -40°C ~ +105°C
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 1.0 W
Duration: 15000 hours
V_{SS5} = 0V

Condition 2 T_A = -40°C ~ +105°C,
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-2 Absolute maximum ratings currents for special conditions (µPD70F3426A)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 48 MHz	40	mA
Output current high		I_{OHA}			-40	mA
Number of active stepper motor drivers					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 24 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper motor drivers					6	

(3) µPD70F3425

Condition 1 T_A = -40°C ~ +105°C
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 0.9 W
Duration: 15000 hours
V_{SS5} = 0V

Condition 2 T_A = -40°C ~ +105°C
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-3 Absolute maximum ratings currents for special conditions (µPD70F3425)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 48 MHz	135	mA
Output current high		I_{OHA}			-135	mA
Number of active stepper motor driver					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 32 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper motor driver					6	

(4) µPD70F3424

Condition 1 T_A = -40°C ~ +105°C
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 0.88 W
Duration: 15000 hours
V_{SS5} = 0V

Condition 2 T_A = -40°C ~ +105°C
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Table 10-4 Absolute maximum ratings currents for special conditions (µPD70F3424)

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 48 MHz	180	mA
Output current high		I_{OHA}			-180	mA
Number of active stepper motor driver					6	
Output current low	All pins	I_{OLA}	Sum of Groups 1, 2, 3, 5, 7, 8	f_{SYS}= 32 MHz	250	mA
Output current high		I_{OHA}			-250	mA
Number of active stepper motor driver					6	

(5) µPD70F3421, µPD70F3422, µPD70F3423

Condition 1 T_A = -40°C ~ +105°C
Operation Modes: RUN, HALT, IDLE
Power dissipation: < 0.86 W
Duration: 15000 hours
V_{SS5} = 0V

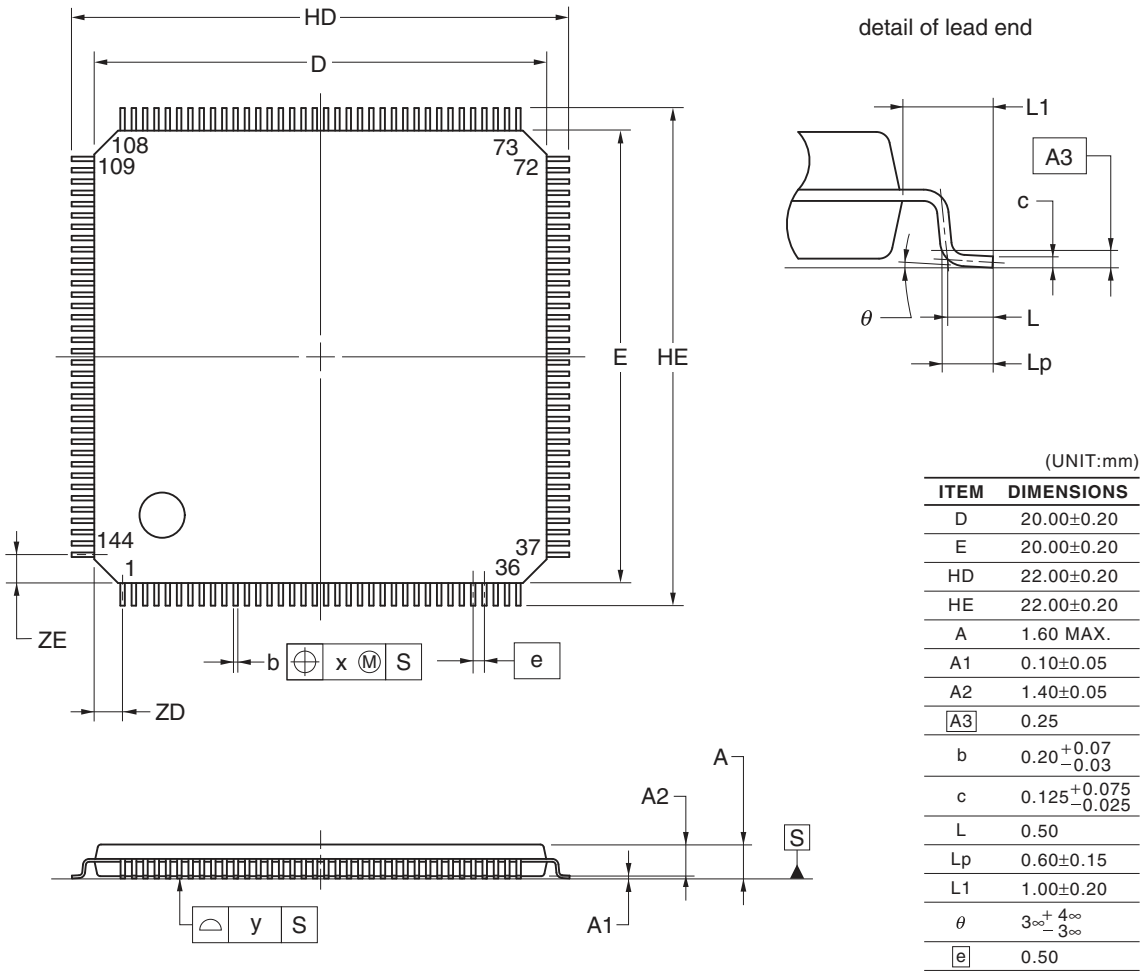
Condition 2 T_A = -40°C ~ +105°C
Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation
Power dissipation: < 0.5W
Duration: 15 years
V_{SS5} = 0V

Note No additional condition must be fulfilled.

Chapter 11 Package

11.1 Package of µPD70F3426AGJ, µPD70F3425GJ, µPD70F3424GJ, µPD70F3423GJ, µPD70F3422GJ, µPD70F3421GJ

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



(UNIT:mm)

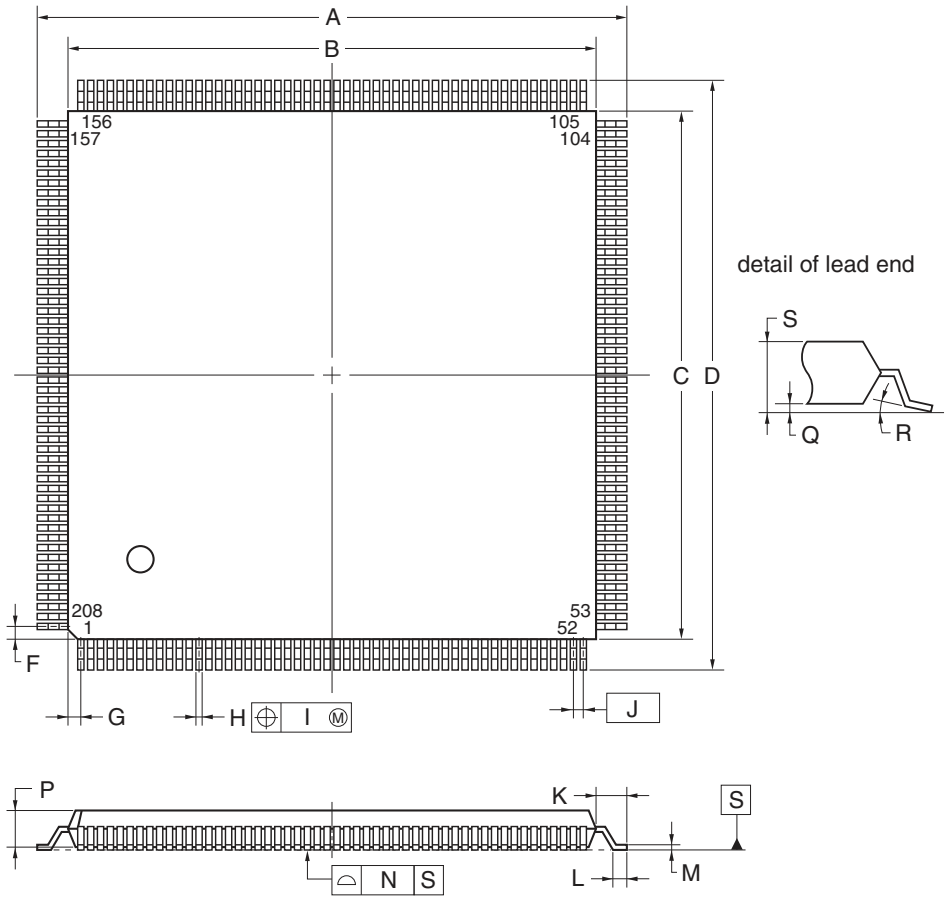
ITEM	DIMENSIONS
D	20.00±0.20
E	20.00±0.20
HD	22.00±0.20
HE	22.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P144GJ-50-GAE-2

Figure 11-1 Package Drawing of µPD70F3426AGJ, µPD70F3425GJ, µPD70F3424GJ, µPD70F3423GJ, µPD70F3422GJ, µPD70F3421GJ

11.2 Package of µPD70F3427GD

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	30.6±0.2
B	28.0±0.2
C	28.0±0.2
D	30.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	3.2±0.1
Q	0.4±0.1
R	5°±5°
S	3.8 MAX.

P208GD-50-LML,MML,SML,WML-7

Figure 11-2 Package Drawing µPD70F3427GD

11.3 Thermal Resistance

Table 11-1 Thermal resistance of V850E/Dx3 products

Product Code	Junction to Ambient	Junction to Case	Junction to Lead	Lead	Unit
	R_{THJA}, Airflow = 0m/s	R_{THJC}	R_{THJL}	R_{THLL}	
µPD70F3421GJ(A)-GAE-QS-AX	43.26	7.53	22.49	0.22	K/W
µPD70F3422GJ(A)-GAE-QS-AX	43.26	7.53	22.49	0.22	K/W
µPD70F3423GJ(A)-GAE-QS-AX	43.26	7.53	22.49	0.22	K/W
µPD70F3424GJ(A)-GAE-QS-AX	43.26	7.53	22.49	0.22	K/W
µPD70F3425GJ(A)-GAE-QS-AX	42.89	6.68	21.08	0.21	K/W
µPD70F3426AGJ(A)-GAE-QS-AX	41.66	5.33	19.77	0.19	K/W
µPD70F3427GD(A)-LML-QS-AX	38.36	10.39	22.99	0.43	K/W

Note Maximum junction temperature T_{Jmax} = 150°C

Chapter 12 Recommended Soldering Conditions

12.1 Description of Recommended Conditions

The recommended soldering conditions by item are indicated by a combination of the soldering process, peak temperature, baking time, and exposure limit all abbreviated as shown below.

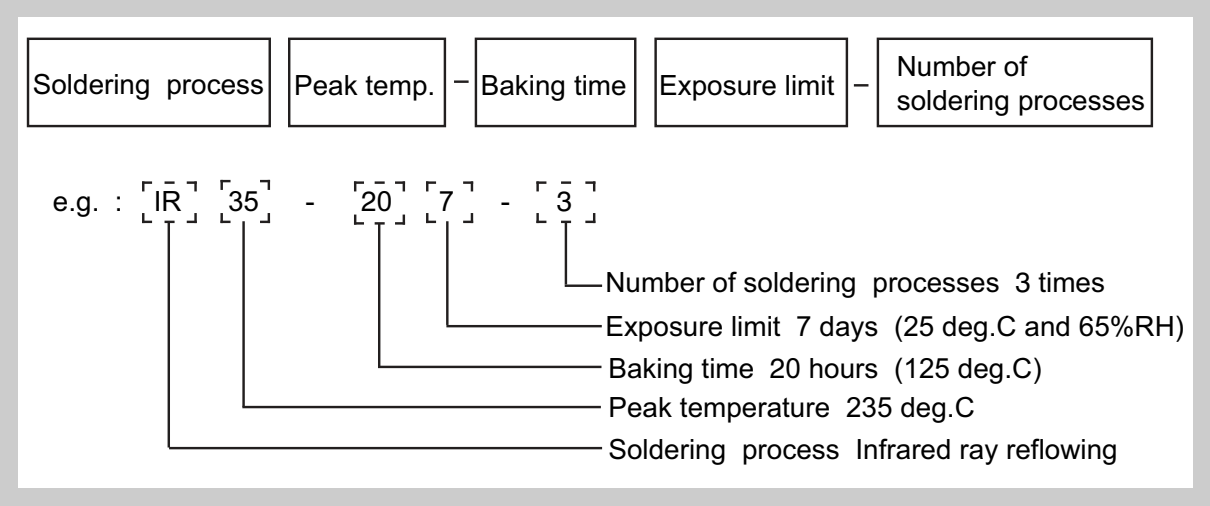


Figure 12-1 Soldering conditions indication

12.1.1 Soldering process

The soldering process is indicated by the following symbols:

Soldering process	Symbol
Infrared Reflow Soldering	IR
Vapour Phase Soldering	VP
Wave Soldering	WS

12.1.2 Peak temperature

The peak temperature is indicated by the two least significant digits (two characters) of the peak value. The peak temperature of the VPS and the infrared ray reflowing process is indicated by the package surface temperature. The wave soldering is indicated by the solder temperature.

Peak temperature	Symbol
215 deg.C	15
220 deg.C	20
230 deg.C	30
235 deg.C	35
260 deg.C	60

12.1.3 Baking time

The baking time is indicated by the following symbols:

Baking time (stored at 125 deg.C)	Symbol
No baking required (0 hours)	00
10 hours	10
16 hours	16
20 hours	20
36 hours	36

12.1.4 Exposure limit

Exposure limit means the maximum limit with which the device can be soldered without problem after unpack. The limit is indicated by the following symbols:

Exposure limit (Temperature 25 deg.C and humidity 65%RH or less)	Symbol
One day (24 hours)	1
Two days (48 hours)	2
Three days (72 hours)	3
Seven days (168 hours)	7
Eight hours	B
Twelve hours	C

12.1.5 Number of soldering process

Number of soldering process is indicated by the following symbols:

Number of soldering processes	Symbol
Once	1
Twice	2

12.2 Recommended Conditions of IR60-207-3

The following is recommended soldering conditions. (Moisture sensitive device)

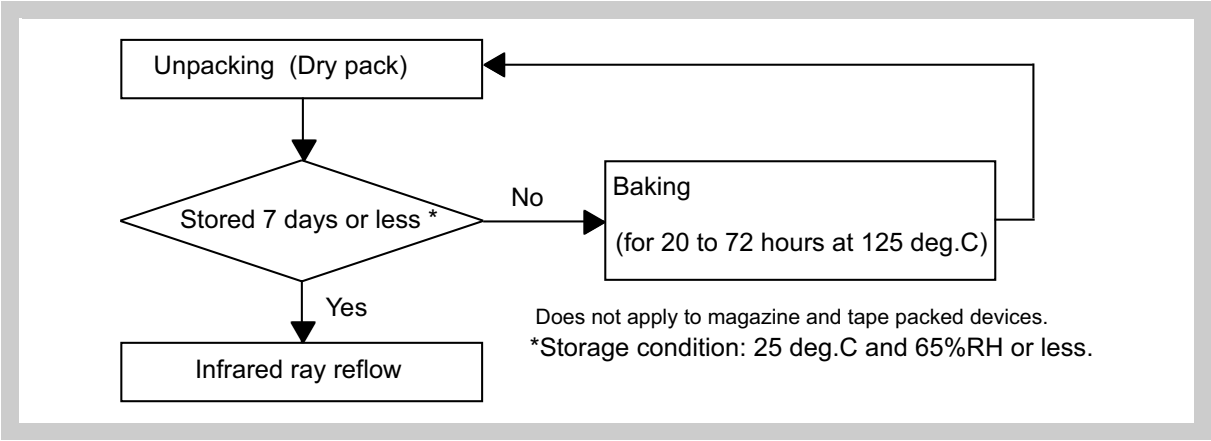


Figure 12-2 Recommended Handling of Unpacked Devices

Peak temperature:	260 deg.C or below (Package's surface temperature)
Reflow time:	60 seconds or less (at 220 deg.C)
Maximum number of reflow processes:	3 times
Exposure limit (Store until the final reflow process starts):	7 days or less
Flux:	Rosin flux containing small amount of chlorine (Flux with a maximum chlorine content of 0.2 Wt% is recommended.)

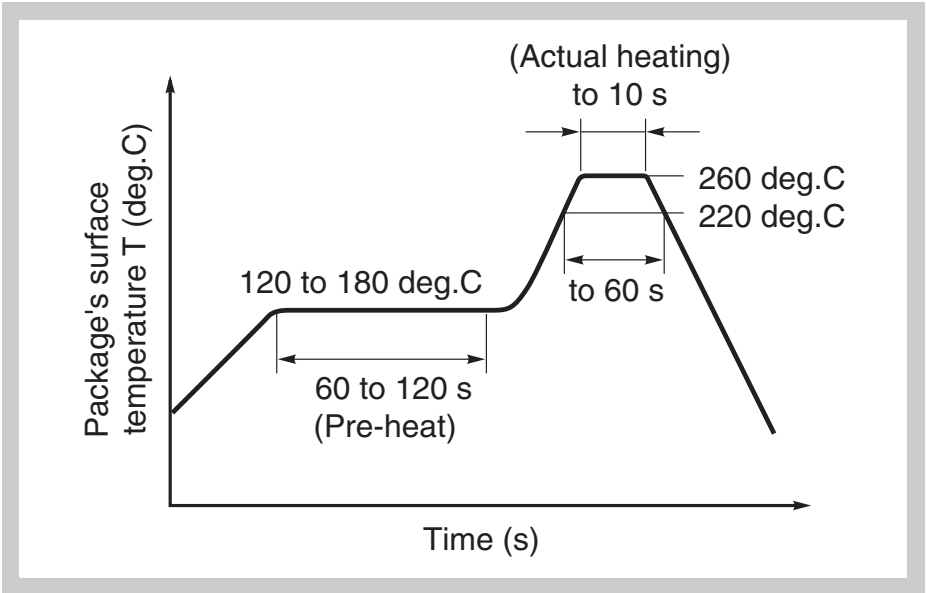


Figure 12-3 Infrared Ray Reflow Temperature Profile

Appendix A Revision History

Item	Date published	Document No.	Comment
1	Jul 5, 2005	EASE-PL-8007-0V1	First release of this document
2	Aug 3, 2005	EASE-PL-8007-0V2	Second release of this document
3	Dec 13, 2005	EASE-PL-8007-0V3	Update of document
			Overview: - Included the derivatives µPD70F3427, µPD70F3426, µPD70F3422, µPD703422. - Included a note describing the expansion of flash and RAM for the derivative µPD70F3426. - Included the LCD I/F to the reduced peripheral set.
			DC characteristics: - Added typical operating current for 48MHz. - Changed VCOMP0/1 to VCMP0/1. - Corrected the table 6-15.
			Pinout Information: - Included the Pinconfiguration of the new derivatives µPD70F3427 and µPD70F3426. - Introduced the pin-group 6 representing the external memory-interface of the new derivative µPD70F3427. - Introduced the pin-group 8 representing the voltage comparator input pins.
			Absolute Maximum Ratings: - Included the DJ3 derivatives µPD70F3427, µPD70F3426, µPD70F3422, µPD703422. - Included the concerned parameters for the µPD70F3427's memory interface.
			General Characteristics: - Included the concerned information regarding the external memory interface of the derivative µPD70F3427.
			Operation Conditions: - Included the DJ3 derivatives µPD70F3427 and µPD70F3426 for the corrseponding CPU clock frequencies 32 MHz and 48 MHz.
			DC-Characteristics: - Included the DJ3 derivatives µPD70F3427 and µPD70F3426. - Separated the characteristics of pin-group 3 for µPD70F3427 and the remaining devices. - Included the characteristics of pin-group 6 for the device µPD70F3427. - Included the supply-currents for added derivatives µPD70F3427 and µPD70F3426. - Added a note regarding current limit function of the derivative µPD70F3427. - Review of chapter "LCD Common and Segment Lines".
			AC-Characteristics: - Included the derivatives µPD70F3427 and µPD70F3426. - Included the external memory access specification for the derivative µPD70F3427.
			Analog Functions: - POC characteristics. Included a note.

Item	Date published	Document No.	Comment
3	Dec 13, 2005	EASE-PL-8007-0V3	Flash Memory: - Included the derivatives µPD70F3427 and µPD70F3426.
			Package: - Included the derivatives µPD70F3427 and µPD70F3426 - Added the package drawings for the derivatives µPD70F3427 and µPD70F3426.
4	Sep 4, 2006	EASE-PL-8007-1V0	Redefinition of that document "Electrical Target Specification" to "Preliminary Data Sheet".
			Family Overview: - Updated operating clock.
			Operation Conditions: - Update the CPU clock frequencies.
			DC-Characteristics: - Updated the supply-currents for all derivatives. - Completion of table 6-23.
			AC-Characteristics: - Updated the AC-Characteristics for the ext. mem. I/F (µPD70F3427).
5	Jan 18, 2007	EASE-PL-8007-1V1	DC-Characteristics: - Included the values for the LCD split voltages - Updated the supply-currents for the derivatives µPD70F3424, µPD70F3426 and µPD70F3427.
			AC- Characteristics: - CSIB updated and expanded characteristics. - LCD Bus Interface updated. - External memory access updated.
			Analog Functions: - Added the Voltage Comparator Characteristics stabilization time.
			Flash Memory: - Updated parameters for End-of-Line programming. Included parameters for missing derivatives.
			Special Conditions for Device Operation at extended Operating Temperature Range (T_A = -40°C ... +105°C) - Included a new chapter describing the operating conditions when device is operating within the extened operating temperature range.
6	Oct. 29, 2009	U20110EE1V0DS00	Overview: - Updated device list.
			Peripherals: - added Memory interface extention for µPD70F3427GD - added 3rd CAN channel for µPD70F3421/22/23/24/25/27 - added Timer Y (TMY) for all devices - corrected number of voltage comparators from 3 to 2
			Internal RAM: - Increased from 16kbytes to 20kbytes for µPD70F3422GJ
			General Characteristics: - Updated the parameters regarding the SSCG modulation range and frequency. - Added input leakage parameters for pin group 6.

Item	Date published	Document No.	Comment
6	Oct. 29, 2009	U20110EE1V0DS00	DC-Characteristics: - Added injected current specification (Table 6-1) - Removed limitation “CMOS2 and SCHMITT2 are only available on Port P8” (Table 6-2, table 6-3) - Added Schmitt2 and CMOS2 (Table 6-6, table 6-7, table 6-8) - Added ADC Low Voltage Operating Range (Table 6-9) - Extended Schmitt 2 and CMOS2 to whole pingroup 3 (Table 6-10, table 6-11) - Added Definitions for VLCD (Table 6-15) - Added Schmitt2 and CMOS2 (Table 6-16 - DC Characteristics Stepper Motor Driver Input Normal Voltage Operation, table 6-17) - Added Stepper Motor Driver Zeropoint Detection - Reduced “Watch” and “Watch mointored” currents for µPD70F3421/22/23/24/25/26 (Table 6-23, table 6-26, table 6-27) - Added “Additional Supply Current (Operating) during Self-Flash-Programming” (Table 6-24) - Reduced supply currents for µPD70F3427 (Table 6-25) - Added table describing when bias current is flowing. - Added LCD common and segment lines operation current - Stepper motor driver output voltage deviation not tested, but specified by design
			AC Characteristics: - Corrected parameters for the serial clock high- and low-level width. - Corrected min. SIBn setup time in low voltage operation CSIB master mode - Corrected maximum I^2C clock SCL0 - Renamed LCD Bus I/F control modes - Corrected D_{VDD5} range of LCD Bus I/F specification - Updated the characteristics for the ext. mem. I/F. - Added/corrected the characteristics for the mem. I/F’s asynchronous synchronous operation. - Added “i” in calculation for T_{DWRA} (Table 7-18)
			Analog Functions: - Updated A/D Converter parameters - Removed uncalibrated Voltage Comparator trheshold: no user calibration required - Reduced POC Threshold Voltage Max. to 3.5V (Table 8-2) - Added TDETV1 for Voltage Comparator (Table 8-3)
			Flash Memory: - Modified parameters for Flash Memory Characteristics.
			Special Conditions for Device Operation at extended Operating Temperature Range (T_A = -40°C ... +105°C): - Added the whole chapter.
			Package / Pin configuration: - thermal resistances specified - Corrected package code for µPD70F3427 to µPD70F3427GD (was µPD70F3427GJ, chapter 2.1) - Updated pin configuration drawings (chapters 2.1, 2.2, 2.3)
			Absolute maximum ratings - Increased Output currents low (Table 3-2) - Added Power Supply Restrictions (Table 3-3) - Updated parameter for the power dissipation and storage temperature - Corrected symbols of currents

Item	Date published	Document No.	Comment
6	Oct. 29, 2009	U20110EE1V0DS00	Operating Conditions - Added SSCG for IICLK, SPCLK0-1 and SPCLK2-15 (Table 5-2) - Added sub chapter “5.3 AC Load Condition - Single Pin Switching”
			Naming: Changed µPD70F3426 to µPD70F3426A (64MHz)
7	Dec 10, 2010	R01DS0049ED0200	Overview: Replaced product names by product codes
			Analog Functions: - Added integral non linearity error (INL) to A/D converter characteristics
			Package: - Corrected/replaced package drawing of 144 pin plastic QFP (package code GAE instead of UEN)
8	Jun 1, 2011	R01DS0049ED0210	AC Characteristics of Flash Memory changed to more relaxed values (t_{MDSET}, t_{COUNT})

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0

V850E/Dx3 - DJ3/DL3

Renesas Electronics Corporation
R01DS0049ED0210, Rev. 2.10