



# CY54/74FCT373T CY54/74FCT573T

## 8-Bit Latches

### Features

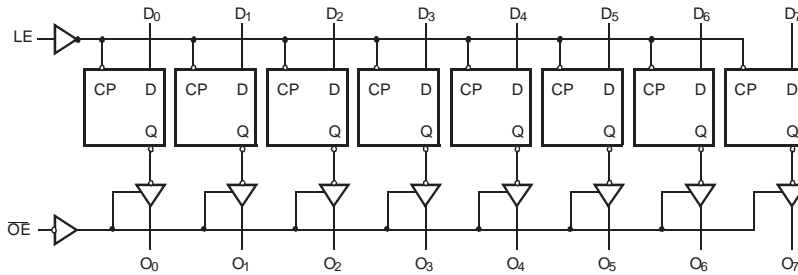
- Function and pinout compatible with FCT, and F logic
- FCT-C speed at 4.2 ns max. (Com'l), FCT-A speed at 5.2 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V
- Matched rise and fall times
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l), 32 mA (Mil)  
Source current 32 mA (Com'l), 12 mA (Mil)

### Functional Description

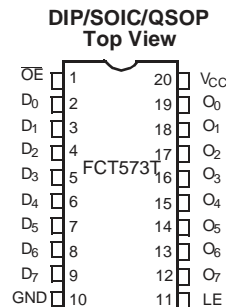
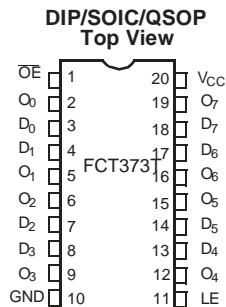
The FCT373T and FCT573T consist of eight latches with three-state outputs for bus organized applications. When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the ( $\overline{OE}$ ) is LOW. When output enable is HIGH, the bus output is in the impedance state. In this mode, data may be entered into the latches. The FCT573T is identical to the FCT373T except for the flow-through pinout, which simplifies board design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

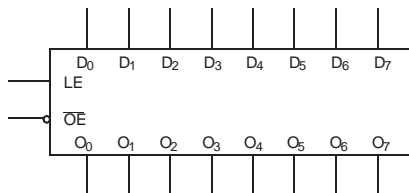
### Logic Block Diagram



### Pin Configurations



### Logic Symbol





**Function Table<sup>[1]</sup>**

Inputs			Outputs
OE	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -65°C to +135°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Output Voltage ..... -0.5V to +7.0V  
 DC Output Current (Maximum Sink Current/Pin) ..... 120 mA  
 Power Dissipation..... 0.5W  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	Com'l	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =32 mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage			2.0			V
V <sub>IL</sub>	Input LOW Voltage					0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs			0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA			-0.7	-1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>				5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V				±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V				±1	μA
I <sub>OZH</sub>	Off State HIGH-Level Output Current	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V				10	μA
I <sub>OZL</sub>	Off State LOW-Level Output Current	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V				-10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V		-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V				±1	μA

**Notes:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = HIGH Impedance  
Q<sub>n</sub> = Previous state of flip flops (Q<sub>n-1</sub>)
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Capacitance<sup>[6]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	6	10	pF
C <sub>OUT</sub>	Output Capacitance	8	12	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	0.1	0.2	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V, f <sub>1</sub> =0, Outputs Open <sup>[8]</sup>	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ =GND, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	0.6	0.12	mA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =10 MHz, $\overline{OE}$ =GND, LE=V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	0.7	1.4	mA
		V <sub>CC</sub> =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =10 MHz, $\overline{OE}$ =GND, LE=V <sub>CC</sub> , V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.0	2.4	mA
		V <sub>CC</sub> =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, $\overline{OE}$ =GND, LE=V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	1.3	2.6 <sup>[11]</sup>	mA
		V <sub>CC</sub> =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =2.5 MHz, $\overline{OE}$ =GND, LE=V <sub>CC</sub> , V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	3.3	10.6 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 I<sub>CC</sub> = Quiescent Current with CMOS input levels  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL inputs HIGH  
 N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
 f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
 f<sub>1</sub> = Input signal frequency  
 N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	FCT373T/FCT573T				FCT373AT/FCT573AT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to O	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to O	2.0	15.0	2.0	13.0	2.0	9.8	2.0	8.5	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	13.5	1.5	12.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	10.0	1.5	7.5	1.5	6.5	1.5	5.5	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time HIGH to LOW D to LE	2.0		2.0		2.0		2.0		ns	9
t <sub>H</sub>	Set-Up Time HIGH to LOW D to LE	1.5		1.5		1.5		1.5		ns	9
t <sub>W</sub>	LE Pulse Width HIGH	6.0		6.0		6.0		5.0		ns	5

Parameter	Description	FCT373CT/ FCT573CT		FCT373DT/ FCT573DT		Unit	Fig. No. <sup>[13]</sup>
		Commercial		Commercial			
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to O	1.5	4.2	1.5	3.8	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to O	2.0	5.5	2.0	4.0	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	5.5	1.5	4.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.0	1.5	4.0	ns	1, 7, 8
t <sub>S</sub>	Set-Up Time, HIGH to LOW D to LE	2.0		1.5		ns	9
t <sub>H</sub>	Set-Up Time, HIGH to LOW D to LE	1.5		1.0		ns	9
t <sub>W</sub>	LE Pulse Width HIGH	5.0		3.0		ns	5

Shaded areas contain preliminary information.

**Note:**

12. Minimum limits are guaranteed but not tested on Propagation Delays.  
 13. See "Parameter Measurement Information" in the General Information section.



**Ordering Information–FCT373T**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT373CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
8.0	CY74FCT373TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT373TDMB	D6	20-Lead (300-Mil) CerDIP	Military

**Ordering Information—FCT573T**

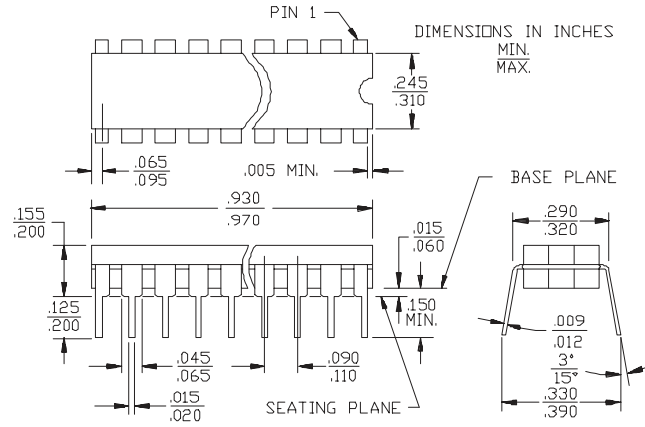
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT573CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT573CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
8.0	CY74FCT573TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT573TDMB	D6	20-Lead (300-Mil) CerDIP	Military

Shaded areas contain preliminary information.

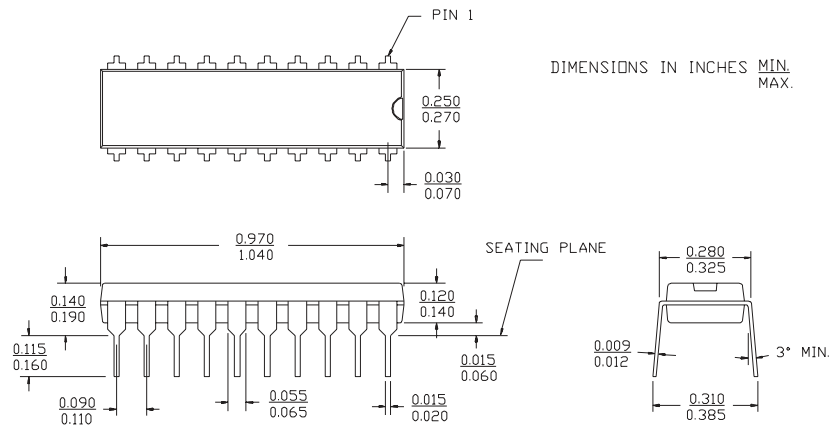
Document #: 38-00272-B

**Package Diagrams**

**20-Lead (300-Mil) CerDIP D6**  
MIL-STD-1835 D-8 Config.A

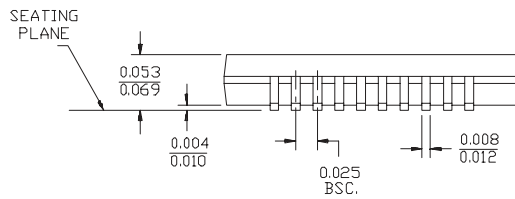
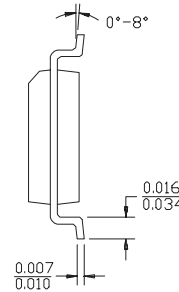
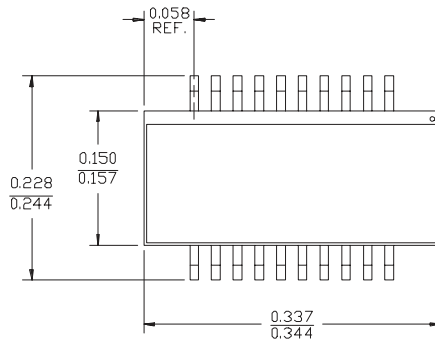


**20-Lead (300-Mil) Molded DIP P5**



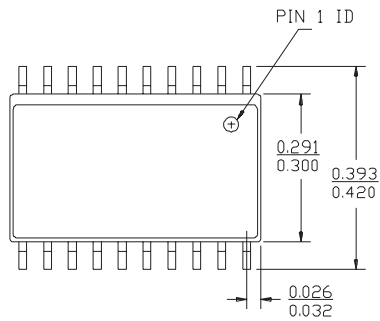
**Package Diagrams** (continued)

**20-Lead Quarter Size Outline Q5**



DIMENSIONS IN INCHES MIN.  
MAX.  
 LEAD COPLANARITY 0.004 MAX.

**20-Lead (300-Mil) Molded SOIC S5**



DIMENSIONS IN INCHES MIN.  
MAX.  
 LEAD COPLANARITY 0.004 MAX.

