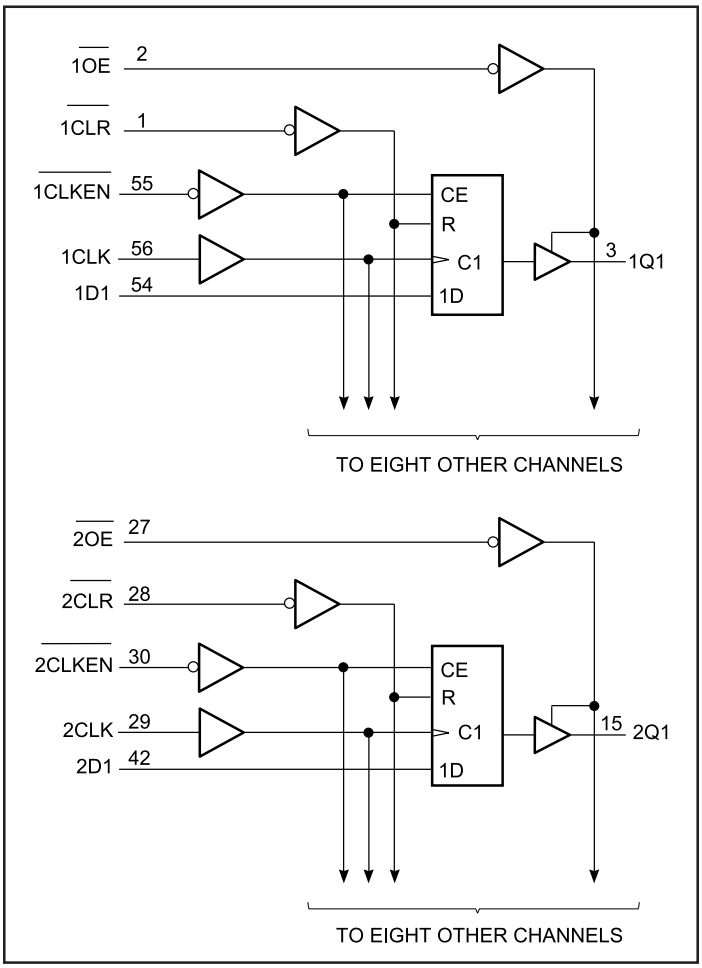
PI74ALVCH16823

18-Bit Bus-Interface Flip-Flop with 3-State Outputs

Product Features

- Designed for low voltage operation, V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-State, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

Logic Block Diagram



Product Description

The 18-bit PI74ALVCH16823 bus-interface flip-flop is designed for 2.3V to 3.6V V_{CC} operation. It features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The PI74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the Clock Enable ($\overline{CLKEN}$) input LOW, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ HIGH disables the clock buffer, thus latching the outputs. Taking the Clear ($\overline{CLR}$) input LOW causes the Q outputs to go LOW independently of the clock.

A buffered Output Enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The Output Enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Product Pin Description

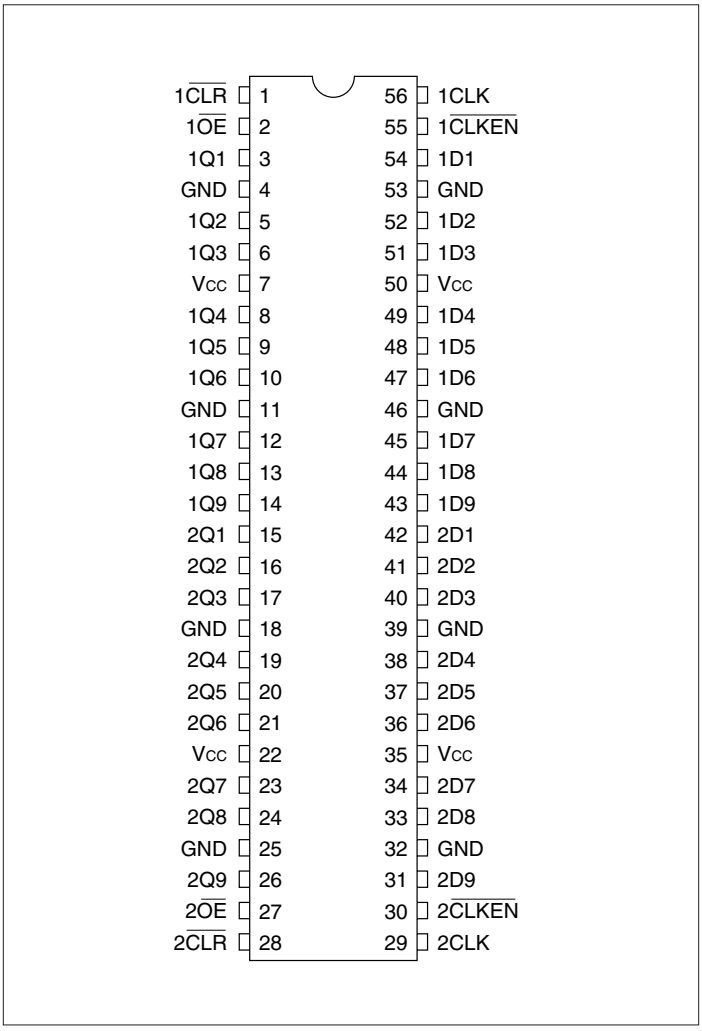
Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{CLR}$	Clear Input (Active LOW)
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table(1)

Inputs					Output
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

Note:
1. H = High Signal Level
   L = Low Signal Level
   X = Irrelevant
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Input Voltage Range, V_{IN}	–0.5V to V_{CC} +0.5V
Output Voltage Range, V_{OUT}	–0.5V to V_{CC} +0.5V
DC Input Voltage	–0.5V to +5.0V
DC Output Current	100 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}[3]	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}[3]	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}[3]	Input Voltage		0		V_{CC}	
V_{OUT}[3]	Output Voltage		0		V_{CC}	
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA, V_{CC} = Min. to Max.	V_{CC} -0.2			
		V_{IH} = 1.7V, I_{OH} = -6mA, V_{CC} = 2.3V	2.0			
		V_{IH} = 1.7V, I_{OH} = -12mA, V_{CC} = 2.3V	1.7			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 2.7V	2.2			
		V_{IH} = 2.0V, I_{OH} = -12mA, V_{CC} = 3.0V	2.4			
		V_{IH} = 2.0V, I_{OH} = -24mA, V_{CC} = 3.0V	2.0			
V_{OL}	Output LOW Voltage	I_{OL} = 100µA, V_{IL} = Min. to Max.			0.2	
		V_{IL} = 0.7V, I_{OL} = 6mA, V_{CC} = 2.3V			0.4	
		V_{IL} = 0.7V, I_{OL} = 12mA, V_{CC} = 2.3V			0.7	
		V_{IL} = 0.8V, I_{OL} = 12mA, V_{CC} = 2.7V			0.4	
		V_{IL} = 0.8V, I_{OL} = 24mA, V_{CC} = 3.0V			0.55	
I_{OH}[3]	Output HIGH Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}[3]	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	

(**Table Continued**)

DC Electrical Characteristics-Continued (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
I_{IN}	Input Current	V_{IN} = V_{CC} or GND, V_{CC} = 3.6V			±5	µA
I_{IN} (HOLD)	Input Hold Current	V_{IN} = 0.7V, V_{CC} = 2.3V	45			
		V_{IN} = 1.7V, V_{CC} = 2.3V	-45			
		V_{IN} = 0.8V, V_{CC} = 3.0V	75			
		V_{IN} = 2.0V, V_{CC} = 3.0V	-75			
		V_{IN} = 0 to 3.6V, V_{CC} = 3.6V			±500	
I_{OZ}	Output Current (3-STATE Outputs)	V_{OUT} = V_{CC} or GND, V_{CC} = 3.6V			±10	
I_{CC}	Supply Current	V_{CC} = 3.6V, I_{OUT} = 0µA, V_{IN} = GND or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.0V to 3.6V One Input at V_{CC} - 0.6V Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	V_{IN} = V_{CC} or GND, V_{CC} = 3.3V		4.5		pF
	Data Inputs			6.5		
C_O	Outputs	V_O = V_{CC} or GND, V_{CC} = 3.3V		7		

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics over Operating Range

Parameters	From (INPUT)	To (OUTPUT)	Conditions	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
				Min.(1)	Max.	Min.(1)	Max.	Min.(1)	Max.	
f_{MAX}				150		150		150		
t_{PD}	CLK	Q	C_L = 50pf R_L = 500Ω	1.0	6.4		5.2	1.0	4.5	ns
	CLR			1.4	6.0		5.2	1.2	4.6	
t_{EN}	$\overline{OE}$			1.0	6.5		5.7	1.0	4.8	
t_{DIS}	$\overline{OE}$			1.8	5.6		4.7	1.3	4.5	

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.

Timing Requirements over Operating Range

Parameters	Description		Conditions	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock Frequency		C_L = 50pF R_L = 500Ω	0	150	0	150	0	150	MHz
t_W	Pulse Duration	CLR LOW		3.3		3.3		3.3		ns
		CLK HIGH or LOW		3.3		3.3		3.3		
t_{SU}	Setup Time	CLR LOW		0.7		0.7		0.8		
		Data LOW		1.4		1.6		1.3		
		Data HIGH		1.1		1.1		1.0		
		CLKEN LOW		1.8		1.9		1.5		
t_H	Hold Time	Data LOW		0.4		0.5		0.5		
		Data HIGH		0.7		0.1		0.8		
		CLKEN LOW		0.2		0.3		0.4		
	Description									
$\Delta t/\Delta v$[(1)]	Input Transition Rise or Fall			0	10	0	10	0	10	ns/V

Notes:
1. Recommended operating conditions.

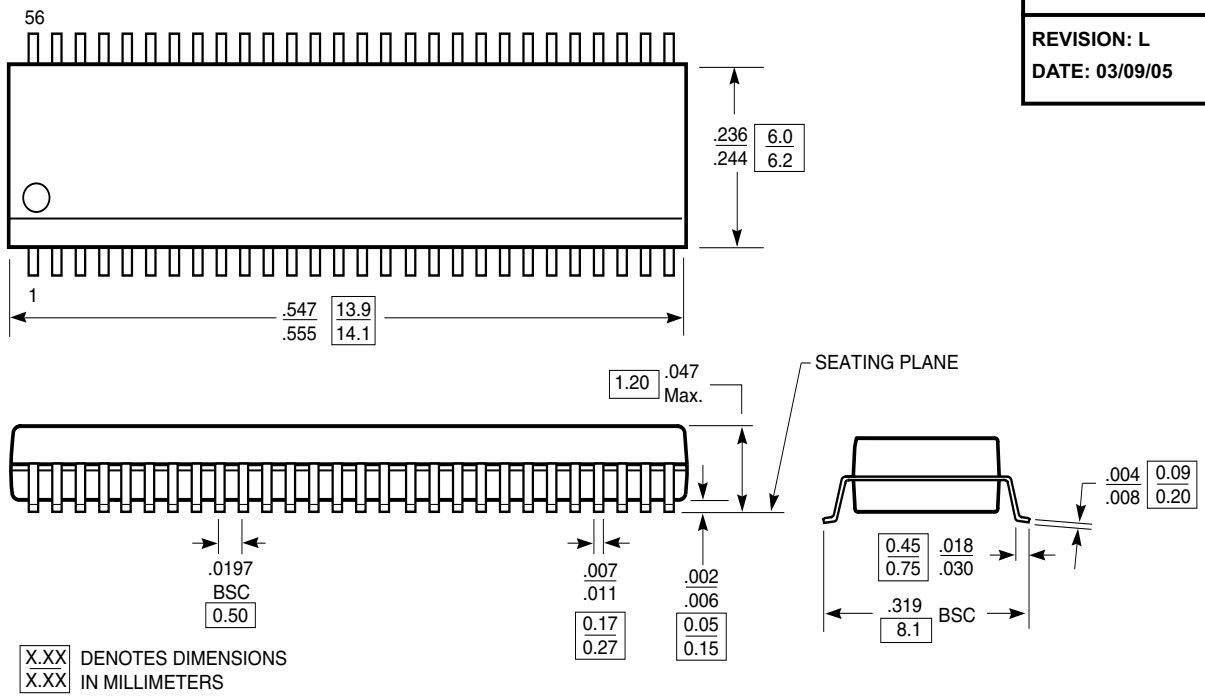
Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	27	30	pF
	Outputs Disabled		16	18	

Packaging Mechanical

DOCUMENT CONTROL NO.
PD - 1502

REVISION: L
DATE: 03/09/05



Notes:
1. Maximum package length and width dimensions do not include mold flash protrusions or gate burrs, which shall not exceed 0.006 inch per side
2. Controlling dimensions in millimeters.
3. Ref: JEDEC MO-153F/EE
4. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM®

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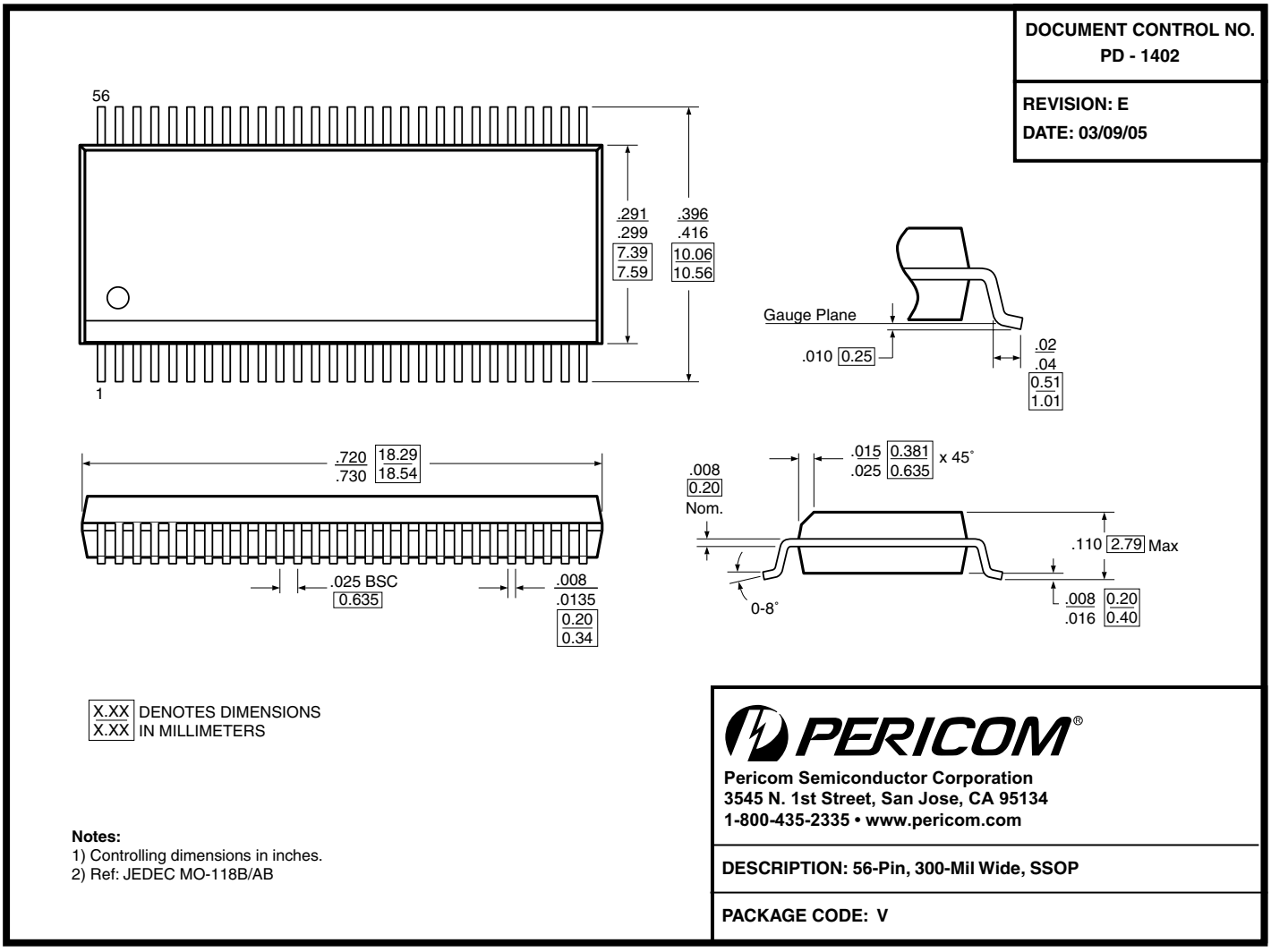
DESCRIPTION: 56-Pin, 240-mil wide TSSOP

PACKAGE CODE: A

Packaging Mechanical



Ordering Information

Ordering Code	Package Type	Package Description
PI74ALVCH16823A	A	56-pin, 240 mil wide plastic TSSOP
PI74ALVCH16823V	V	56-pin, 300 mil wide plastic SSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- Adding an X suffix = Tape/Reel