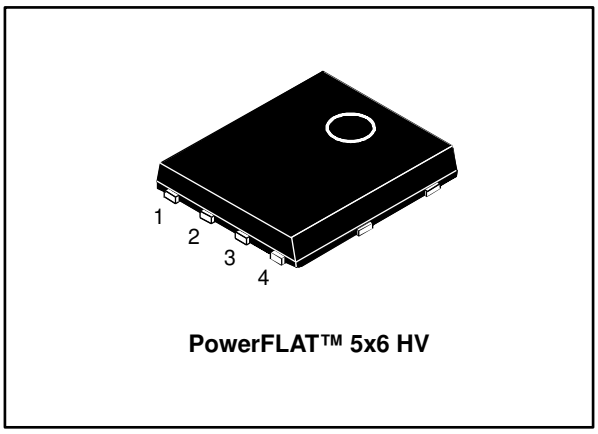
STL15N60M2-EP

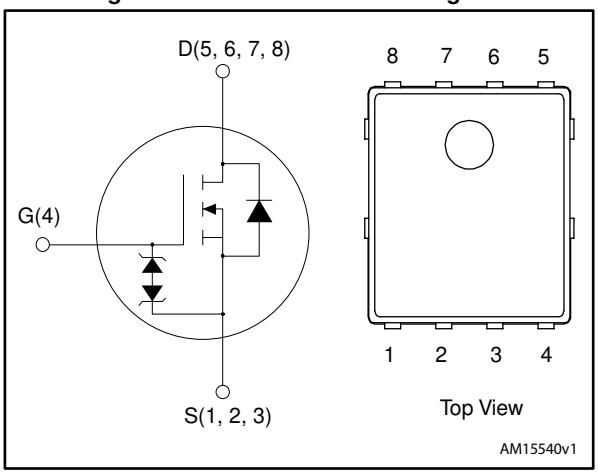
N-channel 600 V, 0.389 Ω typ., 7 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



PowerFLAT™ 5x6 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL15N60M2-EP	650 V	0.418 Ω	7 A	55 W

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL15N60M2-EP	15N60M2EP	PowerFLAT™ 5x6 HV	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	7	A
	Drain current (continuous) at T_{case} = 100 °C	4.6	
I_{DM} (1)	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	55	W
I_{AR} (2)	Avalanche current, repetitive or not repetitive	1.5	A
E_{AS} (3)	Single pulse avalanche energy	110	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
dv/dt (5)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse width limited by T_{jmax}.

(3) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

(4) I_{SD} ≤ 7 A, di/dt=400 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

(5) V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.27	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient	59	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.389	0.418	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	590	-	pF
C_{oss}	Output capacitance		-	30	-	
C_{rss}	Reverse transfer capacitance		-	1.1	-	
$C_{oss\ eq.}$	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	148	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A, V_{GS} = 10 V (see *Figure 16: "Gate charge test circuit"*)	-	17	-	nC
Q_{gs}	Gate-source charge		-	3.1	-	
Q_{gd}	Gate-drain charge		-	7.3	-	

Table 6: Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{OFF}	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	–	5	-	µJ
		V_{DD} = 400 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	–	5.2	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Switching times test circuit for resistive load"* and *Figure 20: "Switching time waveform"*)	-	11	-	ns
t_r	Rise time		-	10	-	
$t_{d(off)}$	Turn-off delay time		-	40	-	
t_f	Fall time		-	15	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM} (1)	Source-drain current (pulsed)		-		28	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.7		µC
I_{RRM}	Reverse recovery current		-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	400		ns
Q_{rr}	Reverse recovery charge		-	3.8		µC
I_{RRM}	Reverse recovery current		-	19		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

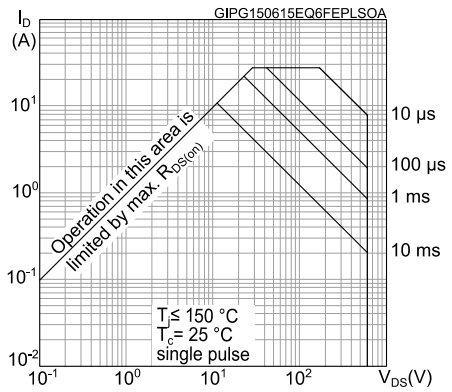


Figure 3: Thermal impedance

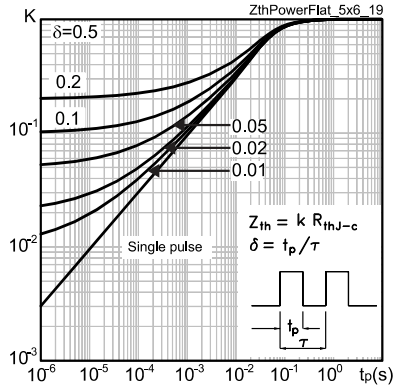


Figure 4: Output characteristics

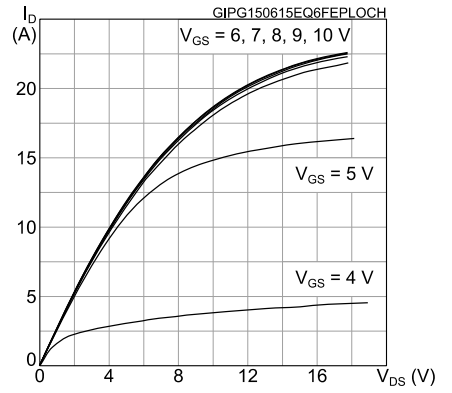


Figure 5: Transfer characteristics

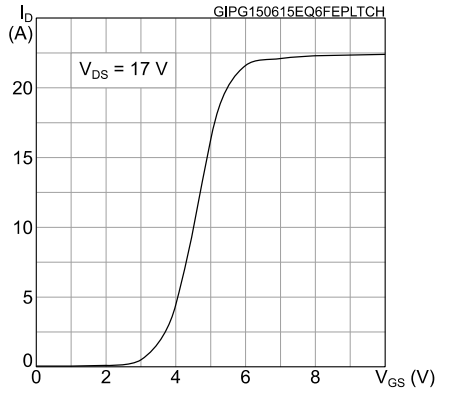


Figure 6: Gate charge vs gate-source voltage

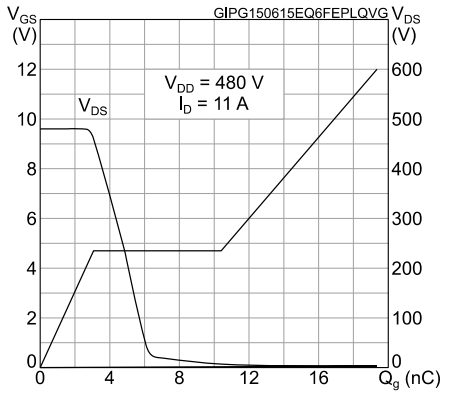


Figure 7: Static drain-source on-resistance

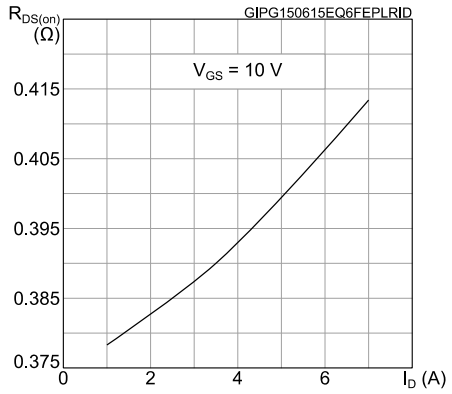


Figure 8: Capacitance variations

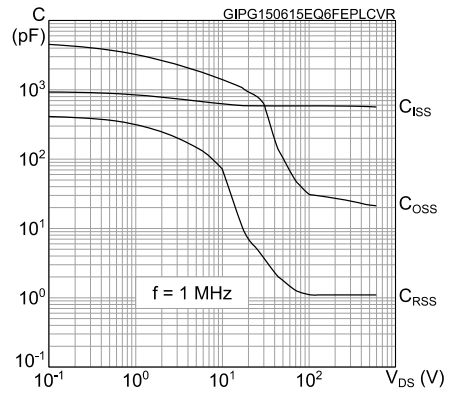


Figure 9: Output capacitance stored energy

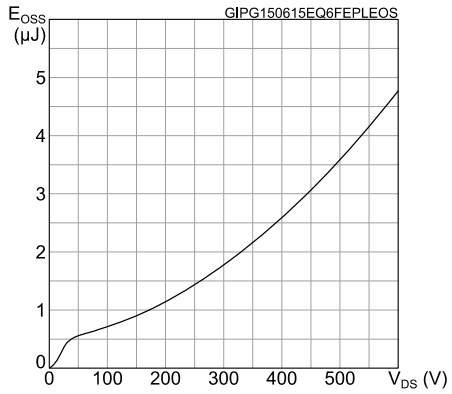


Figure 10: Normalized gate threshold voltage vs temperature

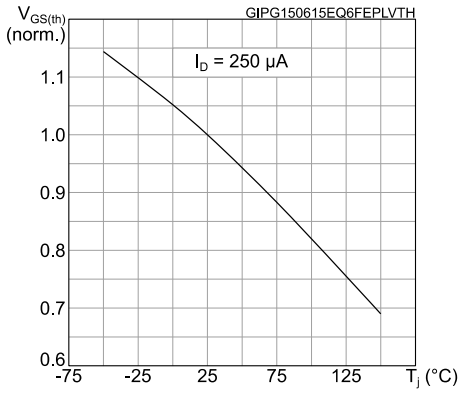


Figure 11: Normalized on-resistance vs temperature

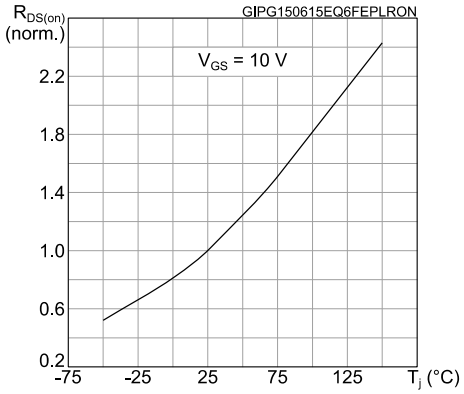


Figure 12: Normalized V(BR)DSS vs temperature

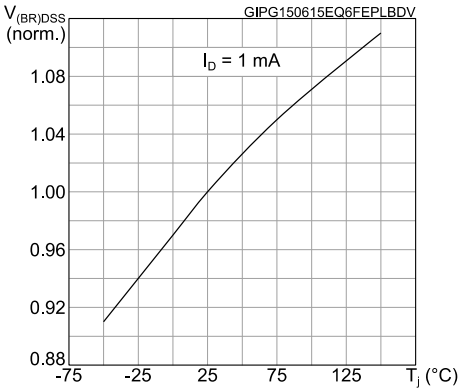


Figure 13: Turn-off switching loss vs drain current

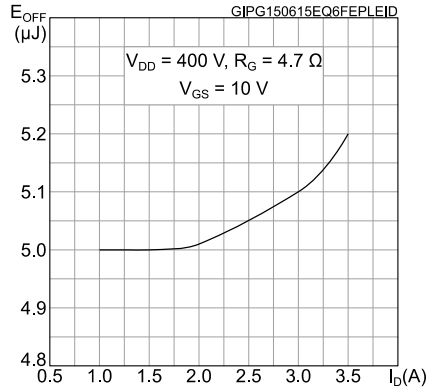
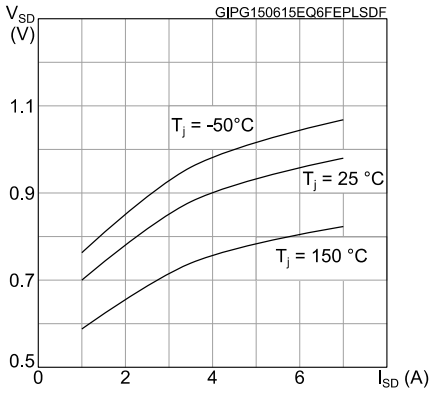


Figure 14: Source-drain diode forward characteristics



3 Test circuits

Figure 15: Switching times test circuit for resistive load

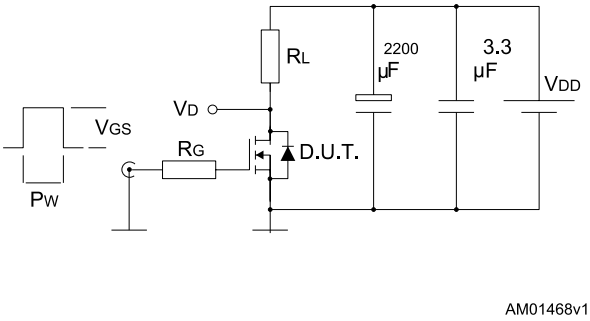


Figure 16: Gate charge test circuit

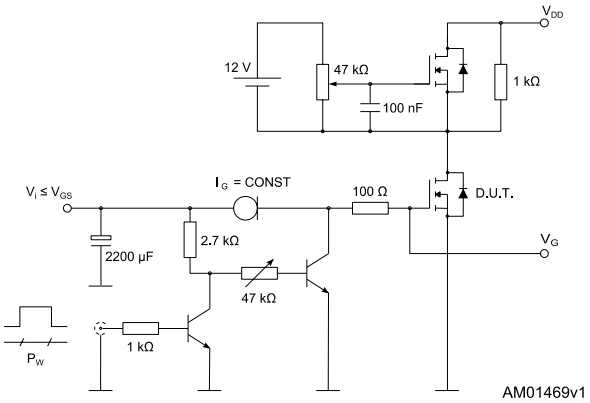


Figure 17: Test circuit for inductive load switching and diode recovery times

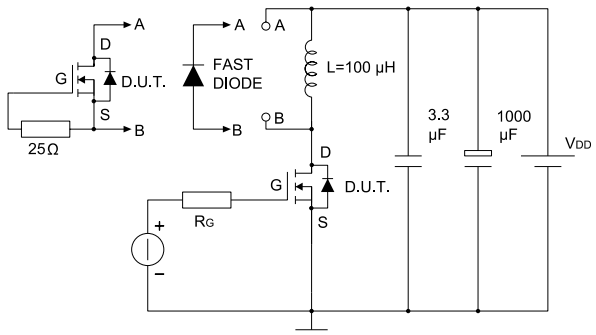


Figure 18: Unclamped inductive load test circuit

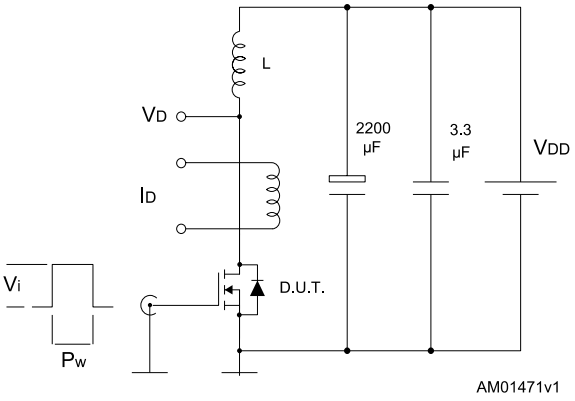


Figure 19: Unclamped inductive waveform

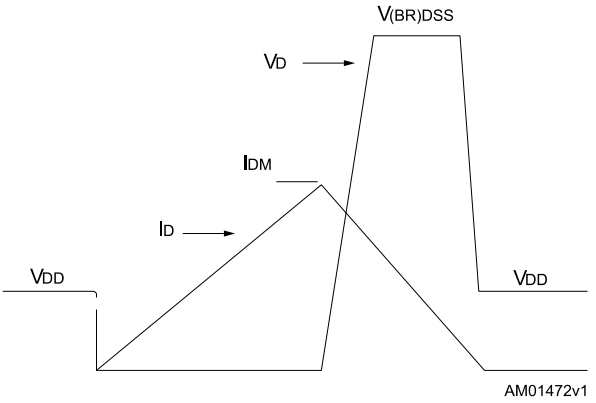
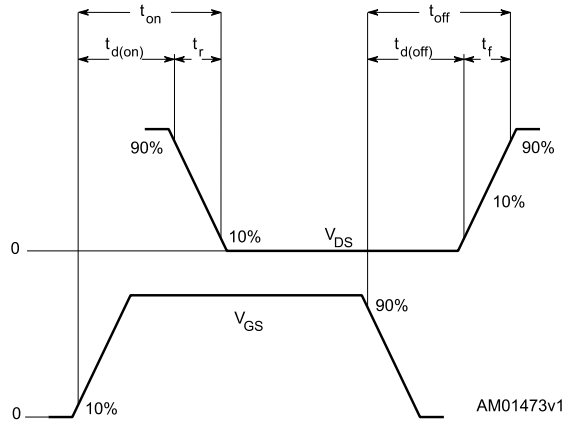


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 21: PowerFLAT™ 5x6 HV package outline

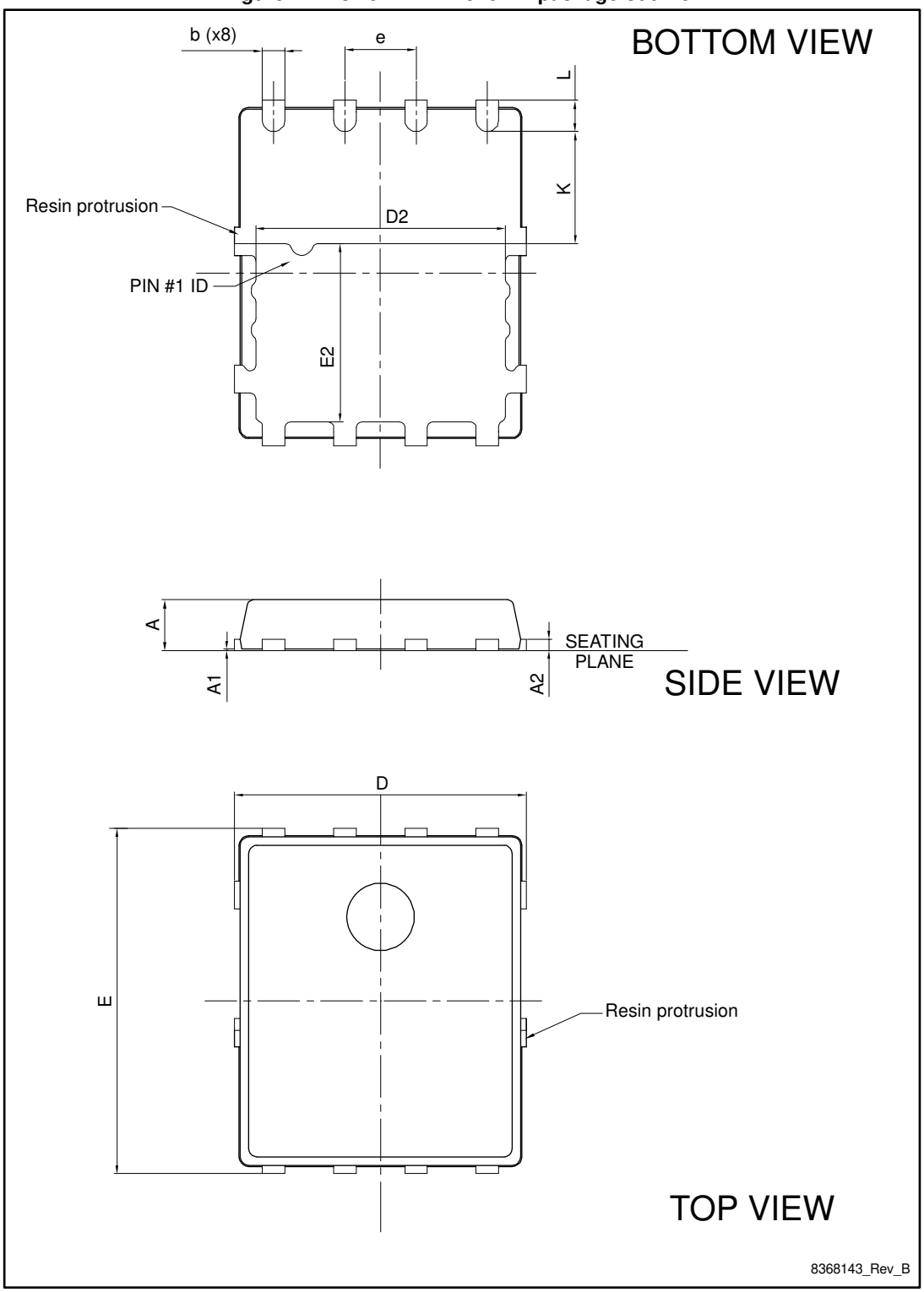
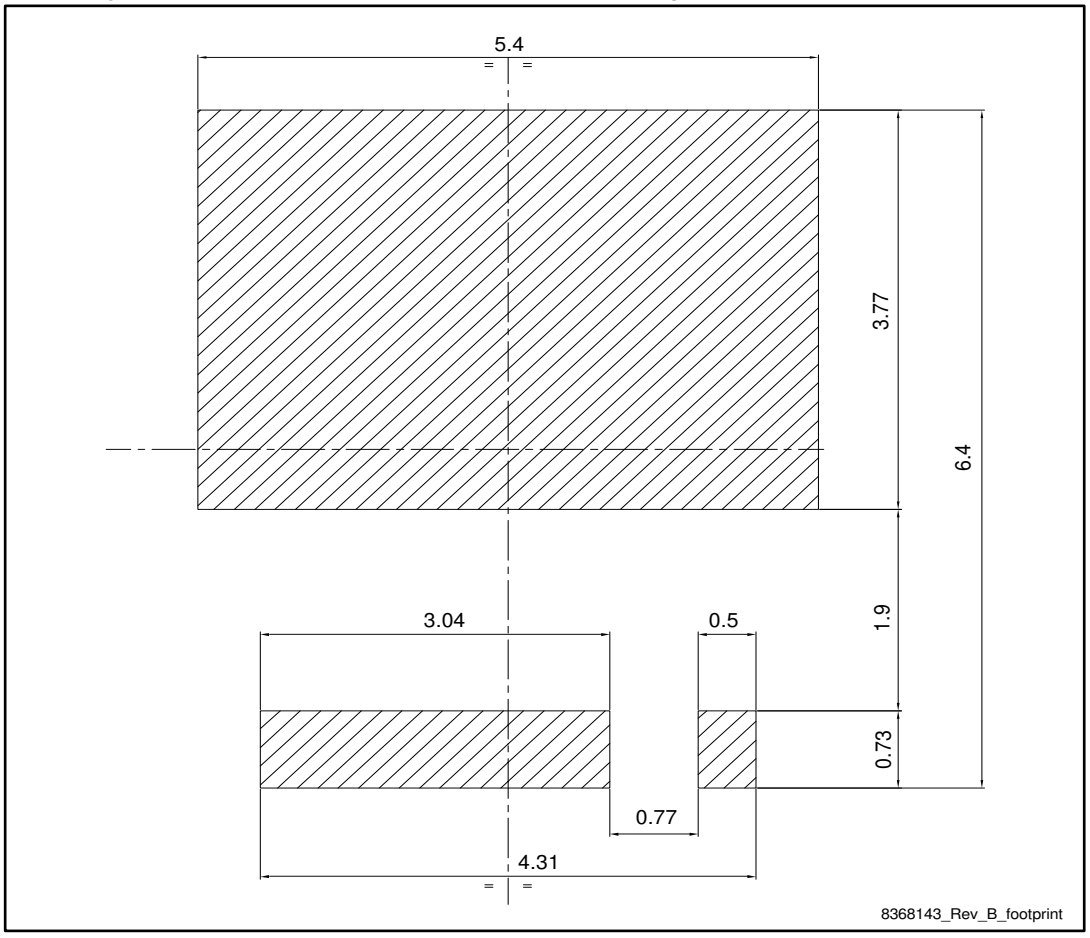


Table 9: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 22: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 23: PowerFLAT™ 5x6 tape outline (dimensions are in mm)

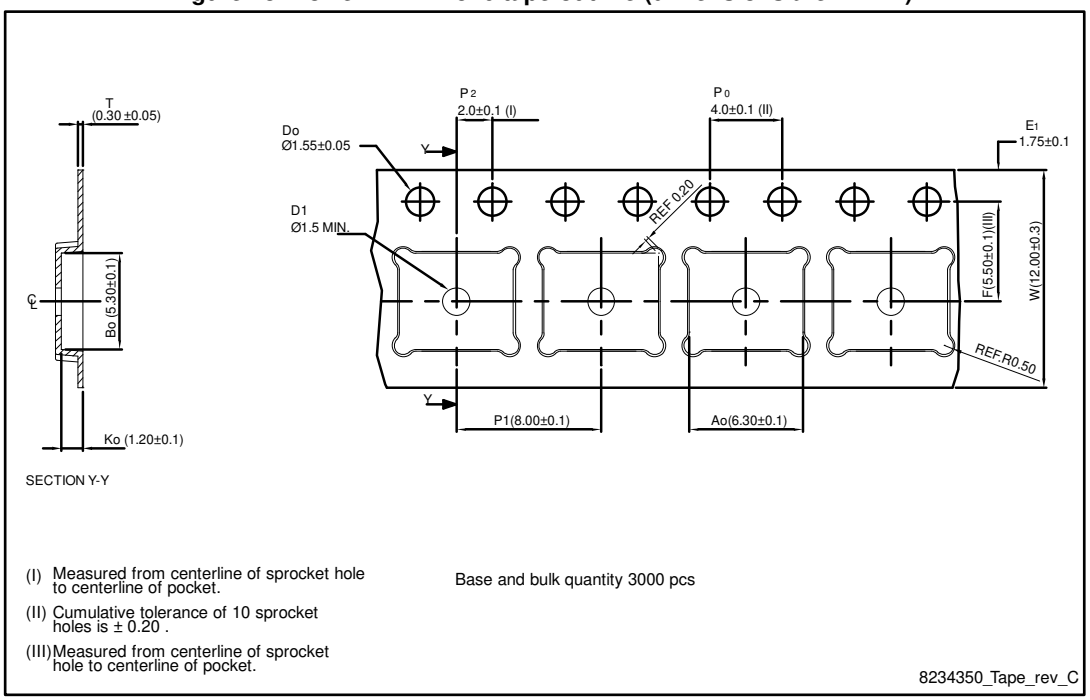


Figure 24: PowerFLAT™ 5x6 package orientation in carrier tape

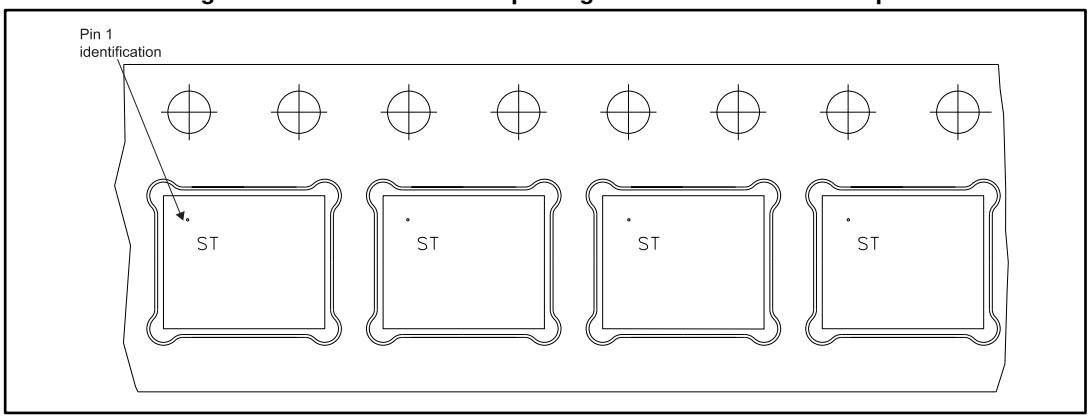
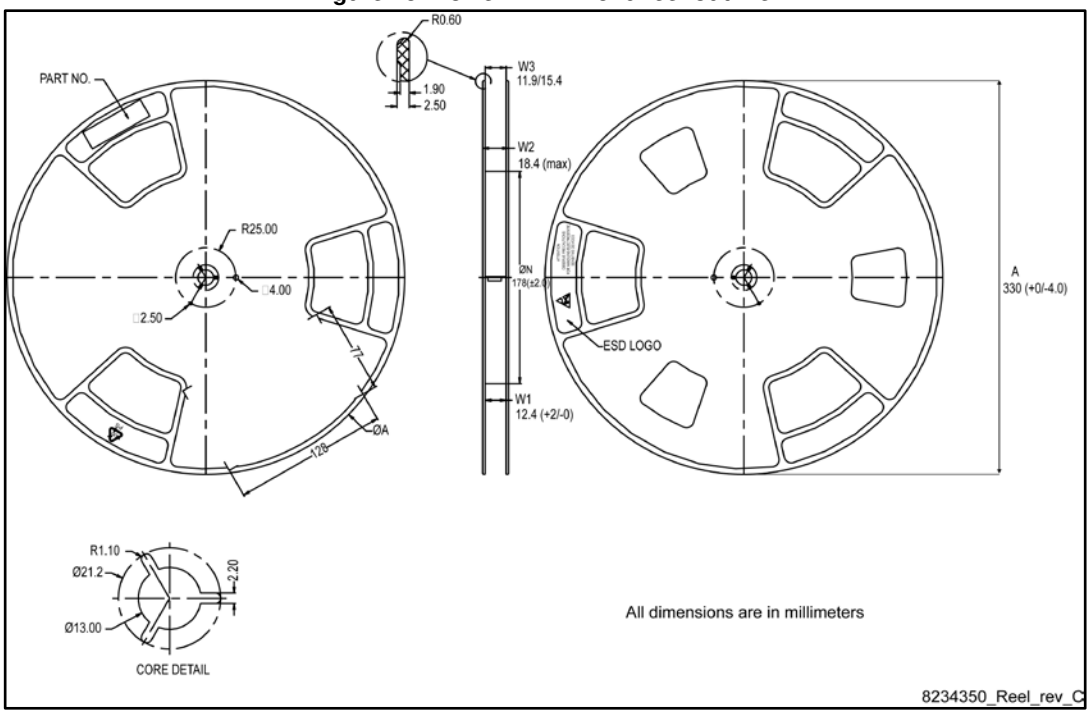


Figure 25: PowerFLAT™ 5x6 reel outline



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
15-Jun-2015	1	First release.

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