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January 2002 Revised January 2003

IN1104 LVDS 4 Port High Speed Repeater

FAIRCHILD

SEMICONDUCTOR*

FIN1104 LVDS 4 Port High Speed Repeater

General Description

This 4 port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The FIN1104 accepts and outputs LVDS levels with a typical differential output swing of 330 mV which provides low EMI at ultra low power dissipation even at high frequencies. The FIN1104 provides a V_{BB} reference for AC coupling on the inputs. In addition the FIN1104 can directly accept LVPECL, HSTL, and SSTL-2 for translation to LVDS.

Features

- Greater than 800 Mbps data rate
- 3.3V power supply operation
- 3.5 ps maximum random jitter and 135 ps maximum deterministic jitter
- Wide rail-to-rail common mode range
- LVDS receiver inputs accept LVPECL, HSTL, and SSTL-2 directly
- Ultra low power consumption
- 20 ps typical channel-to-channel skew
- Power off protection
- > 7.5 kV HBM ESD Protection
- Meets or exceeds the TIA/EIA-644-A LVDS standard
- Available in space saving 24-Lead TSSOP package
- Open circuit fail safe protection
- V_{BB} reference output

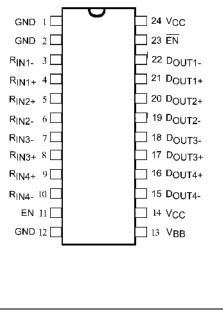
Ordering Code:

Order Number	Package Number	Package Description
FIN1104MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Devices also available	in Tape and Reel. Specify	by appending suffix letter "X" to the ordering code.

Pin Descriptions

Pin Name	Description
R _{IN1+} , R _{IN2+} , R _{IN3+} , R _{IN4+}	Non-inverting LVDS Input
R _{IN1-} , R _{IN2-} , R _{IN3-} , R _{IN4-}	Inverting LVDS Input
$\begin{array}{c} D_{OUT1+}, D_{OUT2+}, \\ D_{OUT3+}, D_{OUT4+} \end{array}$	Non-inverting Driver Output
$\begin{array}{c} D_{OUT1-},D_{OUT2-},\\ D_{OUT3-},D_{OUT4-} \end{array}$	Inverting Driver Output
EN	Driver Enable Pin for All Output
EN	Inverting Driver Enable Pin for all Outputs
V _{CC}	Power Supply
GND	Ground
V _{BB}	Reference Voltage Output

Connection Diagram

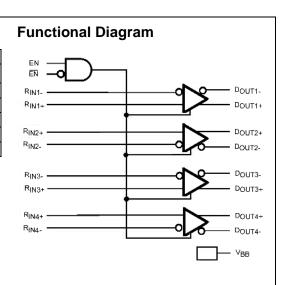


FIN1104

Function Table

Inputs Outputs EN EN $\mathbf{D}_{\mathbf{IN}^+}$ D_{IN-} D_{OUT+} D_{OUT-} Н L Н L Н L Н L L Н L Н Н L Fail Safe Case Н L Х Н Х Х Ζ Ζ Х L Х Х Ζ Ζ

H = HIGH Logic Level L = LOW Logic Level X = Don't Care Z = High Impedance



Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +4.6V
LVDS DC Input Voltage (VIN)	-0.5V to +4.6V
LVDS DC Output Voltage (V _{OUT})	-0.5V to +4.6V
Driver Short Circuit Current (I _{OSD})	Continuous 10 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Max Junction Temperature (T _J)	150°C
Lead Temperature (T _L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	7500V
ESD (Machine Model)	400V

Recommended Operating Conditions

Supply Voltage (V _{CC})	3.0V to 3.6V
Magnitude of Differential	
Voltage (V _{ID})	100 mV to V_{CC}
Common Mode Voltage	(0) (1) (1) (2) to (1) (1) (1)
Range (V _{IC})	$(0V + V_{ID} /2)$ to $(V_{CC} - V_{ID} /2)$
Operating Temperature (T _A)	-40°C to +85°C

FIN1104

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Typ (Note 2)	Max	Units
V _{TH}	Differential Input Threshold HIGH	See Figure 1; $V_{IC} = +0.05V$, +1.2V, or V_C	_C – 0.05V			100	mV
V _{TL}	Differential Input Threshold LOW	See Figure 1; $V_{IC} = +0.05V$, +1.2V, or V_{C}	_C – 0.05V	-100			mV
V _{IH}	Input HIGH Voltage (EN or EN)			2.0		V _{CC}	V
VIL	Input LOW Voltage (EN or EN)			GND		0.8	V
V _{OD}	Output Differential Voltage			250	330	450	mV
ΔV_{OD}	V _{OD} Magnitude Change from Differential LOW-to-HIGH	R_L = 100 Ω_i Driver Enabled, See Figure 2				25	mV
V _{OS}	Offset Voltage			1.125	1.23	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH					25	mV
I _{OS} Short Circuit Output Current	D _{OUT+} = 0V and D _{OUT-} = 0V, Driver Enabled			-3.4	-6	mA	
		V _{OD} = 0V, Driver Enabled			±3.4	±6	mA
I _{IN}	Input Current (EN, \overline{EN} , D_{INx+} , D_{INx-})	$V_{IN} = 0V$ to V_{CC} , Other Input = V_{CC} or $0V$ (for Differential Inputs)				±20	μΑ
I _{OFF}	Power Off Input or Output Current	$V_{CC} = 0V$, V_{IN} or $V_{OUT} = 0V$ to 3.6V				±20	μA
I _{CCZ}	Disabled Power Supply Current	Drivers Disabled			5.4	11	mA
ICC	Power Supply Current	Drivers Enabled, Any Valid Input Condition			30.4	41	mA
I _{OZ}	Disabled Output Leakage Current	Driver Disabled, $D_{OUT+} = 0V$ to 3.6V or $D_{OUT-} = 0V$ to 3.6V				±20	μΑ
VIC	Common Mode Voltage Range	$ V_{ID} = 100 \text{ mV to } V_{CC}$		$0V + V_{ID} /2$		$V_{CC} - (V_{ID} /2)$	V
C _{IN}	Input Capacitance	Ena	able Input		2.6		pF
		LVE	OS Input		2.1		μr
C _{OUT}	Output Capacitance				2.8		pF
V _{BB}	Output Reference Voltage	V _{CC} = 3.3V, I _{BB} = 0 to -275 μA		1.125	1.2	1.375	V

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

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AC Electrical Characteristics

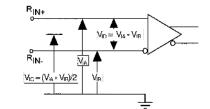
Over supply voltage and operating temperature ranges, unless otherwise specified

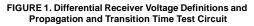
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t _{PLHD}	Differential Output Propagation Delay		0.75	1.1	1.75	
	LOW-to-HIGH		0.75	1.1	1.75	ns
t _{PHLD}	Differential Output Propagation Delay		0.75	1.1	1.75	ns
	HIGH-to-LOW	$R_L = 100 \ \Omega$, $C_L = 5 \ pF$,				
t _{TLHD}	Differential Output Rise Time (20% to 80%)	$V_{ID} = 200 \text{ mV}$ to 450 mV,	0.29	0.4	0.58	ns
t _{THLD}	Differential Output Fall Time (80% to 20%)	$V_{IC} = V_{ID} /2$ to $V_{CC} - (V_{ID} /2)$,	0.29	0.4	0.58	ns
t _{SK(P)}	Pulse Skew t _{PLH} - t _{PHL}	Duty Cycle = 50%,		0.02	0.2	ns
t _{SK(LH)} ,	Channel-to-Channel Skew	See Figure 1 and Figure 3		0.02	0.15	ns
t _{SK(HL)}	(Note 4)			0.02	0.15	
t _{SK(PP)}	Part-to-Part Skew (Note 5)				0.5	ns
f _{MAX}	Maximum Frequency (Note 6)(Note 7)		400	800		MHz
t _{PZHD}	Differential Output Enable Time	-		2.2	5	ns
	from Z to HIGH			2.2	5	115
t _{PZLD}	Differential Output Enable Time			2.5	5	ns
	from Z to LOW	$R_L = 100 \ \Omega$, $C_L = 5 \ pF$,		2.5	5	115
t _{PHZD}	Differential Output Disable Time	See Figure 2 and Figure 3		1.8	5	ns
	from HIGH to Z			1.0	5	115
t _{PLZD}	Differential Output Disable Time			2.1	5	ns
	from LOW to Z			2.1	5	115
t _{DJ}	LVDS Data Jitter,	$V_{ID} = 300 \text{ mV}, \text{ PRBS} = 2^{23} \text{ - } 1,$ $V_{IC} = 1.2 \text{V} \text{ at } 800 \text{ Mbps}$		85	135	ps
	Deterministic			05	155	μs
t _{RJ}	LVDS Clock Jitter,	V _{ID} = 300 mV,		2.1	3.5	ps
	Random (RMS)	V _{IC} = 1.2V at 400 MHz		2.1	5.5	

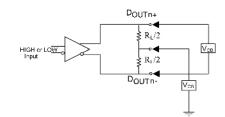
Note 4: t_{SK(LH)}, t_{SK(HL)} is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either Low-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits. Note 6: Passing criteria for maximum frequency is the output $V_{OD} > 200$ mV and the duty cycle is 45% to 55% with all channels switching.

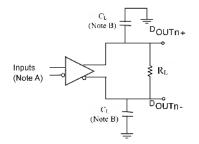
Note 7: Output loading is transmission line environment only; CL is < 1 pF of stray test fixture capacitance.







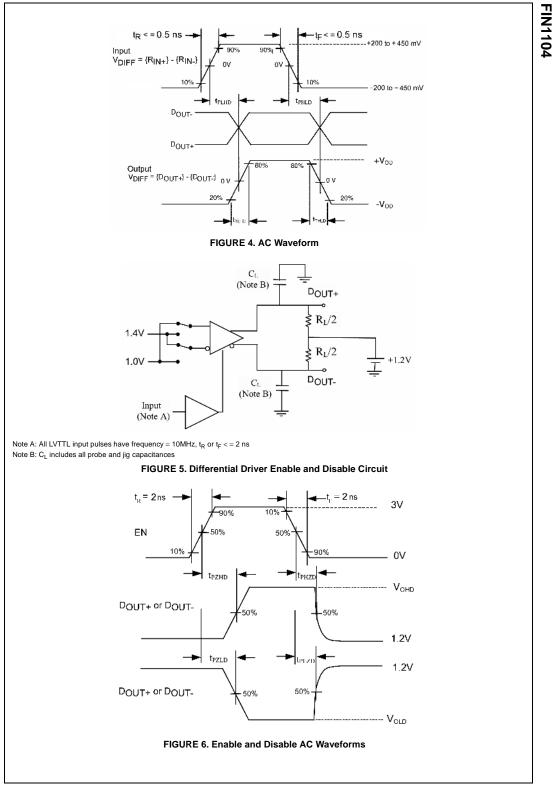


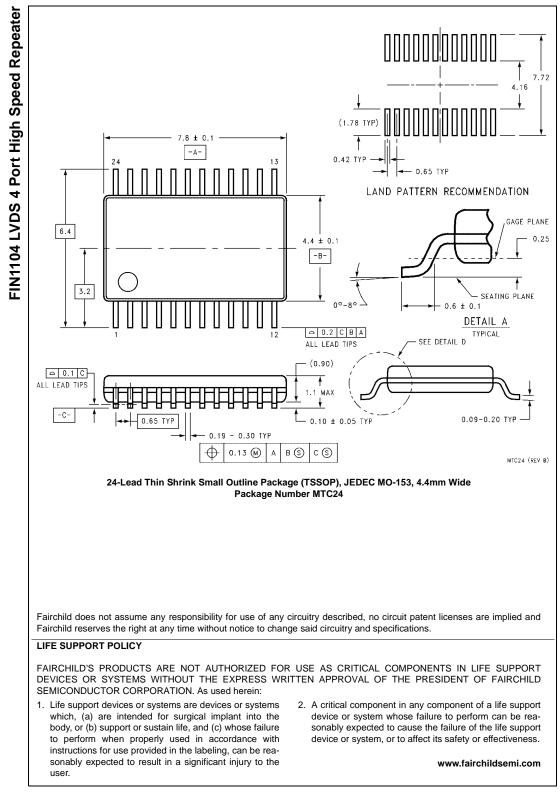


Note A: All LVDS input pulses have frequency = 10 MHz, t_R or $t_F <$ = 0.5 ns

Note B: $\mathbf{C}_{\mathbf{L}}$ includes all probe and test fixture capacitances

FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit





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