DAC7631EVM

This user's guide describes the DAC7631 evaluation module. It covers the operating procedures and characteristics of the EVM board along with the device that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

Contents

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List of Tables

1 Information about Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a CAUTION statement.

A CAUTION statement describes a situtation that could potentially damage this EVM board or your software or equipment.

WARNING

This is an example of a WARNING statement.

A WARNING statement describes a situtation that could potentially cause HARM to **you**.

The information in a caution or a warning is provided for your protection. Read each caution and warning carefully.

2 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through the TI Website at http://www.ti.com.

Data Sheets:	Literature Number:
DAC7631	SBAS122
OPA627	SBOS165
OPA2234	SBOS055
OPA703	SBOS180A
REF3025	SBVS032C
XTR115	SBOS124A

3 Questions about this or other Data Converter EVM's?

If you have questions about this or other Texas Instruments Data Converter evaluation modules, feel free to E-mail the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product you have questions or concerns with.

4 EVM Overview

This section provides an overview of the DAC7631 evaluation module (EVM), and instructions on setting up and using this evaluation module.

4.1 Features

This EVM features the DAC7631 digital-to-analog converter (DAC). It provides a quick and easy way to evaluate the functionality and performance of the high-resolution serial input DAC. The EVM provides the serial interface header to easily attach to any host microprocessor or TI DSP base system for communication.

4.2 Power Requirements

The power requirements of the EVM are described in the following sections.

4.2.1 Supply Voltage

The dc-power supply for the digital section (VDD) of this EVM is dedicated to 5 V via the J3-1 terminal or J6-10 terminal and is referenced to ground through the J3-2 and J6-5 terminals respectively.

The dc-power supply requirements for the analog section of this EVM are as follows; the V_{CC} and V_{SS} are typically 15 V, but can range from ±4.5-V minimum to ±18-V maximum and connect through J1-3 and J1-1, respectively, or through J6-1 and J6-2 terminals. The +5VA connects through J6-3 and the –5VA connects through J6-4. All of the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The device under test (U1) analog power supply can be provided by ±5VA (via J6-3 and J6-4). The V_{CC} supply source provides the positive rail of the external output operational amplifier, U2, and the supply for the reference buffer, U3. The negative rail of U2 can be selected between VSS and AGND via W5 jumper, while the negative supply of U3 is permanently tied to V_{SS}. The external output operational amplifier is installed as an option to provide output signal conditioning or for other output configurations desired.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

4.2.2 Reference Voltage

The externally generated ±2.5-V precision voltage reference is jumper selectable via W7. The external reference voltage source can come from the REF3125, which is a 15 ppm/°C CMOS device or through an XTR115 current loop transmitter. The –2.5-V reference is created by inverting the selected output via the U5 operational-amplifier circuit. These voltage references are buffered through the U3 operational amplifier, which provides the DAC7631 voltage-output range.

5 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC7631 DAC. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TMS320™ DSP family, or some sort of a signal/waveform generator.

The headers J2 and P2 are the connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC7631 EVM using a custom-built cable.

A specific adapter interface card is also available for most of TI's DSP Starter Kits (DSK) and the card model depends on the type of the TI DSP Starter Kit to be used. To acquire the right adapter interface card, be sure to specify the DSP that is used. In addition, there is also an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor, with which this EVM can connect and interface. For more details or information regarding the adapter interface card or the HPA449 platform, call Texas Instruments, or send an e-mail to dataconvapps@list.ti.com.

The DAC output can be monitored through the selected pins of J4 header connector. The output of U1 can be switched from either pin 2 or pin 4 of the header, J4, for stacking reason. Stacking allows a total of two DAC channels (if two DAC7631 EVMs are stacked).

In addition, the option of selecting one DAC output (from J4-2 or J4-4) to be connected to the output operational amplifier, U2, is also possible by using a jumper across the selected pins of J4. The output operational amplifier, U2, is configurable through J5, W5, and W15 for any desired waveform characteristic.

A block diagram of the DAC7631 EVM is shown in Figure 1.

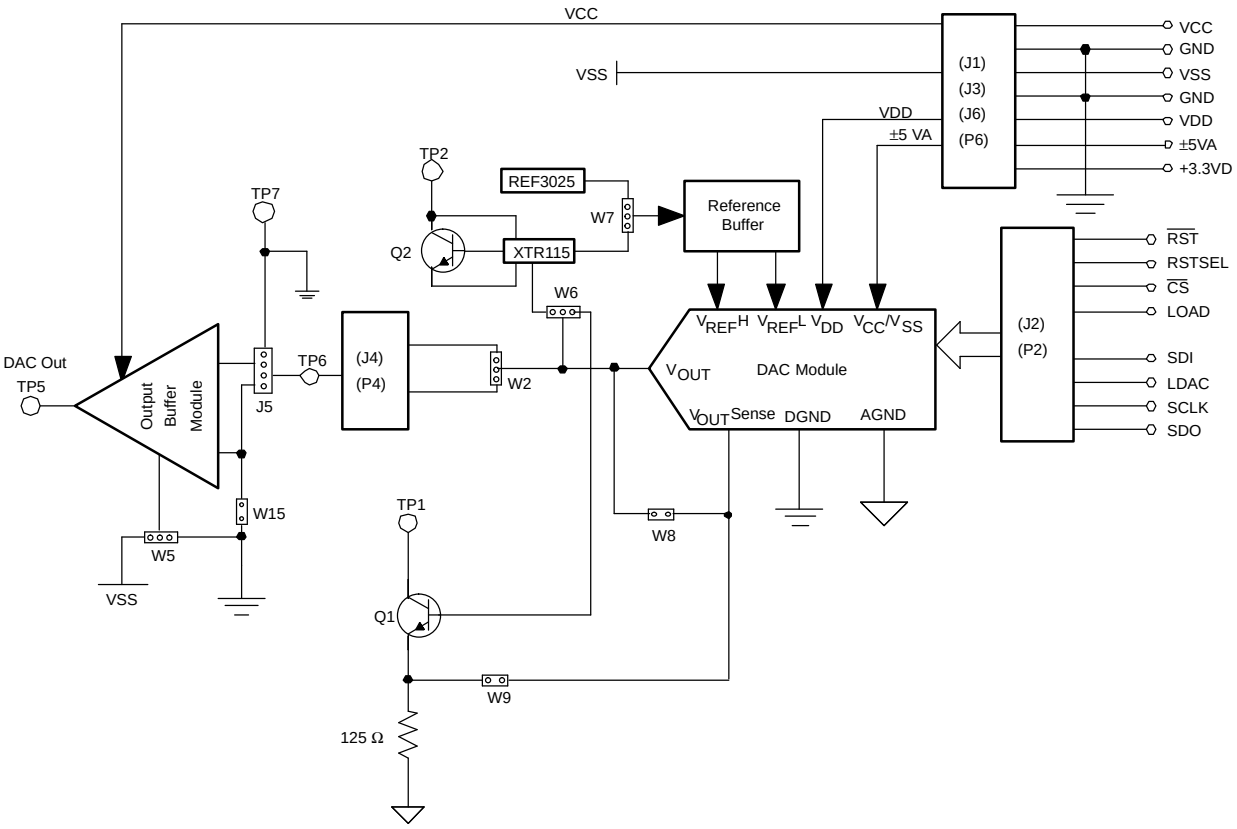

Figure 1. DAC7631 EVM Block Diagram

6 PCB Design and Performance

This section covers the layout design of the PCB, describing the physical and mechanical characteristics of the EVM. This section also shows the resulting performance of the EVM which can be compared to the device specification listed in the data sheet. The list of components used on the module is also included in this section.

6.1 PCB Layout

The DAC7631 EVM is designed to demonstrate the performance quality of the installed DAC device under test, as specified in the data sheet. Careful analysis of the EVM's physical restrictions and factors that contributes to the EVM's performance degradation is the key to a successful design implementation. The obvious attributes that contributes to the poor performance of the EVM can be avoided during the schematic design phase by properly selecting the right components and designing the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and knowing or understanding the components mechanical attributes.

The obscure part of the design lies particularly in the layout process. The main concern is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane does the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices can be seen in the following figures.

The DAC7631 EVM board is constructed on a four-layer, printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) X 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 3 through Figure 6 show the individual artwork layers.

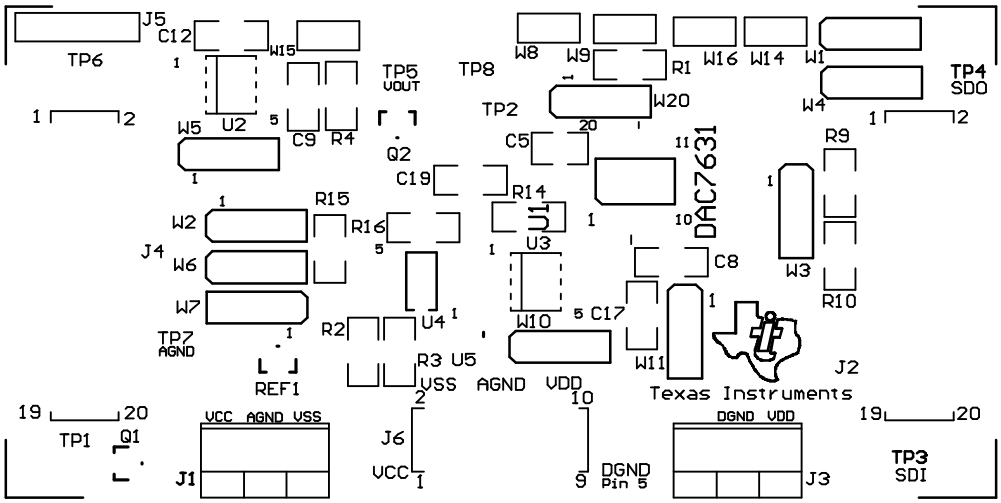

Figure 2. Top Silkscreen

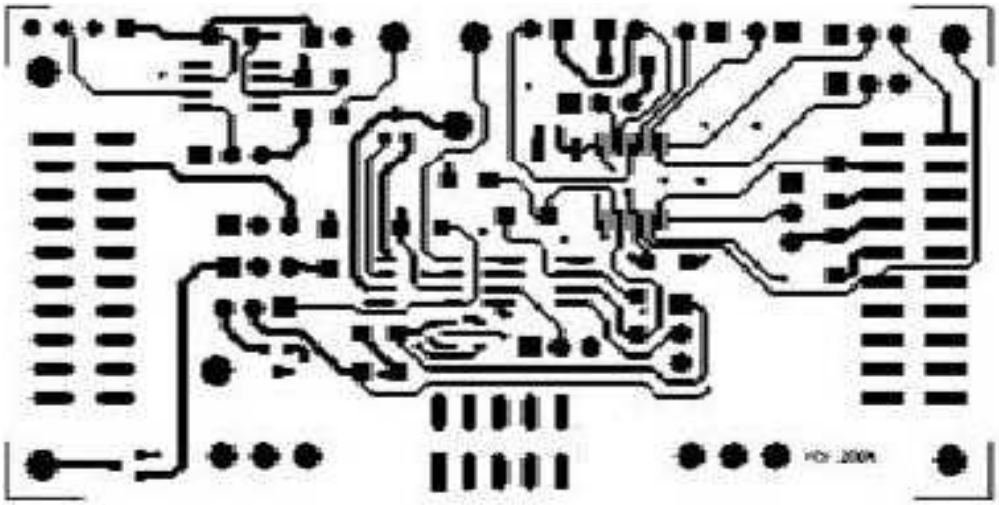

Figure 3. Layer 1 (Top Signal Plane)

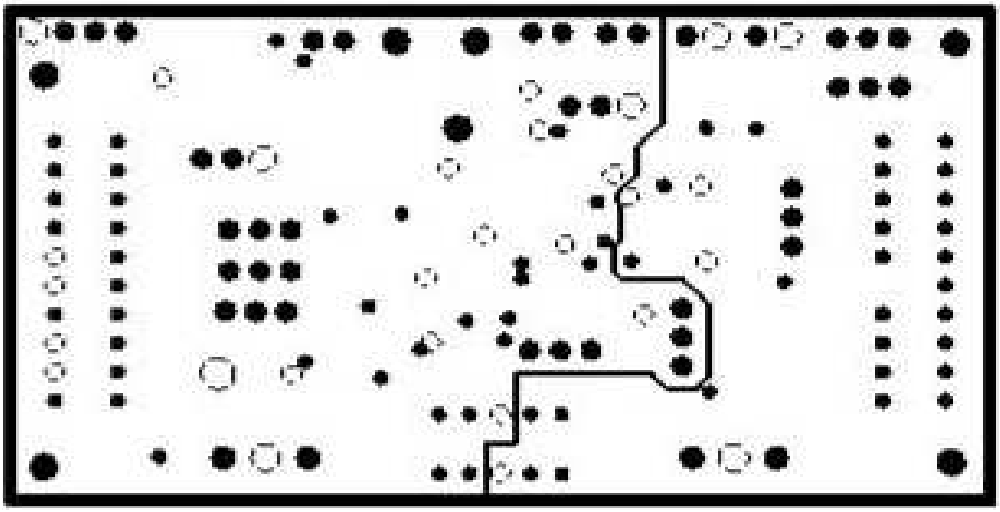

Figure 4. Layer 2 (Ground Plane)

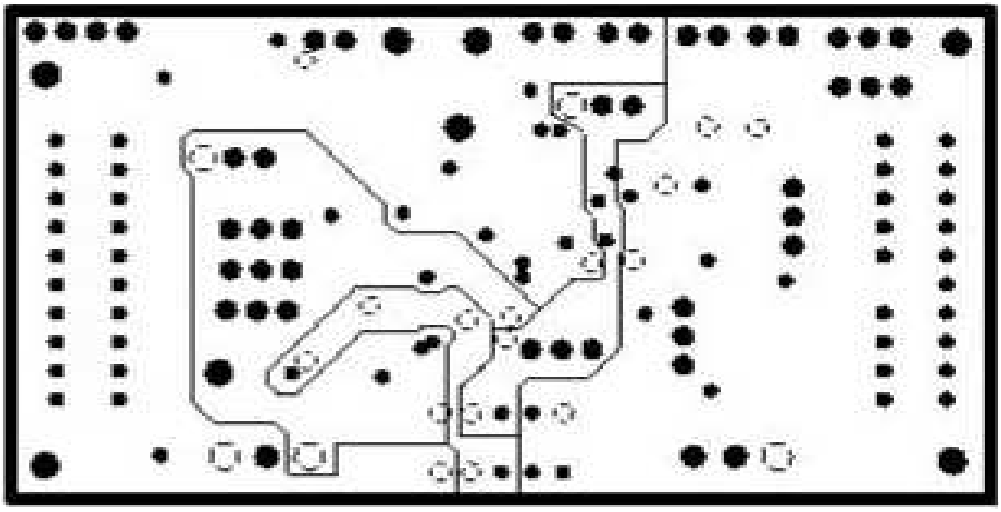

Figure 5. Layer 3 (Power Plane)

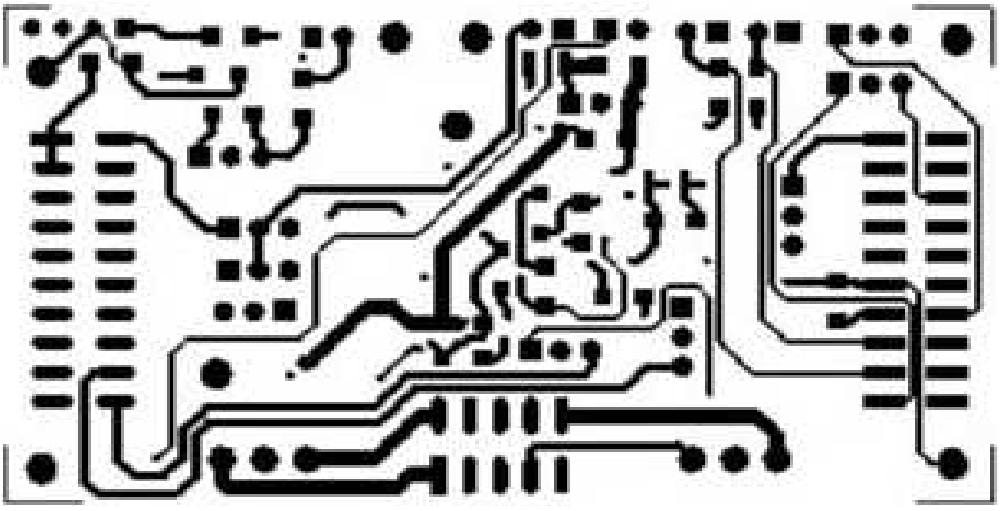

Figure 6. Layer 4 (Bottom Signal Plane)

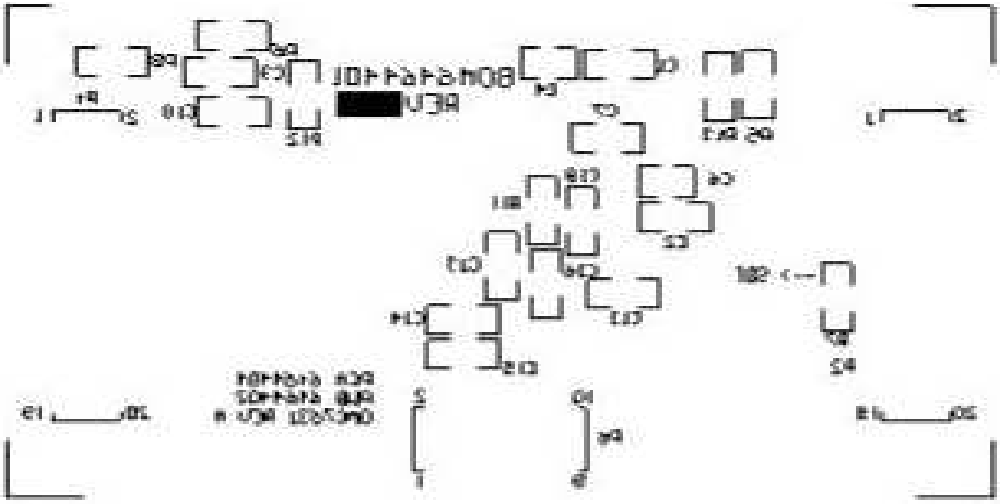

Figure 7. Bottom Silkscreen

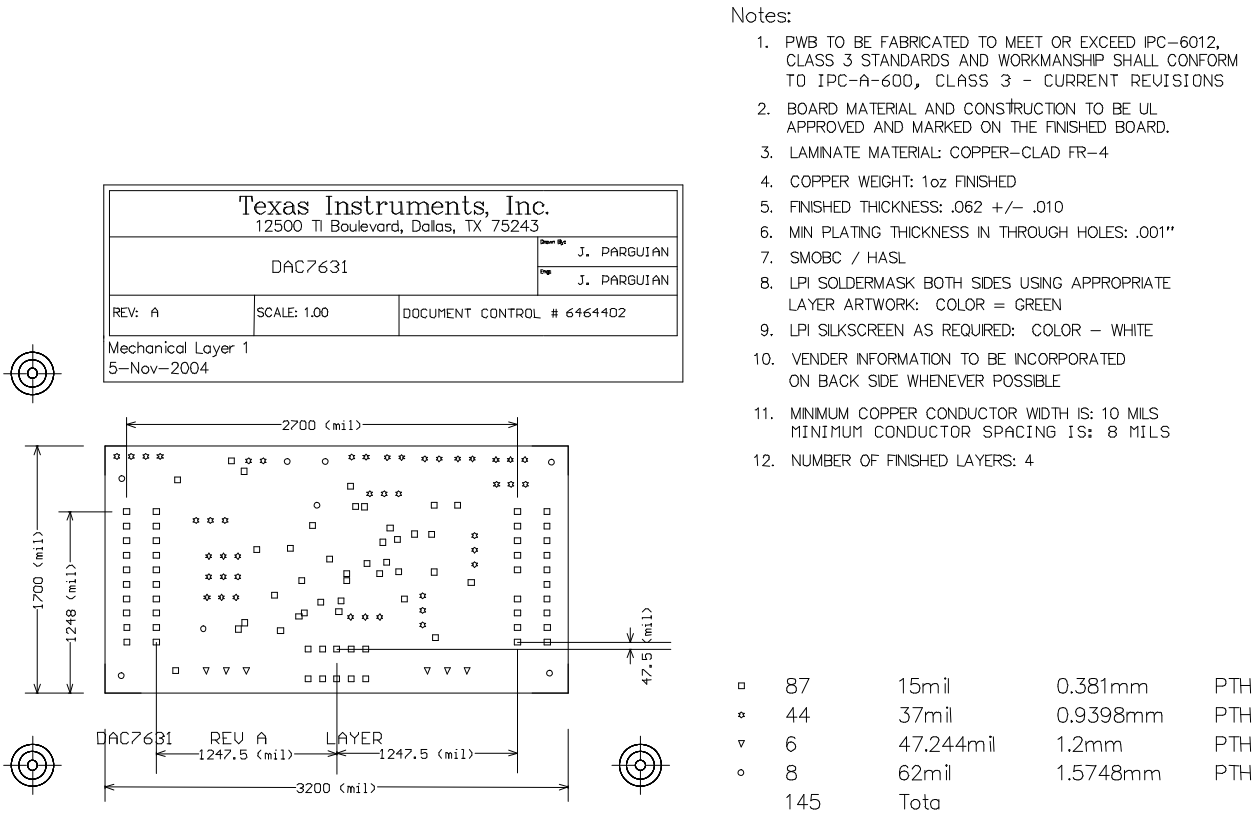

Figure 8. Drill Drawing

6.2 Bill of Materials

Table 1. Parts List

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	2	C9 C10	TDK	C3216COG2A103KT	0.01 µF, 1206 Multilayer Ceramic Capacitor
2	8	C1 C2 C7 C8 C11 C13 C14 C15	TDK	C3216COG1E104KT	0.1 µF, 1206 Multilayer Ceramic Capacitor
3	1	C12	TDK	C3216COG2A102KT	1 nF, 1206 Multilayer Ceramic Capacitor
4	3	C4 C5 C6	TDK	C3225X7R1E106KT	10 µF, 1210 Multilayer Ceramic X5R Capacitor
5	1	C3	TDK	C3216X7R1E471KT	470 pF, 50V, 1206 Multilayer Ceramic Capacitor SMD
6	3	R7 R9 R10 (1)	Panasonic	ERJ-8GEY0R00V	0 Ω, 1/4W 1206 Chip Resistor
7	1	R1	Panasonic	ERJ-8ENF1240V	124 Ω, 1%, 1/8W 1206 Chip Resistor
8	3	R4 R11 R14	Panasonic	ERJ-8GEYJ101V	100 Ω, 1/4W 1206 Chip Resistor
9	1	R8	Panasonic	ERJ-8GEYJ202V	2 kΩ, 5%, 1/4W 1206 Chip Resistor
10	6	R2 R3 R5 R6 R12 R13	Panasonic	ERJ-8ENF1002V	10 kΩ, 1/4W 1206 Chip Resistor
11	2	Q1 Q2	Panasonic	2SC24050RL	FET Transistor NPN 35VCEO 50MA MINI-3P
12	1	J5	Molex	22-03-2041	4 Position Jumper_ 0.1" spacing
13	1	J6	Samtec	TSM-105-01-T-DV	5×2×0.1 10-pin 3A Isolated Power Socket
14	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10×2×0.1, 20 Pin .025"sq SMT Socket
15	2	J1 J3 (1)	On-Shore Technology	ED555/3DS	3-Pin Terminal Connector
16	1	U1	Texas Instruments	DAC7631E	16-bit, Voltage Output, Serial Input DAC
17	1	U2	Texas Instruments	OPA627AU	8-SOP(D) Precision Op Amp
18	8	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	Mill-max	2348-2-01-00-00-07-0	Turret Terminal Test Point
19	2	P2 P4 (2)	Samtec	SSW-110-22-S-D-VS-P	20 Pin 0.025" sq SMT Terminal Strips
20	1	P6 (2)	Samtec	SSW-105-22-F-D-VS-K	3A Isolated 10-pin Power Header
21	4	W8 W9 W14 W16	Molex	22-03-2021	2 Position Jumper_ 0.1" spacing
22	10	W1 W2 W3 W4 W5 W6 W7 W10 W11 W20	Molex	22-03-2031	3 Position Jumper_ 0.1" spacing
23	1	R15	Panasonic	ERJ-8ENF1242V	12.4 kΩ, 1/4 W 1206 Chip Res
24	1	R16	Panasonic	ERJ-8ENF3163V	316 kΩ, 1/4 W 1206 Chip Res
25	2	C18 C19	TDK	C3216COG2A102KT	1000 pF, NPO Ceramic 1206
26	2	C16 C17	TDK	C3216COG2J222KT	2200 pF, NPO Ceramic 1206
27	1	U3	Texas Instruments	OPA2234U	Dual Precision Op-amp 8 SOIC
28	1	U4	Texas Instruments	XTR115U	4-mA to 20-mA Transmitter, 8-SO
29	1	U5	Texas Instruments	OPA703NA	CMOS Op-amp, SOT23-5
30	1	REF1	Texas Instruments	REF3125AIDBZT	Precision 2.5V Ref, SOT23-3

(1) The following parts: J1, J3, R7, R9, and R10 are not installed.
(2) P2, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed in the bottom side of the pc board opposite the J-designated counterpart. For example, J2 is installed on the top side while P2 is installed in the bottom side opposite of J2.

7 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a host processor.

See the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide for more information about the DAC's serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

7.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in Table 2 to operate in bipolar ±2.5-V output operation. The default jumper settings are also shown in Table 2.

Table 2. DAC7631EVM Factory Default Jumper Setting

DAC7631EVM JUMPER DEFAULT CONFIGURATION		
Reference	**Jumper Positiion**	**Function**
W1	2-3	LDAC is driven by the GPIO0 input from J2-2
W2	1-2	DAC output (V_{OUT}) is routed to J4-2
W3	1-2	$\overline{CS}$ signal is driven from J2-1
W4	1-2	$\overline{LOAD}$ is driven by GPIO1 from J2-6
W5	1-2	Negative supply rail of U2 operational-amplifier is supplied with V_{SS}
W6	OPEN	4-mA to 20-mA operation
W7	2-3	External voltage reference source is supplied by REF1
W8	CLOSE	V_{OUT} sense pin is tied to V_{OUT} pin
W9	OPEN	4-mA to 20-mA operation
W10	1-2	External reference to $V_{REF}H$
W11	1-2	External reference to $V_{REF}L$ via U5 for inversion
W14	OPEN	Reset pin high
W15	OPEN	U2 operational amplifier configuration jumper set to unity gain
W16	OPEN	RSTSEL configuration jumper
W20	2-3	Dual supply operation (V_{SS} = –5VA)
J5	2-3	DAC output (V_{OUT}) is routed to the noninverting input of U2

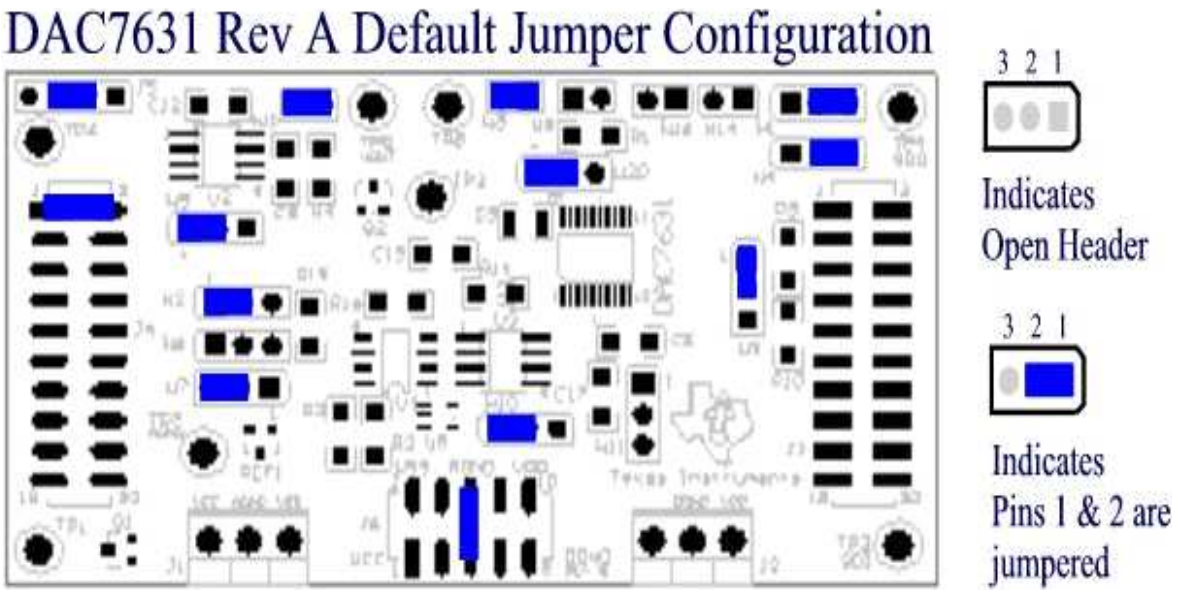

Figure 9. DAC7631EVM Default Jumper Setting

7.2 Host Processor Interface

The host processor drives the DAC. The DAC's proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for a specific TI DSP starter kit as well as an MSP430-based microprocessor as mentioned in section 1 of this manual. Using the interface card alleviates the task of building customize cables and allows easy configuration of a simple evaluation system.

This DAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP. For more information regarding the serial interface of the particular DAC installed, see the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user's guide.

7.3 EVM Stacking

Stacking of the EVM is possible if there is a need to evaluate two DAC7631 to yield a total of two channel outputs. A maximum of two DAC7631 EVMs are allowed because the output terminal, J4, dictates the number of DAC channels that can be connected without the outputs colliding. Table 3 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2.

Table 3. DAC7631 Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC7631 output (V_{OUT}) is routed to J4-2.
	2-3	DAC7631 output (V_{OUT}) is routed to J4-4.

7.4 The Output Operational Amplifier

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation because the odd numbered pins (J4-1 and J4-3) are tied together. The output operational amplifier is set to unity gain configuration by default. Nevertheless, the raw outputs of the DAC can be probed through the even pins of the output terminal J4, which also provides mechanical stability when stacking or plugging into any interface card. In addition, it provides easy access for monitoring up to two DAC channels when stacking two DAC7631 EVMs together; see the *EVM Stacking* section.

The inverting input of U2 can be tied to AGND (via W15) or the DAC output (by shorting pins 1 and 2 of the J5 header) or to any voltage source through J5-1.

The following sections describe the different configurations of the output amplifier, U2.

7.4.1 Unity Gain Output (Default Configuration)

The buffered output configuration can be used to prevent loading the DAC though it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply removing R6 and C12 and replacing it with the desired values. The user can also remove R6 and C12 and solder a 0-Ω resistor in place of R6.

Table 12 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar supply mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Position		Function
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U2, from AGND.
W5	2-3	1-2	Negative rail of operational amplifier is tied to AGND or powered by V_{SS}.

7.4.2 Output Gain of Two

Table 5 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Position		Function
	Unipolar	Bipolar	
W15	CLOSED	CLOSED	Inverting input of the output operation amplifier, U2, is connected to AGND to set for a gain of 2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operation amplifier, U2, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

7.4.3 Output Gain of Five With DAC V_{OUT} Inverted

Table 6. Jumper Settings for a Gain of Five With Inverted Output

Reference	Jumper Position		Function
	Unipolar	Bipolar	
J5	1-2 & 3-4	1-2 & 3-4	Output of DAC is inverted with a gain of 5. Watch for clipping in unipolar mode due to operational amplifier headroom issue.
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U2, from AGND.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

7.5 Digitally Programmable Current Source Application

A digitally programmable, unidirectional current-source circuit is added for the convenience of users who find the need for this type of application. Basically, the output of the DAC7631 can be connected to either the base of transistor, Q1 or the current input pin of the XTR115, U4A, via jumper W6. The sense pin of the DAC7631 should be connected to the emitter side of transistor Q1 via jumper W9, if used. If the XTR115, U4A, is selected to do this operation, the sense pin of the DAC7631 should be tied back to the VOUT pin via jumper W8. The jumper, W7, must be ensured in the position of 2-3 for the REF1 to drive the reference voltage of the DAC7631. A simple configuration of this setup is shown in Figure 10.

To operate the DAC7631 for the digitally programmable, unidirectional current-source application, the DAC7631 must be configured for the unipolar mode of operation. For a 4-mA to 20-mA operation, the VREFL input must be set to accept 500 mV, which can be externally provided through the –REFin input via J4-18. The jumper, W11, should be positioned to 2-3 to pass the voltage through.

The VREFH can take its input from REF1 via jumpers, W7 and W10.

See Table 7 for the setup configuration.

Table 7. Digitally Programmable Current Source Configuration

Reference	Jumper Position		Function
	Q1	U4A	
W2	OPEN	OPEN	Disconnect V_{OUT} from J4 header
W6	1-2	2-3	Routes V_{OUT} to selected device for current operation
W7	2-3	2-3	Routes REF1 to source $V_{REF}H$ of DAC7631
W8	OPEN	CLOSED	Configures the DAC7631 output for proper operation
W9	CLOSED	OPEN	Configures the DAC7631 output for proper operation
W10	1-2	1-2	Routes REF1 to source $V_{REF}H$ of DAC7631
W11	2-3	2-3	Routes –REFin to source $V_{REF}L$ of DAC7631

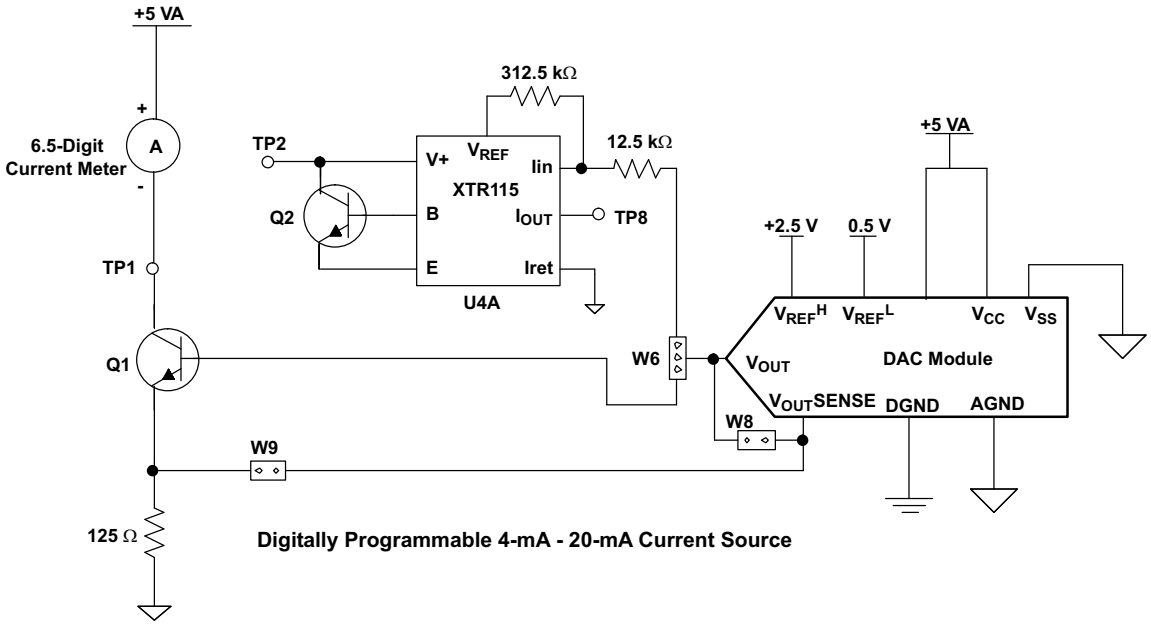

Figure 10. Digitally Programmable Current Source

7.6 Jumper Setting

Table 8 shows the function of each specific jumper setting of the EVM.

Table 8. Jumper Setting Function

Reference	Jumper Setting	Function
W1		LDAC driven by GPIO4 pin, J2-14.
		LDAC driven by GPIO0 pin, J2-2.
W2		Routes DAC V_{OUT} to J4-2.
		Routes DAC V_{OUT} to J4-4.
W3		Chip Enable pin driven by $\overline{CS}$ pin, J2-1.
		Chip Enable pin driven by FSX pin, J2-7.
W4		LOAD driven by GPIO5 pin, J2-19.
		LOAD driven by GPIO1 pin, J2-6.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		V_{OUT} is used for 4-mA to 20-mA operation to drive Q1.
		4-mA to 20-mA application is not used.
		V_{OUT} is used for 4-mA to 20-mA operation to drive U4A.
W7		U4A is used to supply external voltage reference to the DAC7631 DUT.
		REF1 is used to supply external voltage reference to the DAC7631 DUT.

Table 8. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
W8		4-mA to 20-mA operation is used with Q1 for current source.
		4-mA to 20-mA operation is used with U4A for current source.
W9		4-mA to 20-mA operation is used with U4A for current source.
		4-mA to 20-mA operation is used with Q1 for current source.
W10		REF1 or U4A supplies the external reference for $V_{REF}H$ of DAC7631.
		+REFin supplies the external reference for $V_{REF}H$ of DAC7631.
W11		REF1 or U4A supplies the external reference for $V_{REF}L$ of DAC7631 via U5.
		–REFin supplies the external reference for VREFL of DAC7631.
W14		RST_ is pulled up via R5 resistor.
		RST_ is pulled down to DGND and device is held on reset state.
W15		Configures output operational amplifier, U2, to unity gain output.
		Configures the output operational amplifier, U2 with an inverting gain of two.
W16		RSTSEL is pulled up via R13 resistor and device resets to midscale on powerup.
		RSTSEL is pulled down to DGND and device resets to minimumscale on powerup.
W20		Dual-supply operation (V_{SS} = –5VA).
		Single-supply operation (V_{SS} = AGND).

Table 8. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
J5		DAC V_{OUT} is routed to the inverting input of U2.
		DAC V_{OUT} is routed to the noninverting input of U2.
		The noninverting input of U2 is tied to AGND.
		DAC V_{OUT} is routed to the inverting input of U2 and the noninverting input of U2 is tied to AGND.
Legend:		Indicates the corresponding pins that are shorted or closed.

7.7 Schematics

The schematic is located on the following page.

Revision History		
REV	ECN Number	Approved

DAC_VOUT
J4
W2
Vout
-REFin
+REFin
+5VA
C7 0.1µF
C5 10µF
VDD
C6 10µF
C2 0.1µF
C8 0.1µF
R5 10K
R13 10K
U1
VCC
VDD
Vout
VoutSense
VrefH
VrefL
VrefHSense
VrefLSense
VSS
AGND
RST
RSTSEL
CS
CLK
LDAC
LOAD
SDI
SDO
DGND
DAC7631
W8
W14
W16
W3
W1
GPIO4
GPIO0
FSX
-5VA
C4 10µF
C1 0.1µF
W20
P2
J2
CS
SCLK
CLKR
FSX
FSR
SDI
DR
RST
RSTSEL
GPIO5
GPIO0
GPIO1
GPIO4
JP4
JP8
JP10
JP12
JP16
JP18
JP20
TP3
TP4
R7
R9
R10
W4
LOAD
TP1
Q1
MMBT3904_TRANS
VoutSense
W9
R1
125
REF1
REF3025
IN
GND
OUT
+5VA
+REFin
W10
W7
R2
10K
R16
312.5k
R15
12.5k
U4A
XTR115
Vref
Vreg
Iin
V+
Iret
B
Io
E
+5VA
-5VA
C14
C15
0.1µF
U5
OPA703
-REFin
W11
U3A
U3B
OPA2234
R11
100
R3
10K
R14
100
C16
2200pF
C13
C18
1000pF
C17
2200pF
C19
1000pF
VrefH
VrefL
VrefHSense
VrefLSense
VCC
VSS
C11
0.1µF
C10
0.01µF
C9
0.01µF
TP2
TP8
Q2
MMBT3904_TRANS
TP7
TP6
TP5
J5
DAC_VOUT
R8
2K
C3
470pF
U2
Op Amp
R4
100
W5
R6
10K
C12
1nF
W15
R12
10K
J6
+3.3VD
VD2
+5VA
VCC
VSS
-5VA
VD1
VDD
J1
J3
VSS
VCC
VDD
VD2

TEXAS INSTRUMENTS		
12500 TI Boulevard. Dallas, Texas 75243		
Title: DAC7631 EVM		
DOCUMENTCONTROL # 6464403		REV: A
DATE: 30-Nov-2004	SIZE:	SHEET: 1 OF: 1
Engineer: J. PARGUIAN		
Drawn By:		
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