TMS3637
Remote Control Transmitter/Receiver

Data Manual

SCTS037B
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TEXAS INSTRUMENTS

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1 Introduction

The TMS3637 is a versatile 3-V to 6-V remote control transmitter/receiver in a small package that requires no external dual-in-line package (DIP) switches on the system circuit board. The device can be easily set for one of many transmit/receive configurations using configuration codes along with the desired security code, both of which are user programmable. When used as a transmitter, the device encodes the stored security code, transmits it to the remote receiver using any transmission media such as direct wiring, infrared, or radio frequency. When configured as a receiver, the TMS3637 continuously monitors and decodes the transmitted security code (at speeds that can exceed 90 kHz) and activates the output of the device when a match with its internally stored code has been found. All programmed data is stored in nonvolatile EEPROM memory. With more than four million codes alterable only with a programming station, the TMS3637 is well suited for remote control system designs that require high security and accuracy. Schematics of the programming station and other suggested circuits are included in this data manual.

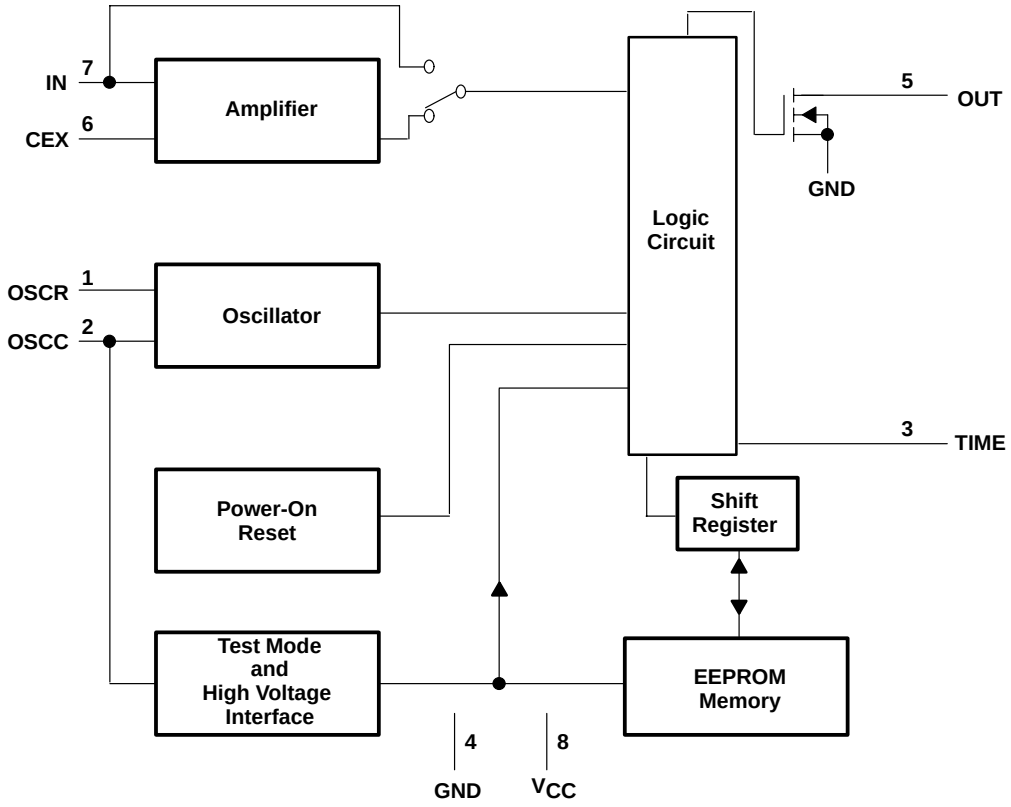
In addition to the device configuration and security code capabilities, the TMS3637 includes several internal features that normally require additional circuitry in a system design. These include an amplifier/comparator for detection and shaping of input signals as low as several millivolts (typically used when an RF link is employed) and an internal oscillator (used to clock the transmitted or received security code).

The TMS3637 is characterized for operation from –25°C to 85°C.

1.1 Features

- Data Encoder (Transmitter) or Data Decoder (Receiver) for Use in Remote Control Applications
- High Security
  - 4,194,304 Unique Codes Available
  - Codes Stored in Nonvolatile Memory (EEPROM)
  - Codes Alterable Only With a Programming Station That Ensures No Security Code Duplications
- Versatile
  - 48 Possible Configurations as a Receiver
  - 18 Possible Configurations as a Transmitter
  - Single, Multiple, or Continuous Cycling Transmission
- Easy Circuit Interface With Various Transmission Media
  - Direct Wired
  - Infrared
  - Radio Frequency
- Minimal Board Space Required: 8-Pin (D or P) Package and No DIP Switches
- Internal On-Chip Oscillator Included, No External Clock Required
- CMOS 2-μm Process Used for Very Low-Power Consumption and 3-V to 6-V Supply Voltage
- Well Suited for All Applications Requiring Remote-Control Operation
  - Garage Door Openers
  - Security Systems for Auto and Home
  - Electronic Keys
  - Consumer Electronics
  - Cable Decoder Boxes
  - Industrial Controls Requiring Precise Activation of Equipment
  - Electronic Serial Number (ESN) Device Identification

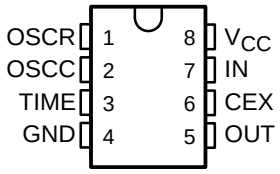
1.2 Functional Block Diagram



1.3 Terminal Assignments

D OR P PACKAGE

(TOP VIEW)



1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CEX	6	I	Capacitor external. CEX is used for gain control of the internal analog amplifier. An external capacitor connected from CEX to GND determines the gain of the amplifier. If the internal amplifier is set for unity gain or the device is not used as a receiver, CEX is left unconnected.
GND	4		Ground
IN	7	I/O	Depending on the device configuration, IN provides inverted OUT data, is used as a receiver input, or is used to enter data during programming. – When the device is configured as a transmitter, IN provides the complement of the OUT data stream and is considered to be noninverted. IN provides its own internal pullup, so no external pullup is required when IN is used to transmit the data. It is cleared to 0 in standby. – When the device is configured as a receiver, IN is used to receive the code. – When the device is in the program mode, IN is used to enter serial data into the device shift registers that load into the EEPROM memory.
OSCC	2	I/O	Oscillator capacitor. Depending on the configuration, OSCC is used for external transmit/receive clock input, control of the internal oscillator, to place the device into program mode, input for a high-voltage EEPROM programming pulse, or the internal analog amplifier in the test mode. – When the device is used as a transmitter or receiver using an external clock, the external clock is connected directly to OSCC. (OSCR must be held low to use an external clock.) – When the device is used as a transmitter or receiver and the internal oscillator is used, a capacitor from OSCC to GND and a resistor from OSCR to GND determines the free-running internal oscillator frequency. In addition, the internal oscillator triangular waveform can be seen at OSCC in this configuration. – When the device is in the data-loading phase of the programming mode, OSCC must be held at V_{CC} + 0.5 V. – After the device has been loaded with data in the programming mode, the internal registers transfer the data to the EEPROM permanently by applying a high-voltage programming pulse to OSCC. – When OSCC is held at V_{CC} + 0.5 V and three or more low pulses are applied to OSCR, the device is in the test mode and the output of the internal analog amplifier can be measured at TIME.
OSCR	1	I	Oscillator resistor. Depending on the configuration, OSCR is used as an external program/read clock input or to control the internal clock frequency. – When the device is in the program/read mode, OSCR is connected to an external clock. – When the device is in the transmit or receive mode, a resistor connected from OSCR to GND (along with a capacitor from OSCC to GND) determines the frequency of the internal clock.
OUT	5	O	OUT is an open-drain output. For that reason, it is necessary to connect a pullup resistor to OUT. Depending on the configuration, OUT provides transmit data, acts as the output for the receiver, or provides the serial output of the stored data in memory during the program and read modes. – When the device is configured as a transmitter, the transmitted data is seen at OUT and is in a 3-state output mode during standby (OUT is floating). While transmitting, the data from OUT is considered inverted. – When the device is configured as a valid transmission receiver (VTR) receiver, OUT provides a VTR pulse and goes low in the standby mode. – When the device is configured as a Q-state receiver, OUT toggles high and low each time a valid code is received. – During the program mode, OUT provides the current data from the EEPROM memory when the new data is clocked into the device.

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TIME	3	I/O	Depending on the configuration, TIME is used for measuring the internal analog-amplifier output in the device test mode, putting the device into the transmit mode, or controlling an internal clock oscillator for various transmitter and receiver configurations. – When OSCC is held at V_{CC} + 0.5 V and three or more low pulses are applied to OSCR, the device is in the test mode and the output of the internal analog amplifier can be measured at TIME. – When the device is configured as a continuous transmitter, an internal pullup is connected to TIME. If TIME is then forced low, the device transmits codes for the duration that TIME is held low. (TIME must be connected to an external pullup.) – When the device is configured as a triggered transmitter and if TIME is then forced low, the device transmits one code or a code train. (TIME must be connected to an external pullup.) – When the device is configured as a periodic transmitter, connect an external resistor and capacitor between TIME and V_{CC} to transmit code after each RC time constant has expired. – When the device is configured as a VTR, TIME must be held high to receive codes. The device produces a VTR pulse on OUT after confirmation of a correct received code. Connecting a parallel resistor and capacitor between TIME and V_{CC} lengthens the output pulse (VTR) duration. – Configured as a train receiver, connect an external parallel resistor and capacitor between TIME and V_{CC}, which are used to set the length of time the device is looking for two, four, or eight correct received codes to output a valid VTR pulse on OUT. – Configured as a Q-state receiver, TIME has the same function as the VTR receiver above, except the detection of the correct code causes OUT to toggle between the low and high states.
V_{CC}	8		5-V supply voltage

2 Specifications

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
Input voltage range (except OSCC), V_I . . . . . –0.6 V to V_{CC} + 0.5 V
Input voltage range, OSCC, V_I . . . . . –0.6 V to 15 V
Output voltage range, OUT, V_O . . . . . –0.6 V to 15 V
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

2.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3		6	V
High-level input voltage, V_{IH}	V_{CC}–0.5		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.5	V
Operating free-air temperature, T_A	–25		85	°C
Receiver supply current, analog, $I_{CC(an)}$			2	mA
Receiver supply current, digital, $I_{CC(dig)}$			200	µA
Transmitter supply current, standby, $I_{CC(stdby)}$			13	µA
Transmitter supply current, code transmission, $I_{CC(code)}$			260	µA
Programming current at OSCC, I_{OSCC}			100	µA
Oscillating period, t_{p0}+ t_{p1} (see Figure 3–1)	10	$1/(f_{osc})$	200	µs
Pulse duration, logic 1 bit, t_{w1} (see Figure 3–1)	5	t_{p1}	100	µs
Pulse duration, logic 0 bit, t_{w2} (see Figure 3–1)	35	3 x t_{p0} + 4 x t_{p1}	700	µs
Setup time, transmitter/receiver external clock on OSCC↓ and before IN↑, t_{su1} (see Figure 3–2)	152	$19 \times t_{w1}$ (receiver)		µs
Pulse duration, IN high, t_{w3} (see Figure 3–2)	48	$6 \times t_{w1}$ (receiver)	$R_{TIME} \times C_{TIME}$ (see Note 2)	µs

NOTES: 2. R_{TIME} is the value of the pullup resistor on TIME and C_{TIME} is the value of the capacitor in parallel with R_{TIME}. C_{TIME} should not exceed 3 µF.

2.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (unless otherwise noted)

2.3.1 Signal Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage, OUT	I_{OL} < 5 mA	0.5			V
	Low-level output voltage, OSCC		0.6		0.7	
V_{OH}	High-level output voltage, OUT	I_{OH} < 5 mA	V_{CC} – 0.5			V
	High-level output voltage, OSCC		1.2		1.6	
I_I	Input current, IN	V_I = 0 V to 6 V			±10	µA
I_O	Output current, OUT	V_O = 0 V to 12 V			±10	µA
C_i	Input capacitance			10		pF
C_o	Output capacitance			5		pF

2.3.2 Amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(PP)}$	Peak-to-peak input voltage		3			mV
$V_{N(PP)}$	External peak-to-peak noise voltage				1	mV
V_O	Output voltage, TIME		V_{OL}		V_{OH}	V
B	Bandwidth	V_I = 3 mV			15	kHz
		V_I = 100 $mV_{peak\ to\ peak}$			500	
		V_I = 200 $mV_{peak\ to\ peak}$			1000	
A_V	Flatband gain	CEX (nF) > 900/f_{osc} (kHz)		200		V/V
		CEX not connected		1		

2.3.3 Internal Oscillator (see Note 3)

PARAMETER		MIN	TYP	MAX	UNIT
f_{RX}	Receiver frequency	10		500	kHz
f_{TX}	Transmitter frequency	f_{RX}/10	f_{RX}/10	f_{RX}/5.5	kHz
	Frequency spread (temperature, V_{CC})			± 20%	

NOTE 3: Typical values are recommended whenever possible.

2.3.4 Power-On Reset

PARAMETER	MIN	MAX	UNIT
V_{CC} level required to trigger power-on reset		2.7	V
Power-on reset duration		40	ms

2.3.5 Write/Erase Endurance

PARAMETER	MIN	TYP	MAX	UNIT
Number of program cycles	20	10000		

2.4 Timing Requirements Over Recommended Ranges of Supply Voltages and Free-Air Temperature

2.4.1 Abort/Retry

	MIN	NOM	MAX
Time between consecutive codes		46 x t_W (transmitter)	
Time out for high-level bit to abort the code		3 x t_W (receiver)	
Time out for low-level bit to abort the code		25 x t_W (receiver)	
Time between aborted code and reading of new code		3 x t_W (receiver)	

2.4.2 EEPROM Read Mode (see Figure 3–3)

		MIN	MAX	UNIT
t_{su2}	Setup time, OSCR high after V_{CC} ↑	50		ms
t_{w4}	Pulse width, OSCR high	10		µs
t_{w5}	Pulse width, OSCR low	10		µs

2.4.3 EEPROM Write Mode (see Figure 3–3 and Figure 3–4)

		MIN	MAX	UNIT
t_{su3}	Setup time, OSCR high after V_{CC} high	50		ms
t_{w6}	Pulse duration, OSCR high	5		µs
t_{w7}	Pulse duration, OSCR low	5		µs
t_v	Valid time, data IN valid before OSCC↑	10		µs

2.4.4 Data Input Setup and Hold Times (see Figure 3–5)

		MIN	NOM	MAX	UNIT
t_{su4}	Setup time, data in before OSCR↓		1		µs
t_{h1}	Hold time, data in after OSCR↓		1		µs

2.5 Switching Characteristics Over Recommended Ranges of Supply Voltages and Free-Air Temperature (unless otherwise noted)

2.5.1 Normal Transmission – Internal Clock (see Figure 3–6)

PARAMETER		MIN	TYP	MAX	UNIT
t_{w8}	Pulse duration, half-oscillating period for OSCC sawtooth ↑↓	5	1/(2 x f_{osc})	100	µs
t_{w9}	Pulse duration, logic bit 1 for IN	5	t_W	100	µs
t_{w10}	Pulse duration, logic bit 0 for IN	35	7 x t_W	700	µs

2.5.2 Modulated Transmission – Internal Clock

PARAMETER		TEST CONDITIOINS	MIN	TYP	MAX	UNIT
$f_{osc(t)}$	Transmitter oscillator frequency		100	110	120	kHz
$f_{osc(r)}$	Receiver oscillator frequency		400	440	480	kHz
$t_{w(H)}$	Pulse duration, high-level modulation at IN	See Figure 3-7	9	1/$f_{osc(t)}$	10	µs
t_c	Cycle time, IN	See Figure 3-7	27	3 x $t_{w(H)}$	30	µs
$t_{c(total)}$	Total cycle time, IN	See Figure 3-7	135	5 x t_c	150	µs
t_{w11}	Pulse duration, logic bit 1 for IN	See Figure 3-7	135	5 x t_c	150	µs
t_{w12}	Pulse duration, logic bit 0 for IN	See Figure 3-7	945	7 x t_{w10}	1050	µs

3 Parameter Measurement Information

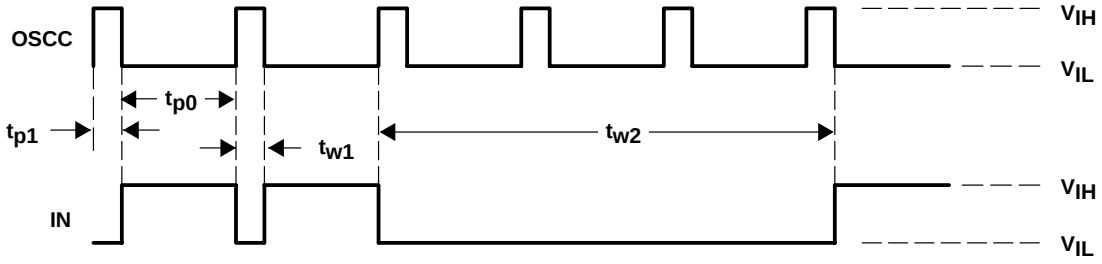


Figure 3–1. Normal Transmission – External Clock

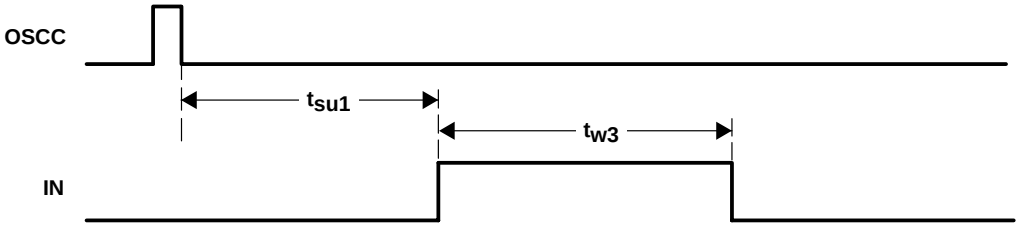


Figure 3–2. VTR Generation

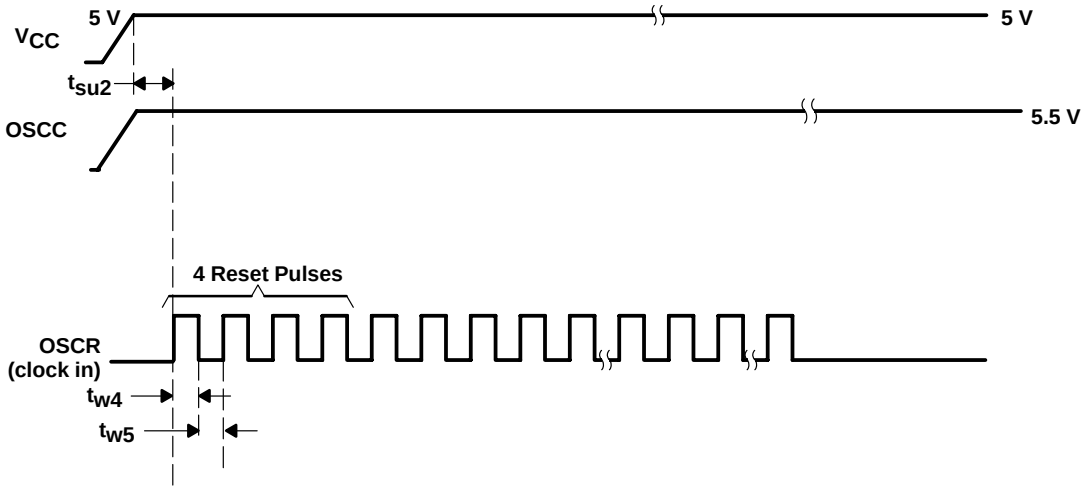


Figure 3–3. EEPROM Read Mode

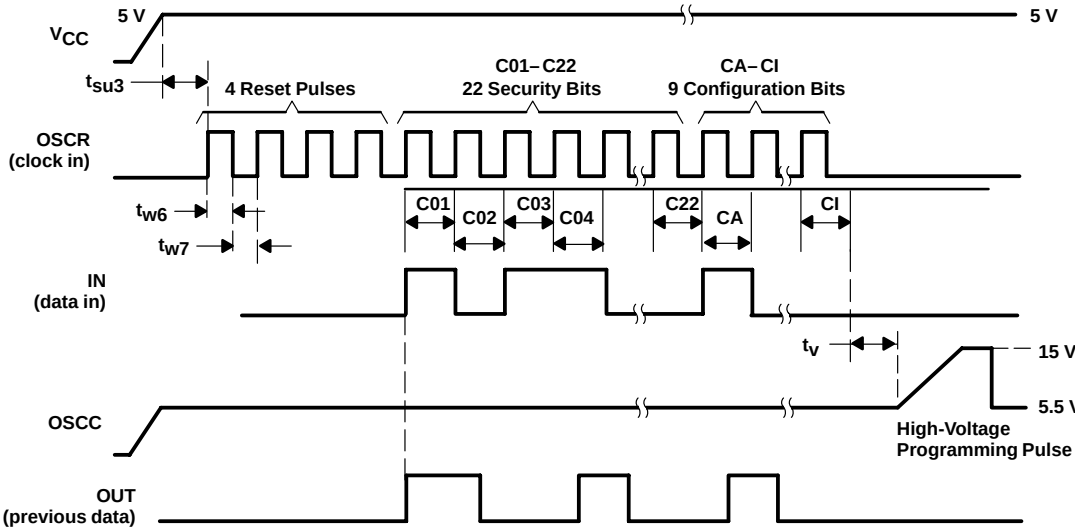


Figure 3–4. EEPROM Write Mode

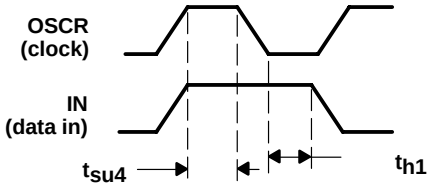


Figure 3–5. Data In Setup and Hold Times

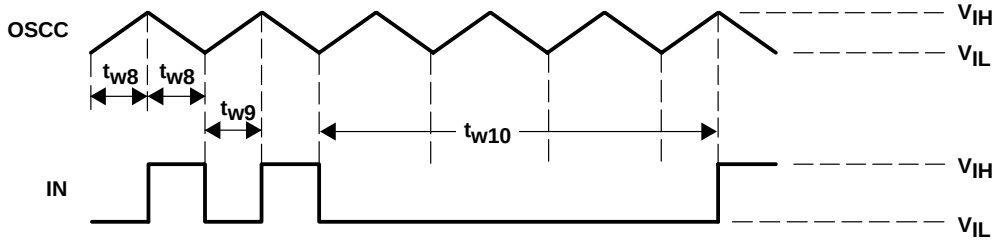


Figure 3–6. Normal Transmission – Internal Clock

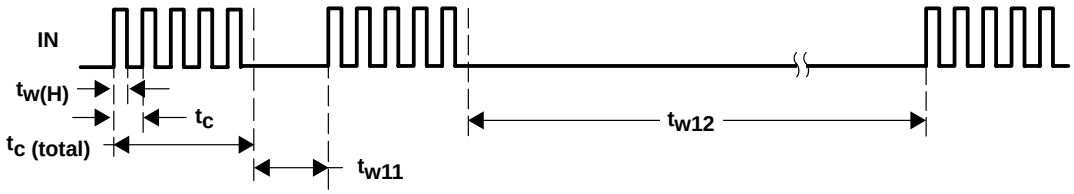


Figure 3–7. Modulated Transmission – Internal Clock

4 Typical Characteristics

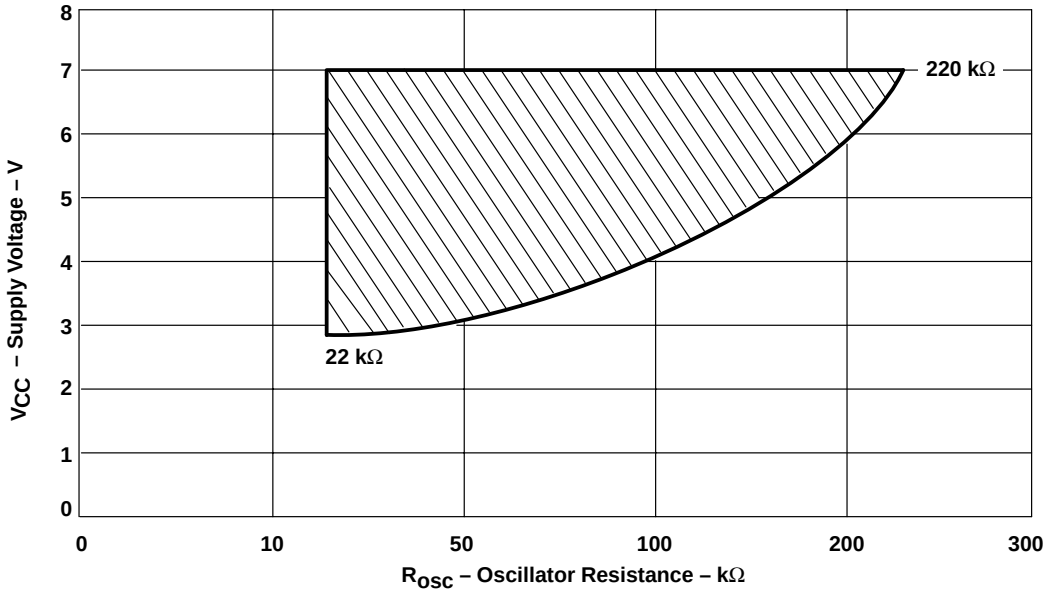


Figure 4–1. Oscillator Resistance Versus Supply Voltage

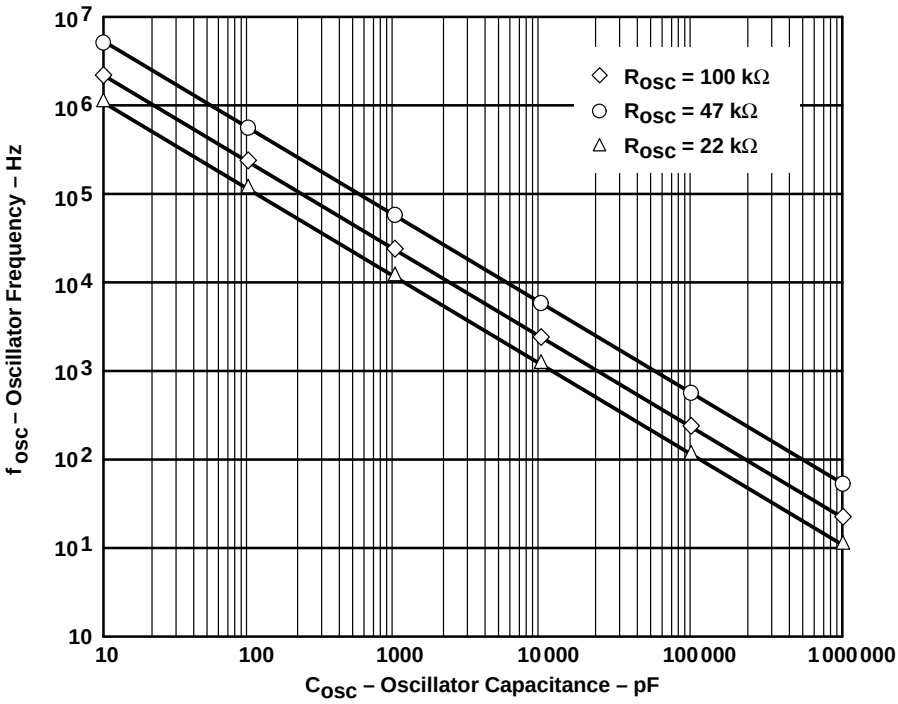


Figure 4–2. Oscillator Frequency Versus Oscillator Capacitance

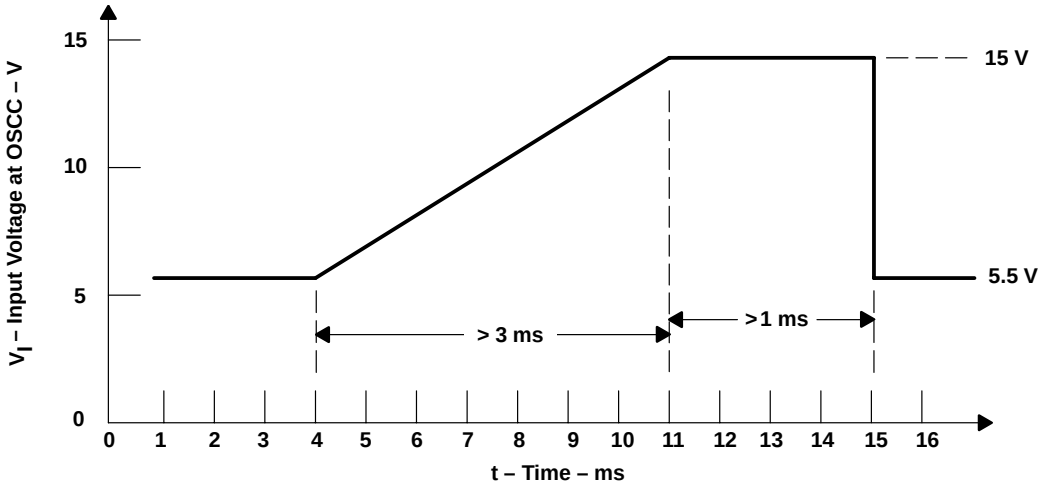


Figure 4–3. High-Voltage Programming Pulse

5 Principles of Operation

5.1 Power-On Reset

The power-on reset function starts when V_{CC} rises above 2.7 V and is completed after four clock periods. After power-on reset, the nine configuration bits contained in the EEPROM memory are loaded into the logic circuits, which determine the device mode and configuration of operation. For correct enabling of the power-on reset operation, it is necessary for V_{CC} to first fall below 2.3 V and remain in this condition for at least 0.5 ms.

5.2 EEPROM Memory (31 Bits)

The EEPROM memory contains a total of 31 bits. The first 22 of the 31 bits contain the security code. These 22 bits are named C01, C02,...C22, and are user definable. The last 9 bits of the total 31 bits are configuration bits named CA,CB,...CI, and are also user definable to select the mode of operation for the device.

5.2.1 Program Read Mode

The procedure described in the following steps is used to read the current contents of the EEPROM memory. This can verify that the correct 22 security codes and 9 configuration bits are stored in memory (see Figure 5–1):

1. Set V_{CC} to 5 V.
2. Apply V_{CC} + 0.5 V to OSCC. Wait at least 50 ms to allow the device to assume the read mode (t_{su2} > 50 ms). This voltage on OSCC forces the device into the read mode, and the terminals are in the following configuration:
   - OSCR: program/read external clock input
   - OUT: serial output of 31 data bits currently stored in EEPROM
3. Apply four reset pulses to OSCR ($t_{w4} = t_{w5} = 10\ \mu s$). This only needs to be done once during each read operation.
4. Apply 31 clock pulses to clock input OSCR ($t_{w4} = t_{w5}$ = 10 μs min). This clocks out the 31 data bits (C01,C02,...C22, and CA,CB,...CI) that are stored in memory. Output data changes state only on falling edge of clock pulses, except on data bit C01. If used, data bit C01 goes high on the rising edge of the clock pulse.

NOTE:
Each succeeding group of 31 clock pulses, when applied, clocks out the data again without any reset pulses required.

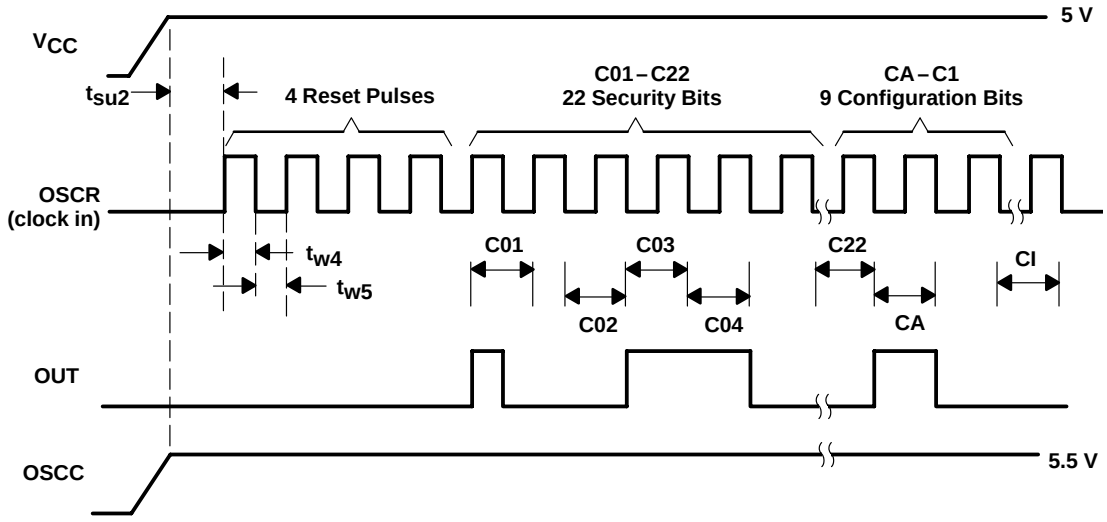


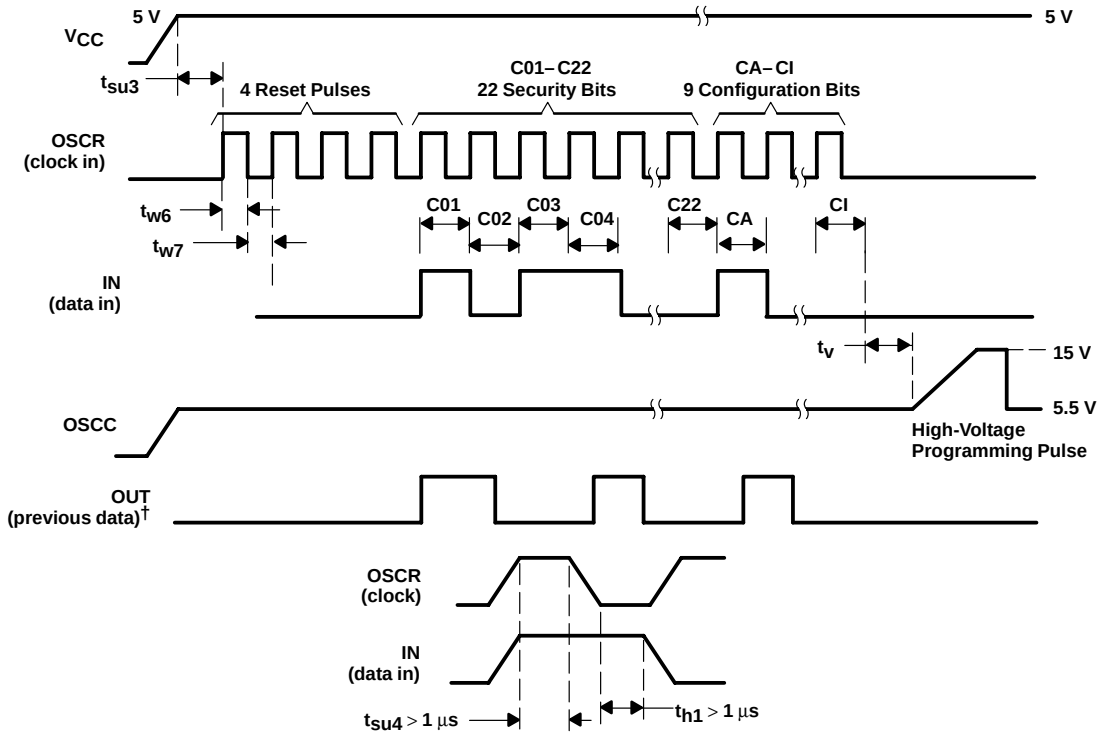
Figure 5–1. EEPROM Read Mode

5.2.2 Program Write Mode

The procedure to write the 31 security code and configuration bits to memory is described below (see Section 3 for timing diagram):

1. Set V_{CC} to 5 V.
2. Apply V_{CC} + 0.5 V to OSCC. This voltage on OSCC forces the device into the program mode, and the terminals are in the following configuration:
   - OSCR: program/read external clock input
   - OSCC: input for high-voltage programming pulse used to permanently store data in memory (see Figure 5–2).
   - OUT: serial output of 31 data bits currently stored in EEPROM
   - IN: serial input for 31 bits of data to be stored
3. After applying V_{CC} + 0.5 V to OSCC (step 2), wait at least 50 ms to allow device to go into the program mode.
4. Apply exactly four clock reset pulses to OSCR (clock input). These reset pulses are applied before clock input pulses for the 31 data bits that contain the security code and configuration bits. The minimum duration of the clock reset pulses must be $t_{w6} = t_{w7} = > 5$ μs, which equates to a clock frequency <100 kHz.
5. Apply exactly 31 clock input pulses to OSCR. This serves to clock in the 31 data bits that should be applied to IN (C01,C02,...C22, and CA,CB,...CI). Each of the 31 data bits must be present on the falling edges of the clock input pulses applied to OSCR with the setup and hold times being 1 μs minimum.
6. The data at OUT is previous data that was stored in EEPROM before this operation. If the device has never been programmed, this data is a random factory test code. The newly programmed data can be read only after it is loaded.
7. Apply a logic low to OSCR for at least 10 μs.

8. After a minimum valid time of t_v = 10 µs, apply the high-voltage programming pulse to permanently store the 31 code bits in EEPROM memory as shown in Figure 5–2. As stated in steps 4 and 5, exactly 4 reset and 31 clock pulses must be applied for the device to successfully program. The device does not transfer the code from its registers into the EEPROM if less than or greater than 4 reset and 31 clock pulses are used before the programming pulse is applied.



† Previous data refers to data that was previously programmed into the device. If programmed for first time, this contains a random test code from the factory.

Figure 5–2. EEPROM Write Mode

5.3 Internal Oscillator Operation for Transmit and Receive Modes Setting Frequency

The TMS3637 has an internal oscillator that can be used in either the transmit or receive configurations of the device. The oscillator free-running frequency (f_{osc}) is controlled by an external resistor and capacitor and is determined by:

$$f_{osc} = 5 / (4 \times C_{osc} \times R_{osc}) \quad (1)$$

where

C_{osc} = capacitor from OSCC to GND
R_{osc} = resistor from OSCR to GND

The allowable oscillation range or R_{osc} versus V_{CC}, and associated f_{osc} values, and range versus C_{osc} for three given values of R_{osc} are given in Section 4.

5.4 Internal Oscillator Operation for Transmit and Receive Modes Sampling Frequency

The internal oscillator of the transmitter or receiver can be externally sampled at OSCC and OSCR. The waveform at OSCC is triangular and the waveform at OSCR is square. The amplitude of these waveforms depends on the capacitor and resistor values used.

5.5 External Oscillator Operation for Transmit and Receive Modes

Instead of using the internal oscillator (with an external resistor and capacitor) in the transmit or receive modes, it is possible to externally drive the device by applying a logic level clock to OSCC. When an externally driven oscillator is used, OSCR must be held to GND. To avoid entering the test/program modes, ensure that the external clock applied to OSCC does not exceed V_{CC} (for more information see Section 5.12).

5.6 Internal Amplifier/Comparator, Description and Gain Setting

The TMS3637 has an internal amplifier that is designed to amplify received signals up to logic levels. In addition, a comparator is cascaded with the amplifier to provide wave shaping of received signals. The comparator also inverts the signal. The minimum received signal strength must be at least 3 mV peak-to-peak (see Figure 5–3 for a schematic of the amplifier/comparator section). The amplifier is enabled only when the TMS3637 is configured as an analog receiver. When the amplifier is not configured as an analog receiver, it is disabled and bypassed to reduce power consumption in any of the three logic receiver modes. A capacitor connected between CEX to GND determines the gain of the amplifier stage. When no capacitor is connected from CEX to GND, the amplifier assumes unity gain and the comparator still functions to shape the received signal. When the internal amplifier is used, it is usually run at the maximum gain of 200. The maximum gain is set by resistances internal to the device as shown in the equation 2. However, to achieve this maximum gain, a low impedance from CEX to GND must exist. Equation 2 defines the capacitance necessary at CEX for maximum gain at different oscillator frequencies (f_{osc}):

$$CEX > 1 / (6.28 \times f_{osc} \times R1) \quad (2)$$

where:

CEX = capacitance required for maximum gain
R1 = 178 Ω (set internally)

With a low impedance between GND and CEX, note that the maximum gain is derived from the noninverting operational amplifier gain equation, (see Figure 5–3):

$$Gv = 1 + R2/R1 = 200 \quad (3)$$

where:

R1 = 178 Ω (set internally)
R2 = 35.5 kΩ (set internally)

If a capacitor is used at CEX, but maximum gain is not desired, equation 4 can determine the gain for any value of CEX:

$$Gv = \sqrt{\left(\frac{1 + 4\pi^2 f_{osc}^2 CT^2 (R1 + R2)^2}{1 + 4\pi^2 f_{osc}^2 CT^2 R1^2}\right)} \quad (4)$$

where:

f_{osc} = oscillator frequency of transmitter (it is the transmitted frequency that is being amplified)
C_T = CEX + 0.15 nF (there is an internal capacitance of 0.15 nF at CEX)
R1 = 178 Ω (set internally)
R2 = 35.5 kΩ (set internally)

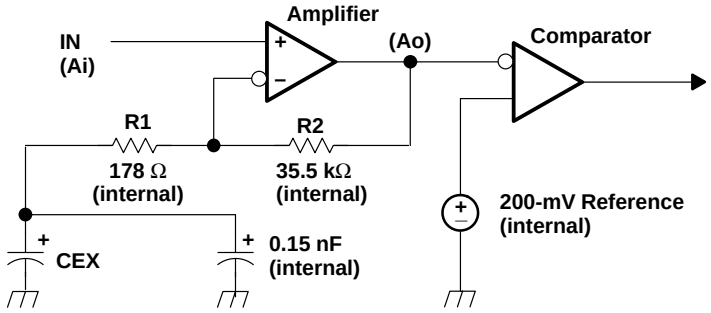


Figure 5–3. Amplifier/Comparator Schematic

5.7 Internal Amplifier/Comparator Test Mode

Normally, the output of the amplifier/comparator section is fed directly to the logic circuitry internal to the device; however, the output of the amplifier/comparator can be sampled external to the device during the amplifier test mode to determine if the amplitude and shape of the received signal is acceptable for the application. To enter the amplifier test mode, apply V_{CC} + 0.5 V to OSCC and apply three or more low-level pulses to OSCR. This can be done by simply brushing a wire connected from OSCR to GND. The output of the amplifier stage is then connected internally to TIME, where it can be sampled for evaluation purposes.

5.8 Mode and Configuration Overview

The TMS3637 device is designed to function in many modes and configurations. The device has five primary modes of operation as shown in Table 5–1.

Table 5–1. Mode and Test Configuration

MODE	DESCRIPTION
1	Amplifier Test
2	Program
3	Read
4	Transmitter
5	Receiver

In the transmitter and receiver modes (see Tables 5–2 and 5–3), there are a total of 66 configurations available, 48 in the receiver mode and 18 in the transmitter mode.

Table 5–2. Transmitter Modes

NO. OF MODES	CONFIG.	OSCR (PIN 1)	OSCC (PIN 2)	TIME (PIN 3)	OUT (PIN 5)	CEX (PIN 6)	IN (PIN 7)	C1–C22 ABCDEFG HI	CA–CI ABCDEFG HI†
1	Normal Continuous	External clock or resistor to GND (internal clock)	Capacitor to GND (internal clock) and output of the internal clock triangular waveform	Starts transmitting when low	Serial output of currently stored data	N/C	N/C	Transmit data from memory	11100000X
1	Normal Triggered								110DE0001
1	Normal Periodic								110DE0000
1	Modulated Triggered								100DE0001
1	Modulated Continuous								10100000X
1	Modulated Periodic								100000000
3	Code Train Normal Triggered								110DE0001
3	Code Train Normal Periodic								110DE0000
1	Code Train Modulated Triggered								100DE0001
3	Code Train Modulated Periodic								100DE0000

† X = don't care and can be held high or low

Table 5–3. Receiver Modes

NO. OF MODES†	CONFIG.	OSCR (PIN 1)	OSCC (PIN 2)	TIME (PIN 3)	OUT (PIN 5)	CEX (PIN 6)	IN (PIN 7)	C1–C22 ABCDEF GHI	CA–CI ABCDEFG HI‡
2	Analog Normal VTR	External clock or resistor to GND (Internal clock)	Capacitor to GND (Internal clock)	Requires a high-to-enable receiver or a resistor and capacitor in parallel connected between V_{CC} and ground to lengthen the OUT pulse. When operated in periodic mode, a resistor and capacitor in parallel connected between V_{CC} and ground causes a reset.	Serial output of currently stored data and configuration data	Capacitor to GND for receiver analog amplifier gain	Receive signal input	Data received	010XX010I
6	Analog Normal Train								010DE011I
8	Analog Normal Q-state								010DE000I
2	Modulated VTR								000XXX10I
6	Modulated Train								000DEX11I
8	Modulated Q-state								000DEX00I
2	Logic Normal VTR					N/C			010XX110I
6	Logic Normal Train								010DE111I
8	Logic Normal Q-state								010DE100I

† Number of modes refers to total possible modes for that configuration: includes noninverting or inverting and number of codes (train).
‡ X = don't care and can be held high or low, I = 1 inverting, I = 0 for noninverting

The multitude of transmit and receive configurations are discussed in subsection 5.10.3 and Section 5.12. A reference for the quick, correct programming of the device in the desired mode and configuration is discussed in Section 5.12. Table 5–4 lists the signals required to set the amplifier test, program, and read modes.

Table 5–4. Amplifier Test, Program, and Read Modes

MODE	NO. OF MODES †	CONFIG.	OSCR (PIN 1)	OSCC (PIN 2)	TIME (PIN 3)	OUT (PIN 5)	CEX (PIN 6)	IN (PIN 7)	C1–C22 ABCDE FGHI	CA–CI ABCDE FGHI
Amplifier Test	1	Amplifier Test	3 or more low pulses	V_{CC} + 0.5 V	Internal amplifier out	N/C	Capacitor to GND (for gain)	Receive signal input	X‡	X‡
Program	1	Program	External clock	V_{CC} + 0.5 V and high voltage programming pulse (ramp to 15 V)	N/C	Serial out of previous data	N/C	New serial data and configu-ration input	Data to be stored	Configu-ration to be stored
Read	1	Read EEPROM	External clock	V_{CC} + 0.5 V	N/C	Serial out of stored data	N/C	N/C	Stored data	Stored configu-ration

† Number of modes refers to total possible modes for that configuration; which includes noninverting mode or inverting mode and number of train codes.
‡ X = don't care and can be held high or low

5.9 Transmitter Configurations

Of the total 31 data bits that are stored by the TMS3637, the last nine (CA through CI) configure the device in one of 18 possible transmitter configurations. The device can run continuous, triggered, or periodic in transmission. In addition, each of these functions can have a single, pulse, or train output in both normal and modulated configurations. (For a definition of which configuration bits to set for all possible 18 transmitter configurations, see subsection 5.10.3.) To enter any transmitter configuration, always start by setting EEPROM bits CA = 1 and CF = CG = CH = 0.

When OUT transmits the code, the code is considered to be inverted. OUT also requires an external pullup resistor. When IN transmits the code, the code is the complement of OUT and is considered noninverted. An internal pullup resistor is connected to IN, so no external pullup is required when it transmits the code.

5.9.1 Continuous Transmitter (CC = 1)

When the device is configured as a transmitter (CA = 1, CF = CG = CH = 0) and the EEPROM bit CC is set to 1, the chip is programmed to function as a continuous transmitter. In this condition, the TMS3637 serially transmits the same code indefinitely. The transmit sequence is enabled by setting TIME to low. TIME is externally connected to a pullup resistor, so a simple switch between TIME and GND can force TIME low. The code transmission continues as long as TIME is kept low. When TIME returns to high, the transmission of the code is completed and the transmitter is disabled. The oscillator is consequently inhibited, and the power consumption is reduced to the standby value (13 μA). The time between two consecutive codes (tbc) during the transmission is equal to 57 pulse durations (tbc = 57 t_{w8}, see Figure 3–6). The continuous transmitter must be operated in either the normal (CB = 1) or modulated (CB = 0) modes.

5.9.2 Triggered Transmitter (CC = 0, CI = 1)

When the chip is configured as a transmitter (CA = 1, CF = CG = CH = 0) and EEPROM bits CC and CI low and high, respectively, the chip is programmed to work as a triggered transmitter. The TMS3637 transmits a single code or a code train when TIME is forced low, and then the device enters the standby mode. In order to retransmit a code, TIME must be taken high (or opened) and then forced low again. The triggered transmitter must be operated in either the normal (CB = 1) or modulated (CB = 0) modes.

5.9.3 Periodic Transmitter (CC = 0, CI = 0)

When the chip is configured as a transmitter (CA =1, CF = CG = CH = 0) and the EEPROM bits CC and CI are cleared to 0, the chip is programmed to work as a periodic transmitter. In this case, the internal pullup resistor on TIME is disconnected and TIME is externally connected to V_{CC} through a parallel RC. The TMS3637 transmits one code or a code train and goes into the standby mode. After a time equal to one RC time constant, the TMS3637 is enabled and transmits the code again. The TMS3637 then enters the standby mode and repeats the process. During the code transmission, the external capacitor is loaded by V_{CC}. During the standby mode, it is discharged through the resistor. The transmission cycle starts again when the capacitor voltage falls below the trigger value of TIME. In this way, it is possible to obtain a very low average value of I_{CC}. Typically, it is possible to obtain I_{CC} = 1.5 μA at a transmission frequency of 2 Hz. The periodic transmitter must be operated in either the normal (CB = 1) or modulated (CB = 0) modes.

5.10 Transmitter Modes

In addition to the three transmitter configurations discussed previously, the TMS3637 transmitter can operate in four modes: normal, continuous, triggered, and periodic. The following paragraphs describe the configuration bit setting required to place the TMS3637 in each of the four modes.

5.10.1 Normal Mode (CB = 1)

When the chip is configured as a continuous transmitter (CA = 1, CF = CG = CH = 0, and CC = 1), as a triggered transmitter (CA = 1, CF = CG = CH = 0, and CC = 0, CI = 1), or as a periodic transmitter (CA = 1, CF = CG = CH = 0, and CC = 0, CI = 0), and EEPROM bit CB is set to 1, the TMS3637 operates as a normal transmitter and emits the stored code on OUT (the open drain requires a pullup resistor). The format for the code appearing on OUT is:

- Each code transmission consists of a 3-bit precode (010) or sync word followed by 22 data bits (C1 through C22) stored in the EEPROM.
- A bit code 1 is represented high with a duration of t_1, and a bit code 0 is represented high with a duration of $t_2 = 7\ t_1$.

An example of OUT is shown in Figure 5–4.

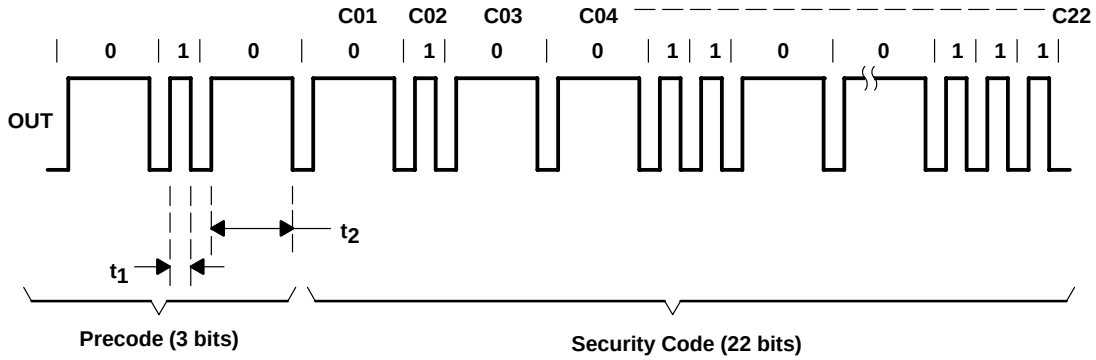


Figure 5–4. OUT Waveform in Normal Transmission

5.10.2 Modulated Mode (CB = 0)

When the chip is configured as a continuous transmitter (CA = 1, CF = CG = CH = 0, and CC = 1), as a triggered transmitter (CA = 1, CF = CG = CH = 0, and CC = 0, CI = 1), or as a periodic transmitter (CA = 1, CF = CG = CH = 0, and CC = 0, CI = 0), and EEPROM bit CB clears to 0, the device is programmed to function as a modulated transmitter. The oscillator frequency must be 120 kHz.

In the modulated mode, a bit code 1 is represented high with a pulse width of $t_3 = t_4$. A bit code 0 is represented by a high of $t_0 = 7\ t_4$ as in the normal mode, except that the bit codes are each separated by a pulse train composed of five elementary pulses. The total duration of $t_4 = 125\ \mu s$ as shown in Figure 5–5.

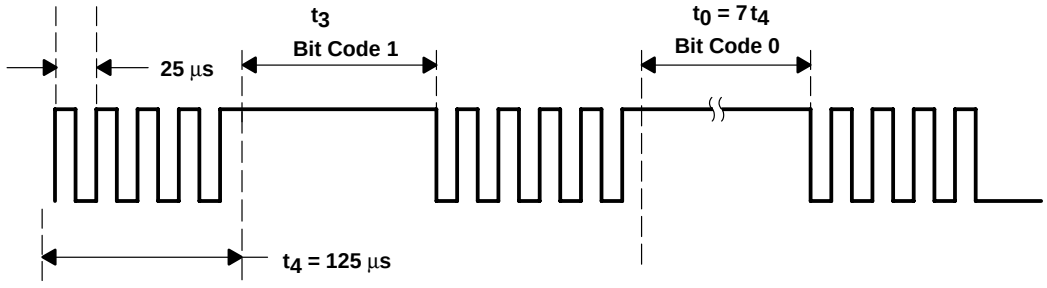


Figure 5–5. OUT Waveform in Modulated Mode

5.10.3 Code-Train Mode (CD, CE)

When the chip is configured as a triggered transmitter (CA = 1, CF = CG = CH = 0, and CC = 0, CI = 1) or as a periodic transmitter (CA = 1, CF = CG = CH = 0 and CC = 0, CI = 0), it can transmit the stored code two, four, or eight times, depending on the values stored in bits CD and CE as shown in Table 5–5 and Figure 5–6.

Table 5–5. Code-Train Modes

CD	CE	TRAIN
1	0	2 codes
0	1	4 codes
1	1	8 codes

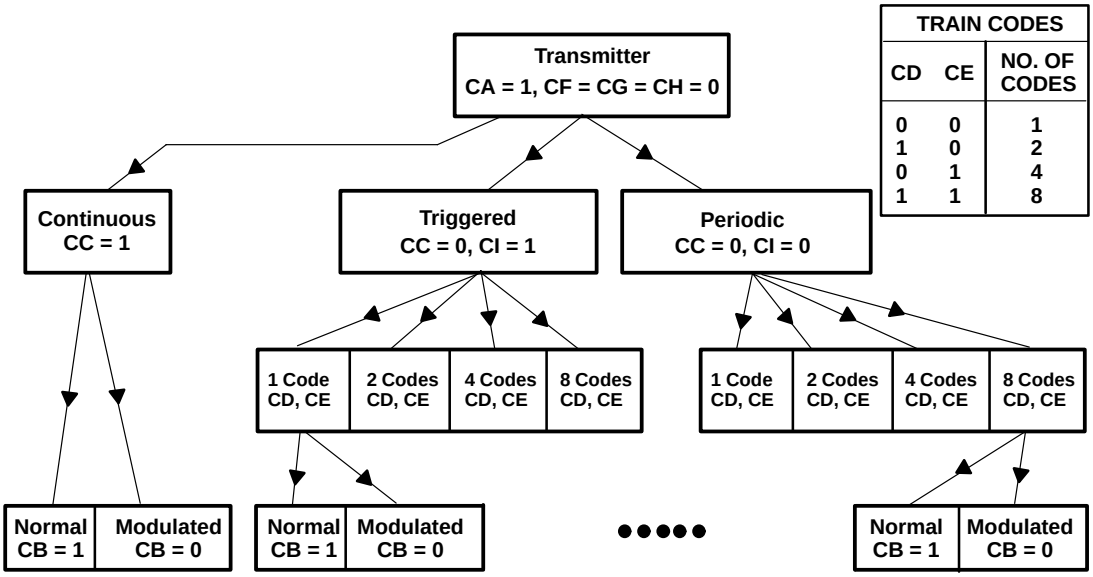


Figure 5–6. Transmitter Configurations

5.11 Receiver Configurations

As with the transmitter configurations, the TMS3637 uses the last nine bits of the 31 data bits stored in memory to program the device for a multitude of receiver configurations (48 possible configurations). The configuration must match the transmitter when selecting the receiver configuration (see Table 5–6 to determine compatible transmitter and receiver combinations). The definition of which configuration bits to set for all the possible 48 receiver configurations is discussed in Section 5.12.

In the receive mode, the TMS3637 receives the transmitted code on IN and compares the code with the code stored in memory. When the two codes are equal, a valid transmission pulse is sent to OUT. To have reliable reception of the transmitted code, the receiver clock frequency must be approximately seven times greater than the clock frequency for the transmitter clock. To set any receiver configuration in the receiver mode, always start by clearing the EEPROM bits CA = CC = 0.

Table 5–6. Transmitter/Receiver Compatibility†

RCVR / XMITTER	ANALOG NORMAL VTR	ANALOG NORMAL TRAIN	ANALOG NORMAL Q-STATE	MODULATED VTR	MODULATED TRAIN	MODULATED Q-STATE	LOGIC NORMAL VTR	LOGIC NORMAL TRAIN	LOGIC NORMAL Q-STATE
Normal Continuous	X	X	X				X	X	X
Normal Triggered	X	X	X				X	X	X
Normal Periodic	X	X	X				X	X	X
Modulated Continuous				X	X	X			
Modulated Triggered				X	X	X			
Modulated Periodic				X	X	X			
Code Train Normal Triggered	X	X	X				X	X	X
Code Train Normal Periodic	X	X	X				X	X	X
Code Train Modulated Triggered				X	X	X			
Code Train Modulated Periodic				X	X	X			

† X denotes compatible transmitter/receiver combinations.

5.11.1 Valid Transmission Receiver (CG = 1, CH = 0)

When the TMS3637 is configured as a receiver (CA = CC = 0) and the configuration bits CG = 1 and CH = 0, the device is configured as a valid transmission receiver. Bits CB, CF, and CI must also be set to specify modulated or normal modes, analog or logic (for normal mode only), and noninverting or inverting format of the output code. Other receiver modes are discussed in Section 5.12.

In the valid transmission receiver (VTR) configuration, an external pullup resistor is connected to TIME. When the TMS3637 recognizes the received code as correct, it produces a high pulse (VTR pulse) on OUT. The VTR output pulse duration is equal to 48 times the pulse duration of the received data and is produced after a delay time equal to $152 \times 2/f_{osc}$ from the end of the received code. If a capacitor is added in parallel to the pullup resistor on TIME, the VTR pulse duration on the output terminal can be increased according to a quantity determined by the time constant of RC. By choosing a large capacitor value (no greater than 1 μF), it is possible to have a VTR output pulse duration of up to several seconds. When the VTR duration is longer than the repetition period of received codes, the VTR has a duration as long as that of the correct received code.

5.11.2 Train Receiver (CG = 1, CH = 1, CD, CE)

When the TMS3637 is configured as a receiver (CA = CC = 0) and EEPROM bits CG and CH are both set to 1, the device is configured as a train receiver. Bits CB, CF, and CI must also be set to specify modulated or normal modes, analog or logic (for normal mode only), and noninverting or inverting format.

In the train-receiver configuration, the device outputs a VTR pulse on OUT only after the reception of two, four, or eight received codes that occur within one period of the train code counter oscillator. This feature

further increases the security of the device by not recognizing the correct received code until it is repeated two, four, or eight times within a period of time specified by an external RC combination described in the following paragraphs.

When the TMS3637 is configured as a train receiver, connect an external resistor and capacitor in parallel between TIME and V_{CC}, which sets the length of time the device searches for two, four, or eight correct received codes. When the device receives two, four, or eight correct codes (not necessarily in succession) within the time constant of the external RC network, a valid VTR pulse is placed on OUT at the conclusion of the RC time constant.

The number of codes in the train required is determined by the setting of bits CD and CE as shown in Table 5–7.

Table 5–7. Bits CD and CE in Train Receiver

CD	CE	TRAIN
1	0	2 codes
0	1	4 codes
1	1	8 codes

5.11.3 Q-State Receiver (CG = 0, CH = 0, CD, CE)

When the TMS3637 is configured as a receiver (CA = CC = 0) and EEPROM bits CG and CH are both cleared to 0, the device is configured as a Q-state receiver. Bits CB, CF, and CI must also be set to specify modulated or normal modes, analog or logic (for normal mode only), and noninverting or inverting format of the output code.

The Q-state receiver is similar to a train receiver, except that when a train of one, two, four or eight codes are recognized as valid, OUT toggles. After power-on reset, OUT is floating, since OUT is an open-drain output. As with the train receiver, OUT can change value only after the RC time constant present on TIME.

Use Table 5–8 to determine the setting of bits CD and CE.

Table 5–8. Bits CD and CE in Q-State Receiver

CD	CE	TRAIN
0	0	1 code
1	0	2 codes
0	1	4 codes
1	1	8 codes

5.12 Receiver Modes

Figure 5–7 shows all possible receiver combinations. The bit values are also shown that determine the mode of operation.

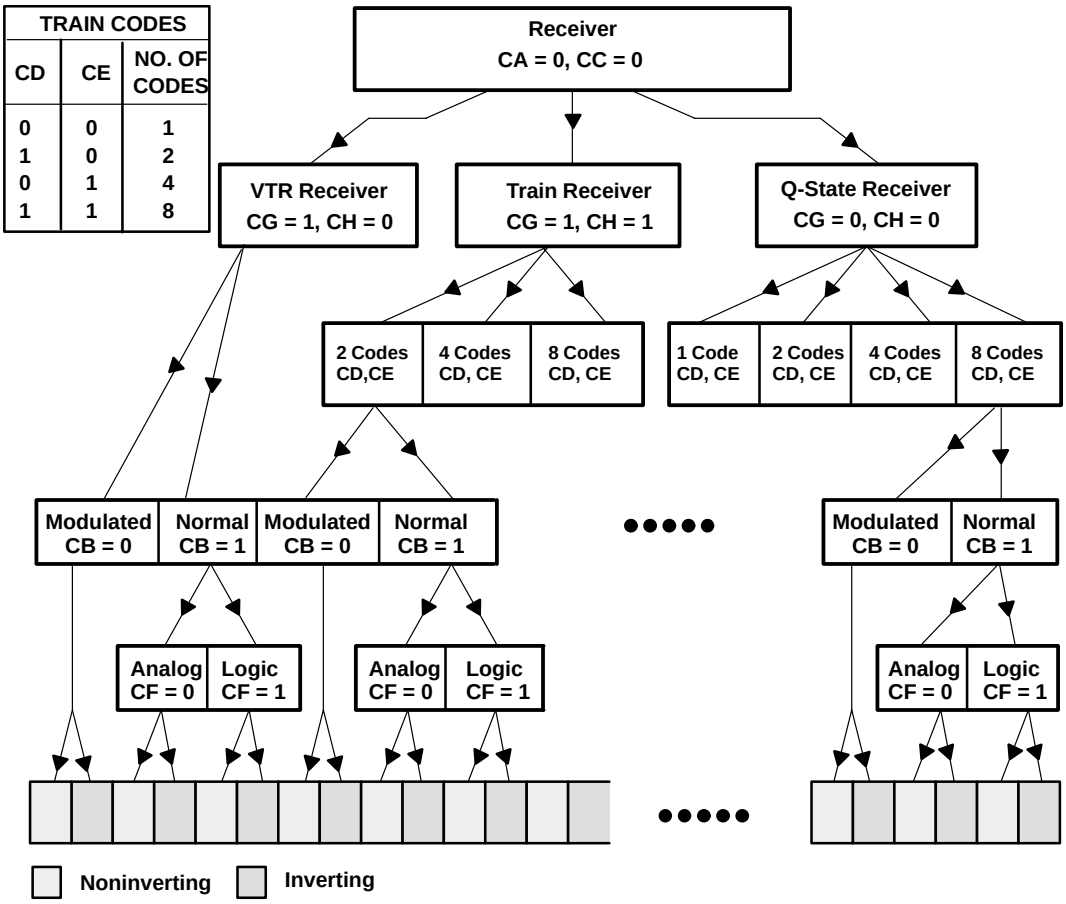


Figure 5–7. Receiver Configurations

5.12.1 Normal Mode (CB = 1)

The normal receiver function corresponds to a normal transmitter.

5.12.2 Modulated Mode (CB = 0)

The modulated receiver functions in a way that corresponds to a modulated transmitter. The oscillator frequency of the receiver must be 480 kHz. The signal used as an input must be demodulated to the carrier frequency of 40 kHz and then sent to IN.

5.12.3 Analog Mode (CF = 0)

In this configuration, the received code is sent directly to IN where it is amplified and passed through a comparator to filter and square the received code waveform to logic levels. The phase of the output signal of the internal amplifier section is reversed with respect to the input. The capacitor connected between CEX and GND and the internal resistor of 178 Ω determines the cutoff frequency of the amplifier, which is in a high-pass configuration.

5.12.4 Logic Mode (CF = 1)

In this configuration, the received code is at logic level. The analog amplifier and comparator connected internally to IN is bypassed. This is typically the configuration used when the transmitter and receiver are connected together by a hard line.

5.12.5 Noninverting Mode (CI = 0) or Inverting Mode (CI = 1)

The code input to IN is not inverted before passing to the logic circuitry. The following considerations must be taken to determine if a noninverting or inverting receiver should be used:

- Transmitting from OUT on the transmitter is considered inverted.
- Transmitting from IN on the transmitter is considered noninverted.
- Using the logic mode on the receiver (CF = 1) does not invert the signal.
- Using the analog mode on the receiver (CF = 0) does invert the signal.
- Determine whether the signal path between the transmitter and receiver inverts the signal.

The code input to IN is internally inverted before passing to the logic circuitry.

NOTE:

Do not use the TMS3637 in the log inverting modes CA = 0, CC = 0, CF = 0, or CI = 1. The amplifier sensitivity is degraded in these modes.

6 Application Information

6.1 General Applications

In this section an example schematic is shown for each of the four transmission media categories for which the device can be configured. These schematics help to define the capabilities of the TMS3637. When configured for infrared, one transmitter works for both normal and modulated modes. In addition, a recommended programming station is shown. The schematics are:

- Direct-wired connection of transmitter/receiver
  - Two wires
  - Four wires
- Infrared coupling of transmitter/receiver
  - Normal transmission mode
  - Modulated transmission mode
- Radio frequency (RF) coupling of transmitter/receiver
- RF receiver and decoder
- Programming station used to program the TMS3637
  -

6.2 Direct-Wire Connection of Transmitter and Receiver

The transmitter and receiver can be connected together by a direct two-wire or four-wire line. Both configurations are described in the following paragraphs.

6.2.1 Two-Wire Direct Connection

Table 6–1 list the parts for the schematic of a two-wire direct connection of the transmitter and receiver shown in Figure 6–1. Only two wires are required, primarily because the transmitted code is superimposed on the source voltage delivered to the transmitter, and the transmitter uses its own internal oscillator. The transmitter is configured as a normal continuous transmitter and the content of the configuration EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
1	1	1	0	0	0	0	0	0

The device uses its internal oscillator to clock the data out (transmitter) and clock data in (receiver). The oscillating frequency of the transmitter is approximately 5.7 kHz. With V_{CC} = 5 V, the transmitted code on OUT (point A) is a square waveform between 0 V (internal connection to GND) and 5 V. At point B, the maximum value is 5 V (when OUT is open) and the minimum value is $4.8 \times 10K/(10K+220) = 4.892$ V (when OUT is at 0 V). The voltage swing is then 5 V − 4.892 V = 108 mV. The voltage swing must not be much greater than 100 mV because this is superimposed on the source voltage used to power the device. At point C, the maximum value is $V_{CC}/2 = 2.5$ V and the minimum value is 2.5 V − 0.108 V = 2.4 V due to the coupling through capacitor C2. At point D, R6 and C4 act as a low-pass filter (with a cutoff frequency of approximately 11 kHz) so that the code passes but higher frequency noise is suppressed. The receiver is configured as an analog normal 1-code Q-state noninverting receiver and the content of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
0	1	0	0	0	0	0	0	0

The receiver is used in the noninverting mode. Using OUT on the transmitter to transmit the code inverts it, but the internal analog amplifier in the receiver (CF = 0) reinverts the signal. The signal path between the transmitter and receiver does not invert the signal. The result is a signal that is noninverted at the internal logic controller of the receiver, hence use CI = 0 for a noninverting receiver.

As required, the oscillating frequency of the receiver is about ten times greater than that of the 57 kHz transmitter. This is easily set by keeping R_{osc} constant but reducing C_{osc} to one-tenth of its original value. The signal on IN is internally amplified and the gain is calculated using equation 1:

$$G = \sqrt{\left(\frac{1 + 39 \times 32.5E6 \times 103E\text{-}18 \times 1.27E9}{1 + 39 \times 32.5E6 \times 103E\text{-}18 \times 31.7E3}\right)} = 13 \quad (1)$$

The input to the internal comparator has a voltage swing of approximately 1.4 V peak-to-peak (13 × 108 mV). OUT on the receiver maintains the same status for approximately 0.5 s (1M × 470 nF).

Table 6–1. Two-Wire Direct Connection

DEVICE	FUNCTION
U1	TMS3637 configured as a normal continuous logic transmitter
U2	TMS3637 configured as a analog normal Q-state noninverting receiver
R1	Pullup resistor on OUT, an open drain
R2	Resistor on OSCR that, in conjunction with C1, determines the internal oscillator frequency of U1.
R3	Resistor that provides current limiting and isolation between V_{CC} and transmitter OUT swing.
R4	Upper portion of voltage divider used to bias receiver output
R5	Lower portion of voltage divider used to bias receiver output
R6	Resistor that is part of RC low-pass network on front end of U2 receiver
R7	Resistor on TIME that, along with C5, determines OUT pulse duration on U2.
R8	Resistor on OSCR that, in conjunction with C7, determines internal oscillator frequency on U2.
R9	Current-limiting resistor for LED indicator
C1	Capacitor on OSCC that, in conjunction with R2, determines internal oscillator frequency of U1.
C2	AC-coupling capacitor for output logic pulses from U1
C3	Power-supply bypass capacitor
C4	Capacitor that is part of RC low-pass network used on front-end of U2 receiver.
C5	Capacitor on TIME that, in conjunction with R7, determines OUT pulse duration on U2.
C6	Capacitor that sets gain of internal receive amplifier in U2.
C7	Capacitor on OSCC that, in conjunction with R8, determines internal oscillator frequency of U2.
D1	LED for indication of Q-state output toggling on and off

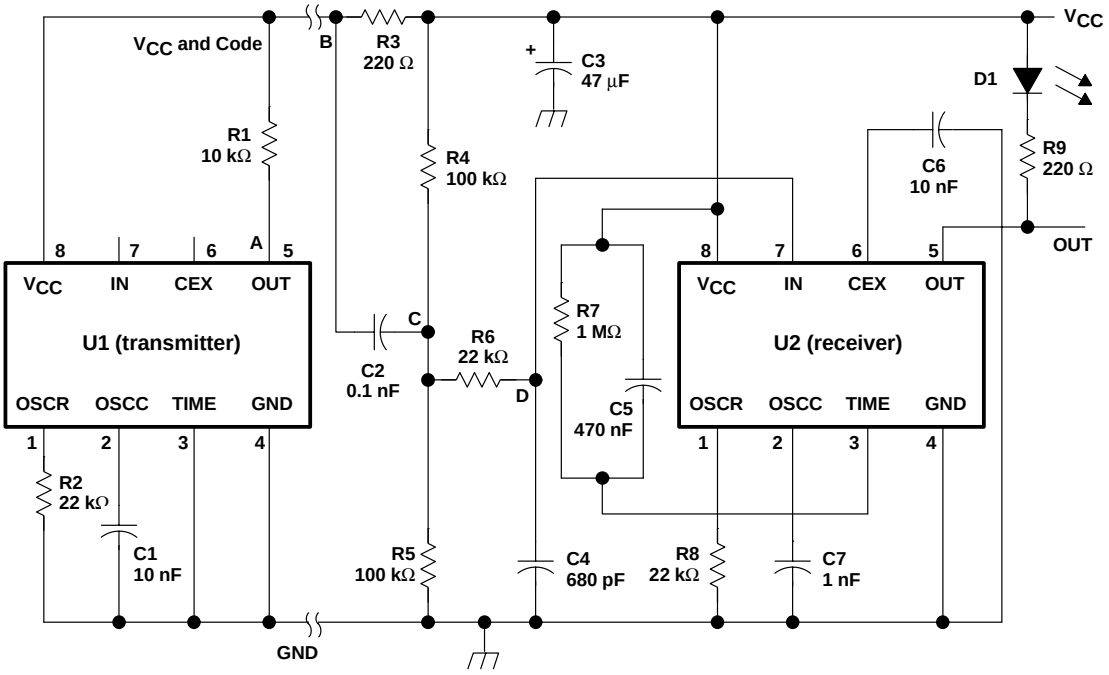


Figure 6–1. Two-Wire Direct Connection

6.2.2 Four-Wire Direct Connection

Table 6–2 lists the parts for the schematic of a four-wire direct connection of the transmitter/receiver shown in Figure 6–2. In this example, the V_{CC}, code, clock, and GND are provided through four separate wires.

The transmitter is configured as a normal continuous transmitter and the content of the configuration EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
1	1	1	0	0	0	0	0	0

The transmitter uses its external oscillator to clock the data out. This external oscillator is a simple inverting (NOT) gate that has a positive feedback loop through a resistor. The frequency of the oscillator is approximately 26 kHz.

The receiver is configured as a logic normal (1-code) Q-state inverting receiver, and the content of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
0	1	0	0	0	1	0	0	1

The receiver is used in the inverting mode. The code is considered to be inverted when using OUT on the transmitter to transmit the code. The signal path between the transmitter and receiver does not invert the signal; using the logic mode (CF = 1) also does not invert the signal. The result is a signal that is inverted at the internal logic controller of the receiver; then use CI = 1, and an inverting receiver is used. (When IN transmits the code, the signal is not inverted; then use CI = 0. An external pullup is not required when IN is used in this manner).

As required, the oscillating frequency is approximately 260 kHz, which is a frequency approximately ten times greater than that of the transmitter. This is provided by the internal oscillator in the receiver. OUT on the receiver maintains the same status for approximately 0.5 seconds (1M × 470 nF). A typical application is an electronic key as shown in Figure 6–3.

Table 6–2. Four-Wire Direct Connection

DEVICE	FUNCTION
U1	TMS3637 configured as a normal continuous logic transmitter
U2	TMS3637 configured as an analog normal (1-code) Q-state noninverting receiver
U3	Inverter (NOT gate) used as external clock
R1	Feedback resistor for U3
R2	Resistor on TIME that, in conjunction with C2, determines OUT pulse duration on U2.
R3	Resistor on OSCR that, in conjunction with C3, determines internal oscillator frequency of U2.
R4	Pullup resistor for transmitter OUT, which is an open-drain output
R5	Current-limiting resistor for D1
C1	Part of feedback circuit used to cause U3 to oscillate
C2	Capacitor on TIME that, in conjunction with R2, determines OUT pulse duration on U2.
C3	Capacitor on OSCC that, in conjunction with R3, determines internal oscillator frequency of U2.
D1	LED for indication of received code

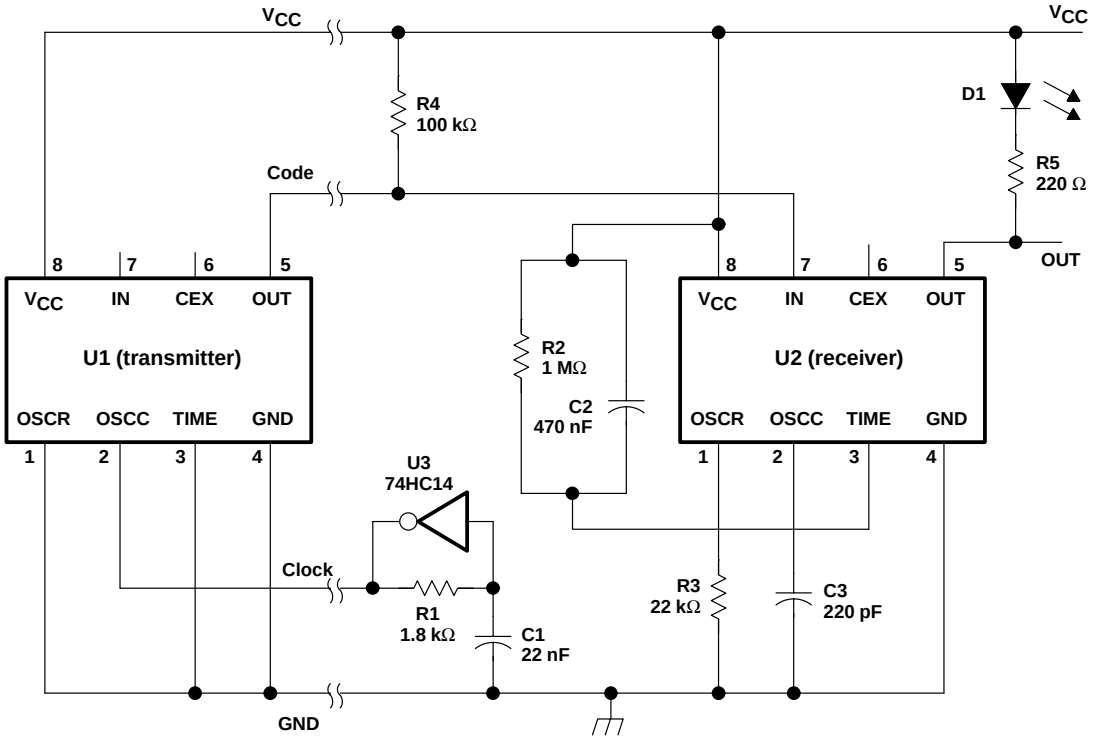


Figure 6–2. Four-Wire Direct Connection

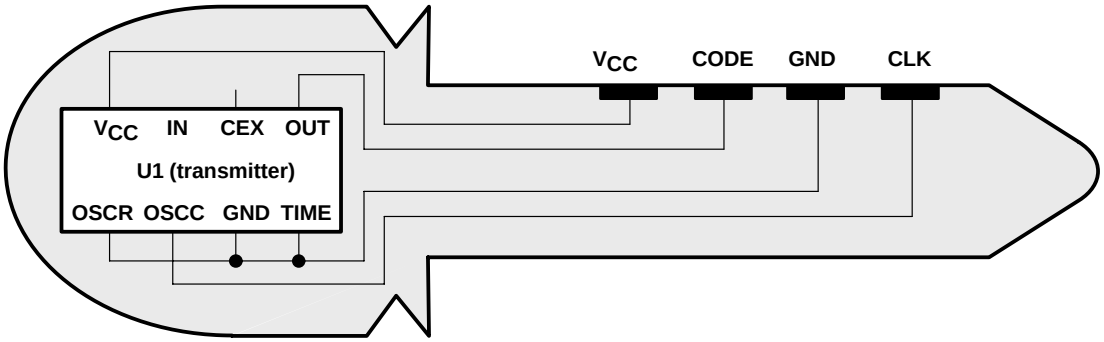


Figure 6–3. Four-Wire Direct Connection Key

6.3 Infrared Coupling of Transmitter/Receiver — Normal Transmission Mode

Table 6-3 lists the parts for the schematic of an infrared transmitter working in the normal transmission configuration as shown in Figure 6–4. Table 6–4 lists the parts for the infrared receiver shown in Figure 6–5.

The transmitter is configured as a normal continuous transmitter, and the content of the configuration EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
1	1	1	0	0	0	0	0	0

The transmitter uses its internal oscillator to clock the data out. The frequency of the oscillator is approximately 26 kHz.

The receiver is configured as a logic normal (1-code) Q-state inverting receiver and the content of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
0	1	0	0	0	1	0	0	1

The receiver is used in the inverting mode. The code is considered to be inverted when using OUT on the transmitter to transmit the code. The signal path between the transmitter and receiver does not invert the signal. Using the logic mode (CF = 1) also does not invert the signal. The result is a signal that is inverted at the internal logic controller of the receiver, then use CI = 1 for an inverting receiver.

As required, the oscillating frequency of the receiver is 260 kHz, which is approximately ten times greater than that of the transmitter. This is provided by the internal oscillator in the receiver. OUT on the receiver maintains the same status for approximately 0.5 seconds (1M $\times$ 470 nF).

Table 6–3. Infrared Transmitter Component Functions (Normal Transmission Mode)

DEVICE	FUNCTION
U1	TMS3637 configured as a normal continuous transmitter
R1	Resistor on OSCR that, in conjunction with C1, determines the internal oscillator frequency of U1.
R2	Current-limiting resistor for LED
R3	Current-limiting base-drive resistor for Q1
R4	Pullup resistor for OUT on U1 and bias for Q1
R5	Current-limiting collector resistor for Q1
R6	Pullup resistor for TIME
C1	Capacitor on OSCC that, in conjunction with R1, determines the internal oscillator frequency of U1.
C2	Power-supply bypass capacitor
D1	LED for visual indication of transmitted code
D2	Infrared LED used to transmit code
Q1	The pnp transistor that drives infrared LEDs
S1	S1 is closed for transmission.

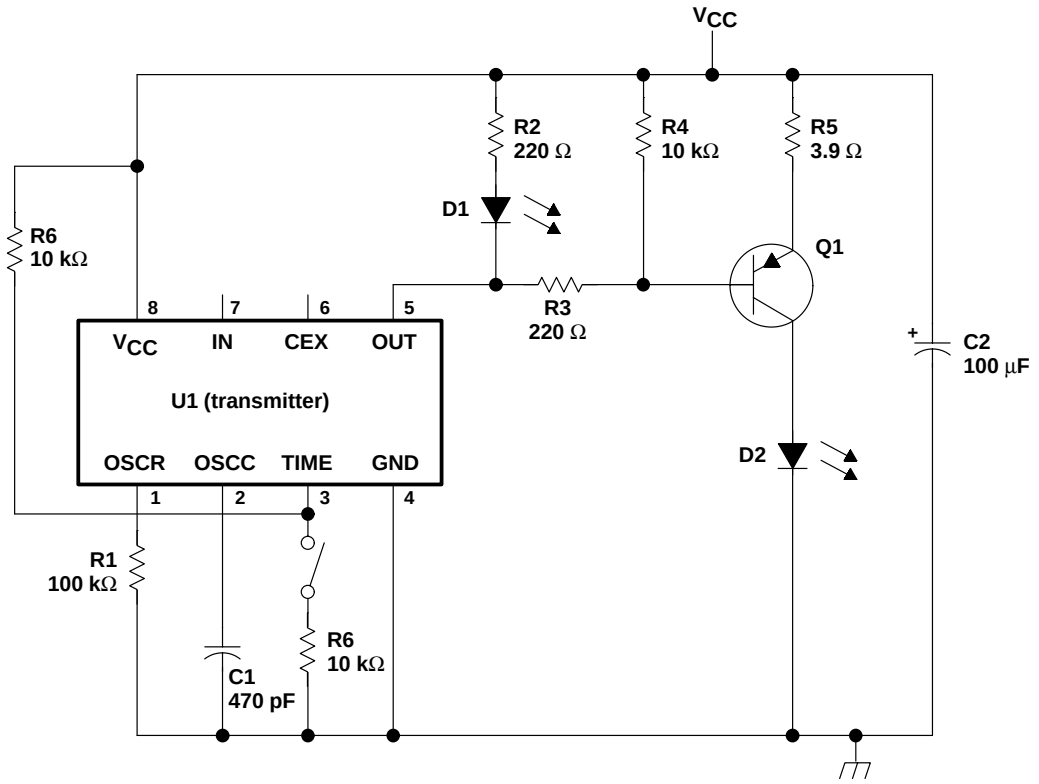


Figure 6–4. Infrared Transmitter

Table 6–4. Infrared Receiver Component Functions (Normal Transmission Mode)

DEVICE	FUNCTION
U1	TMS3637 configured as a logic normal (1-code) Q-state inverting receiver
R1	Current-limiting resistor for IR transistor Q1
R2	Base-bias resistor for Q1
R3	Collector current-limiting resistor for Q2
R4	Collector current-limiting resistor for Q3
R5	Emitter current-limiter for Q3
R6	Resistor on TIME that, in conjunction with C3, determines OUT pulse duration on U1.
R7	Resistor on OSCR that, in conjunction with C4, determines internal oscillator frequency of U1.
R8	Current-limiting resistor for LED indicator
C1	AC-coupling capacitor that passes fluctuating voltage from phototransistor Q1
C2	Power-supply bypass capacitor
C3	Capacitor on TIME that, in conjunction with R6, determines OUT pulse duration on U1.
C4	Capacitor on OSCC that, in conjunction with R7, determines the internal oscillator frequency of U1.
C5	Capacitor that determines the gain of the internal analog receive amplifier on U1.
D1	LED indicator that toggles on/off when valid code is received

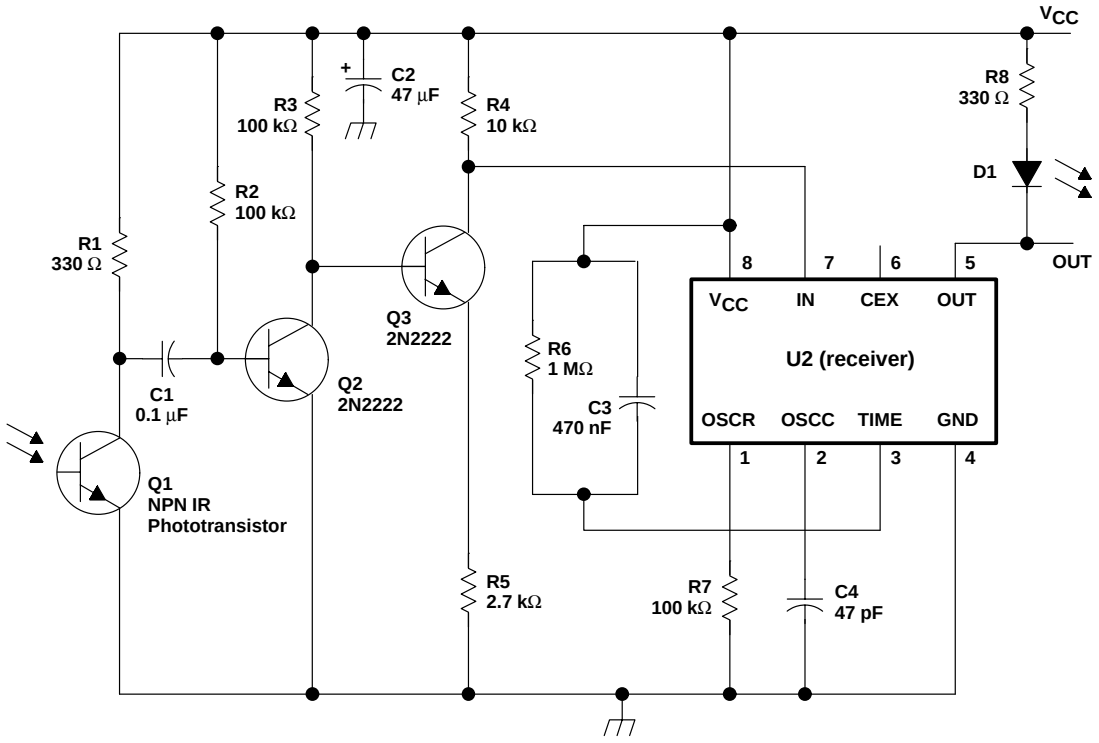


Figure 6–5. Infrared Receiver

6.4 Infrared Coupling of Transmitter/Receiver— Modulated Transmission Mode

Table 6–5 lists the parts for the schematic of an infrared receiver working in the modulated continuous configuration shown in Figure 6–6. This modulated receiver can be used with a normal infrared transmitter (see Figure 6–4) provided that the following guide lines are observed.

The transmitter is configured as a modulated transmitter, and the content of the configuration EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
1	0	1	0	0	0	0	0	0

The oscillating frequency of the transmitter must always be 120 kHz. This is accomplished by using a correct combination of R_{osc} and C_{osc}.

The receiver is cascaded with a TDA3048 (or equivalent) to process the received signal and demodulate it. The receiver is configured as a modulated (1-code) Q-state inverting receiver, and the content of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
0	0	0	0	0	0	0	0	1

The receiver is used in the inverting mode. The code is considered to be inverted when using OUT on the transmitter to transmit the code. The signal path between the transmitter and receiver does not invert the signal; using the modulated mode (CB = 0) also does not invert the signal. The result is a signal that is inverted at the internal logic controller of the receiver; then CI = 1 for an inverting receiver. The oscillating frequency of the receiver is approximately 900 kHz. OUT on the receiver maintains the same status for approximately 0.5 seconds (1M $\times$ 470 nF).

Table 6–5. Infrared Receiver Component Functions (Modulated Transmission Mode)

DEVICE	FUNCTION
U1	Demodulator TDA3048 (or equivalent)
U2	TMS3637 configured as a normal logic (1-code) Q-state inverting receiver
R1	Current-limiting resistor for U1
R2	Resistor on TIME that, in conjunction with C2, determines OUT pulse duration on U2.
R3	Resistor on OSCR that, in conjunction with C3, determines the internal oscillator frequency of U2.
R4	Power-supply current-limiting resistor
C1	Power-supply filter capacitor
C2	Capacitor on TIME that, in conjunction with R2, determines OUT pulse duration on U2.
C3	Capacitor on OSCC that, in conjunction with R3, determines the internal oscillator frequency of U2.
Q1	Infrared phototransistor for received code
D2	Diode that is used to prevent back-EMF in L2 from sourcing current to OUT.
L2	Coil of relay R1
RY1	Relay, 12 V, SPDT

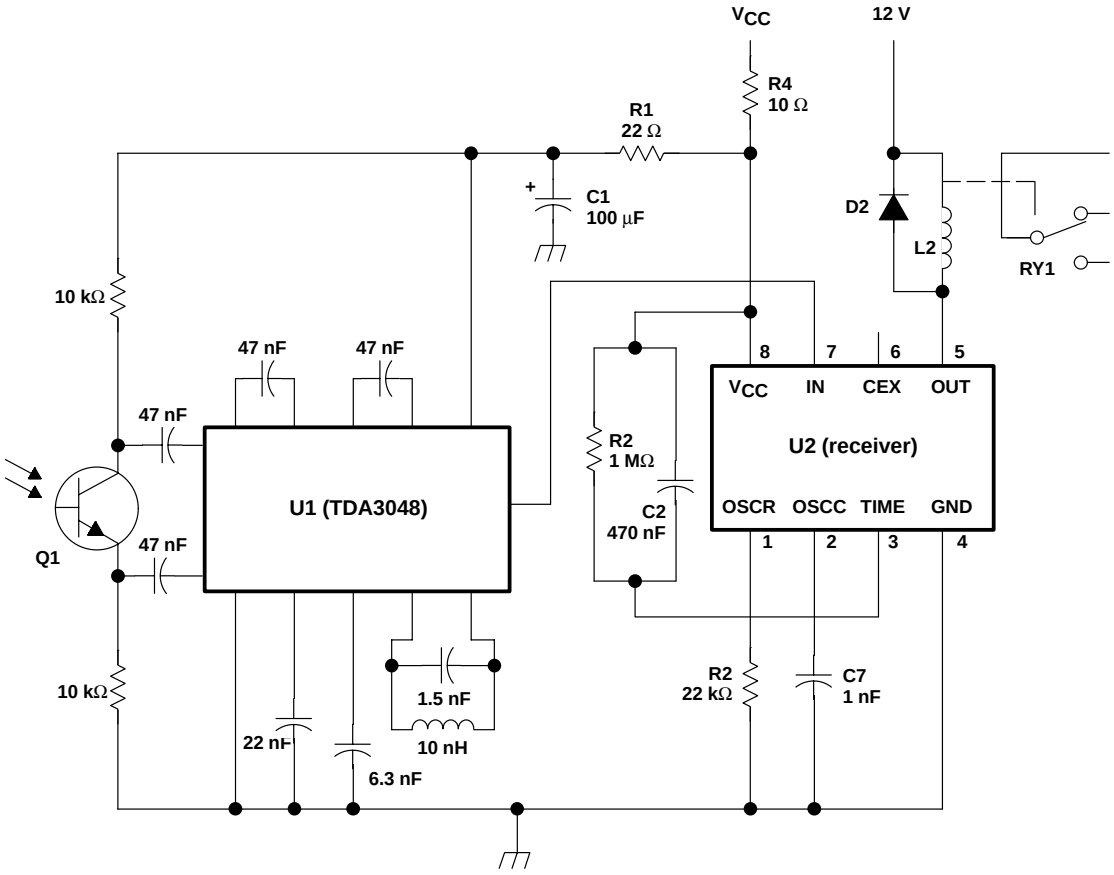


Figure 6–6. Infrared Modulated Receiver

6.5 Radio Frequency (RF) Coupling of Transmitter and Receiver

Table 6–6 lists the parts for the schematic of a radio frequency transmitter and receiver shown in Figure 6–7. In Figure 6–7, the transmitter is configured as a normal continuous transmitter and the content of the configuration of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
1	1	1	0	0	0	0	0	0

The oscillating frequency of the transmitter is about 5.7 kHz, and the transmitter code is pulse modulated.

Table 6–6. RF Transmitter Component Functions

DEVICE	FUNCTION
U1	TMC3637 configured as a transmitter
R1	Resistor on OSCR that, in conjunction with C1, determines the internal oscillator frequency of U1.
R2	Base drive current-Limiting resistor for Q1
C1	Capacitor on OSCC that, in conjunction with R1, determines the internal oscillator frequency of U1.
C2	Capacitive part of LC tank circuit variable for frequency adjustment (2 pF – 10 pF)
C3	Power-supply bypass capacitor (to present low impedance to RF on $V_{CC)}$
L1	Inductive part of LC tank circuit-strip-line type
L2	RF choke presents high impedance to RF between the tank and V_{CC}.
Q1	The npn RF transistor turns on the LC circuit.

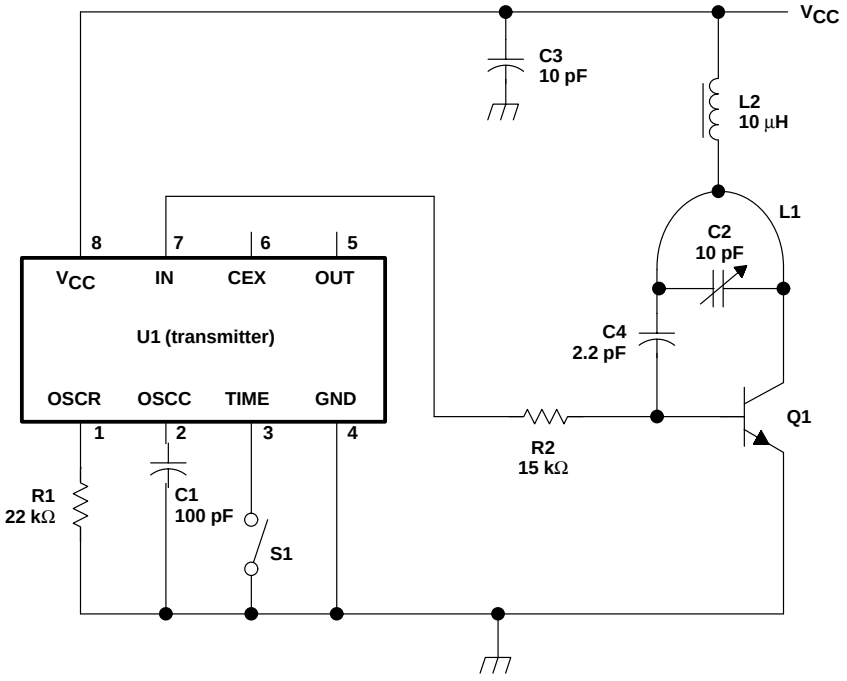


Figure 6–7. Radio Frequency Transmitter

Inductance L2 is an RF choke, while L1 is a strip-line 0.1-μH inductance that is 1.5-mm wide and 3.5-cm long. The frequency range of the transmitter (tunable by C2–10 pF) is approximately 165 MHz – 370 MHz. A good RF transistor with an H_{FE} exceeding 500 MHz is recommended. No external antenna is required, provided the recommended antenna is used on the receiver as described in the following paragraphs.

IN is used for the data out. IN provides the complement of the data out in the transmitter configuration.

In Figure 6–8, the receiver is configured as an analog normal noninverting VTR receiver, and the content of the EEPROM cells is:

CA	CB	CC	CD	CE	CF	CG	CH	CI
0	1	0	0	0	0	1	0	0

The receiver is used in the noninverting mode. Using IN on the transmitter to transmit the code is considered noninverted, but the internal analog amplifier in the receiver (CF = 0) inverts the signal. The signal path between the transmitter and receiver also inverts the signal. The result is a signal that is noninverted at the internal logic controller of the receiver, then C1 = 0, a noninverting receiver.

The receiver can be tuned from approximately 200 MHz – 430 MHz using the trim capacitor C4. The antenna used is a metal wire that is 12 inches long. Inductances L1 and L2 are in the range of 0.2 μH – 2 μH.

The oscillating frequency of the receiver is 57 kHz, which is approximately ten times that of the transmitter, and the gain of the internal analog amplifier is approximately 200. OUT on the receiver maintains the same status for approximately 0.5 second (1M $\times$ 470 nF).

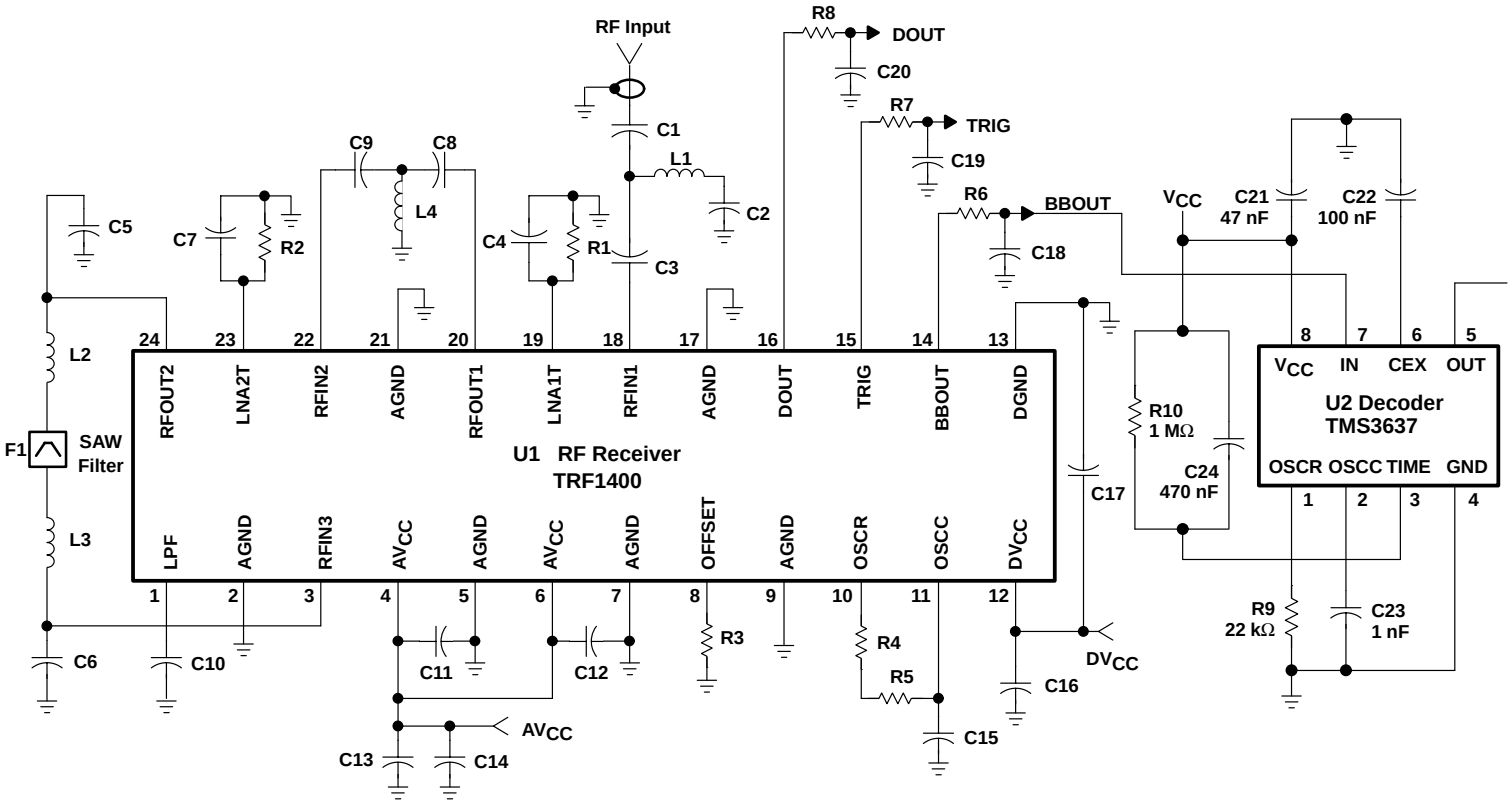


Figure 6–8. TRF1400 RF Receiver and TMS3637 Decoder Circuit

6.6 RF Receiver and Decoder

Table 6–7 lists the parts for the schematic shown in Figure 6–8. Figure 6–8 shows a Texas Instruments TRF1400 RF receiver and a Texas Instruments TMS3637 receiver connected as an RF receiver and decoder combination. Table 6–7 lists the components that comprise this circuit. As with any RF design, the successful integration of these two devices relies heavily on the board layout and the quality of the external components. This circuit demonstrates performance of the TRF1400 and TMS3637 at 300 MHz. Specified component tolerances and, where applicable, Q should be observed during the selection of parts.

A complete set of Gerber photoplotter files for the TRF1400 circuit board can be obtained from any TI™ Field Sales Office.

Table 6–7. TRF1400 RF Receiver and TCM3637 Decoder Parts List (for 300 MHz operation)

DESIGNATORS	DESCRIPTION	VALUE	MANUFACTURER	MANUFACTURER P/N
C1	Capacitor	4 pF	Murata	GRM40C0G040C050V
C2	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C3	Capacitor	22 pF	Murata	GRM40C0G220J050BD
C4	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C5	Capacitor	5 pF	Murata	GRM40C0G050D050BD
C6	Capacitor	1.5 pF	Murata	GRM40C0G1R5C050BD
C7	Capacitor	100 pF	Murata	GRM40C0G101J050BD
C8	Capacitor	3 pF	Murata	GRM40C0G030C050BD
C9	Capacitor	18 pF	Murata	GRM40C0G180J050BD
C10	Capacitor	0.047 μF	Murata	GRM40X7R473K050
C11	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C12	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C13	Capacitor	0.022 μF	Murata	GRM40X7R223K050BL
C14	Capacitor, Tantalum†	4.7 μF	Sprague	293D475X9050D2T
C15	Capacitor	220 pF, 5%	Murata	GRM40C0G221J050BD
C16	Capacitor, Tantalum†	4.7 μF	Sprague	293D475X9050D2T
C17	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C18	Capacitor	0.022 μF	Murata	GRM40X7R223K050BL
C19	Capacitor	2200 pF	Murata	GRM40X7R222K050BD
C20	Capacitor	0.022 μF	Murata	GRM40X7R223K050BL
C21	Capacitor	47 μF		
C22	Capacitor	100 μF		
C23	Capacitor	1 nF		
C24	Capacitor	470 nF		
E1§	2-Pin Connector		3M	2340–6111–TN
E2§	2-Pin Connector		3M	2340–6111–TN
E3§	6-Pin Connector		3M	2340–6111–TN
S1–S2	Header shunts		3M	929952–10
F1	SAW filter‡	RF1211	RFM	RF1211

† Tantalum capacitors are rated at 6.3 Vdc minimum
‡ SAW = surface acoustic wave
§ Not shown on schematic

TI is a trademark of Texas Instruments Incorporated.

Table 6–7. TRF1400 RF Receiver and TCM3637 Decoder Parts List (for 300 MHz operation) (continued)

DESIGNATORS	DESCRIPTION	VALUE	MANUFACTURER	MANUFACTURER P/N
L1	Inductor	47 nH	Coilcraft	0805HS470TMBC
L2	Inductor	82 nH	Coilcraft	0805HS820TKBC
L3	Inductor	120 nH	Coilcraft	0805HS121TKBC
L4	Inductor	39 nH	Coilcraft	0805HS390TMBC
P1	RF SMA Connector		Johnson	142–0701–201
R1	Resistor	1200 Ω		
R2	Resistor	1200 Ω		
R3	Resistor	1M Ω		
R4	Resistor	130 KΩ, 1%		
R5	Resistor	0 Ω		
R6	Resistor	1 KΩ		
R7	Resistor	100 Ω		
R8	Resistor	1 KΩ		
R9	Resistor	27 kΩ		
R10	Resistor	1M Ω		
U1	RF Receiver		Texas Instruments	TRF1400
U2	Decoder		Texas Instruments	TMS3637

6.7 Programming Station

A programming station schematic is shown in Figure 6–9. This station is made up of two major parts: 1)a shift register/clock circuit that outputs exactly 35 bits serially (four reset pulses, 22 security bits, and 9 configuration bits), and 2) a transistor ramp generator that outputs the programming pulse required to store data in the EEPROM. The following paragraphs detail the function of the circuit.

Before the momentary switch SW5 is pressed, the shift registers U9–U13 shift-load input is low so that they are continually loading whatever code is present on the DIP switches SW1–SW4. In addition, the binary counter U6 is in a clear state and its output is 00000000.

When momentary switch SW5 is pressed, the set-reset (S-R) latch on U1 acts as a debouncer and outputs a logic level 1, which releases the clear on binary counter U6. It places a high on the shift input to the shift registers
U9 – U13, allowing them to shift out the stored 35 bits as soon as a clock is applied to them. The output of the S-R latch on U1 is also connected to the D input of the D flip-flop on U2. The D flip-flop is clocked by the free-running 555 timer (U8) configured for astable operation on a 8-kHz clock. Therefore, on the next rising edge of the U8 clock, the D flip-flop on U2 outputs a high signal. The output of the D flip-flop enables the AND gate on U3 to pass the 8-kHz clock. The 8-kHz clock signal is routed to the dual 4-bit binary counters (U6) that have had their CLR terminal released by the S-R latch (from pressing the momentary switch SW5). The outputs of the U6 counters are connected to the counter-comparator U7, which outputs low when the count reaches exactly 35 clock pulses (as defined by the code 11000100 on U7 Q inputs). The output of U7 then clears the D flip-flop on U2, the 8-kHz clock is no longer able to pass, and the counting stops.

During this entire counting sequence, the shift registers U9 through U13 are clocked with exactly 35 bits. Due to the momentary switch being pressed, the S-R latch output is high on the shift-register shift enable, allowing the registers to shift out the 35 bits of data to the code input of the TMS3637. The TMS3637 is clocked synchronously with this data on OSCR.

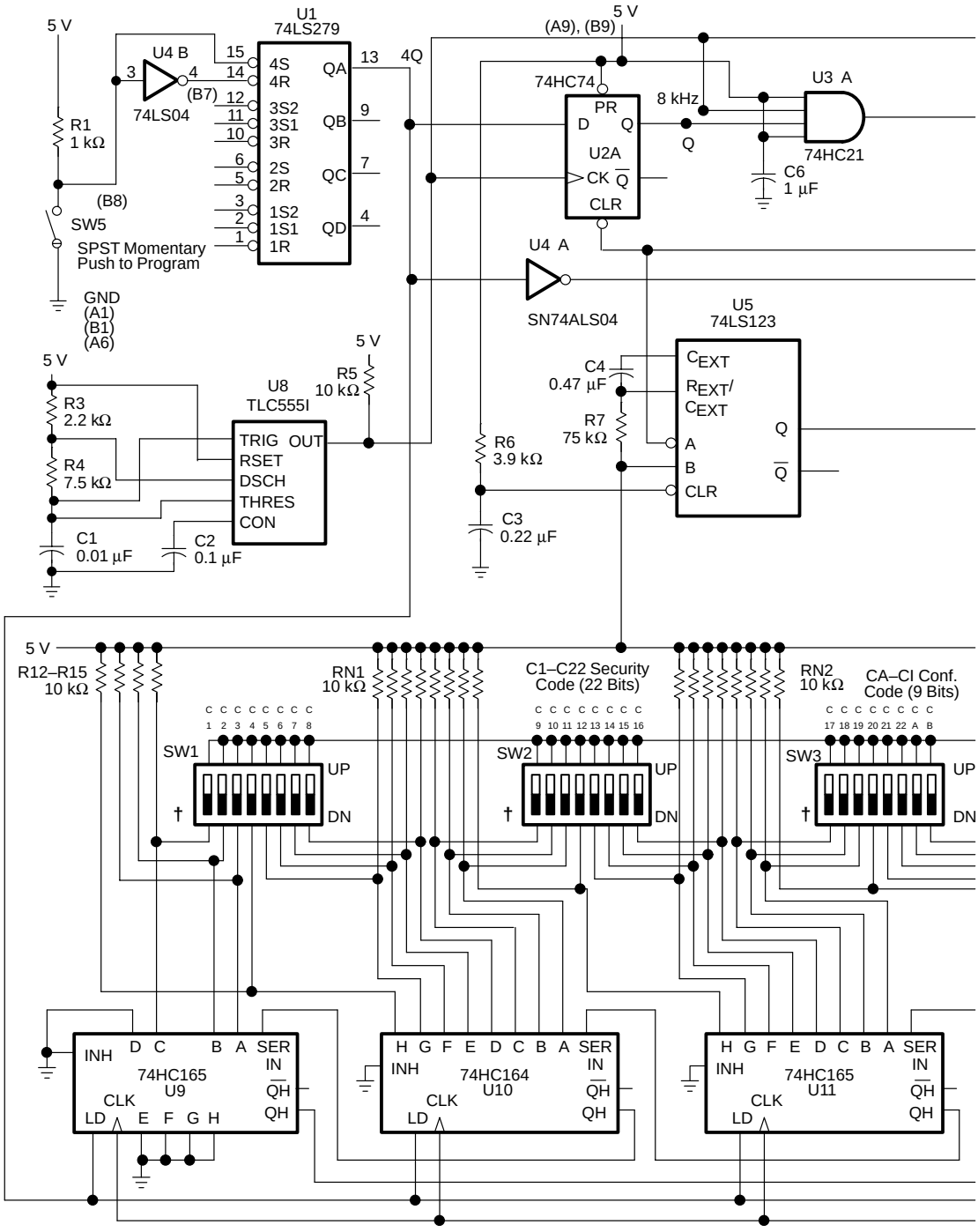
Because the binary counter U6 is released from its cleared state and the U9–U13 registers are allowed to shift data only during the time that the momentary switch is pressed, it is required that the switch be held

closed for the duration of the entire clocking sequence which is 4.4 ms or greater (125 μs × 35 bits = 4.4 ms).

At the conclusion of the count, the one-shot timer U5 is edge triggered by the output of the counter-comparator U7. The output from U5 enables the EEPROM programming-pulse ramp generator that is made up of Q1 and Q2. When U5 goes high (for approximately 13 ms), transistor Q1 turns on. U5 goes high and turns off Q2, and the voltage on OSCC of the TMS3637 is allowed to ramp from 5.5 V to 17 V using the RC time constant established by R10 and C5. The required ramp characteristics to successfully program the EEPROM are defined in this data manual (see Figure 3–4). After the U5 time expires, the voltage on OSCC again returns to 5.5 V (approximately one diode drop above 5 V) and the TMS3637 is programmed.

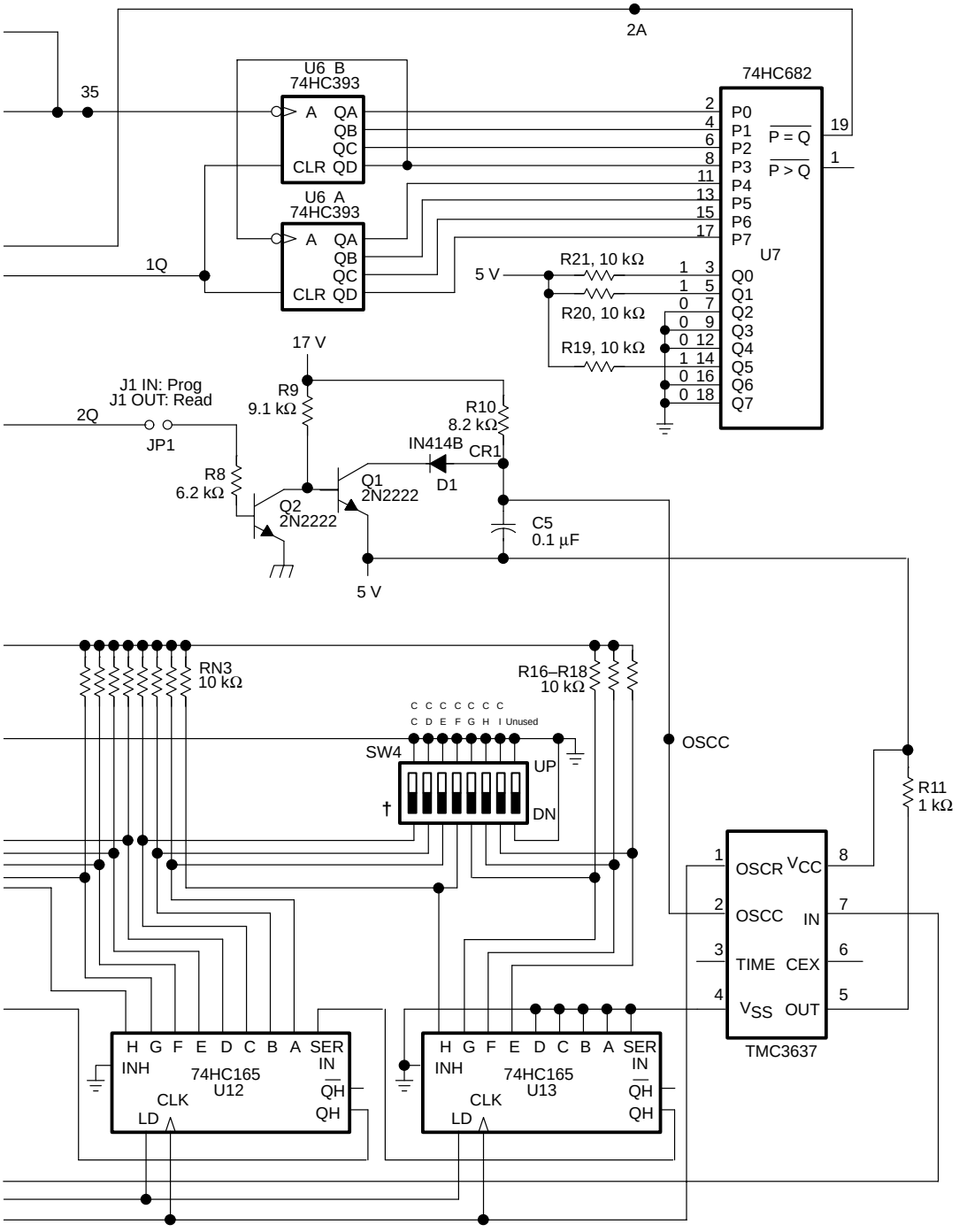
The U5 timer normally outputs one pulse when the circuit is powered up. This is inherent of the timer device. To prevent the timer from outputting this pulse and inadvertently programming the TMS3637, a power-on reset RC combination is included. When power is first applied to the circuit, timer U5 remains in the clear state until capacitor C3 can charge through resistor R6, preventing the generation of a programming pulse.

After the programming button is released, the circuit again returns to its steady-state mode where counter U6 is held in a cleared state and the shift resisters U9–U13 are always loaded with the current code on the DIP switches SW1–SW4.



† Notch in lower left corner of dip switches. Up is open = 1, down is closed = 0. All the chips are bypassed with 0.1-mF (C7 – C20) ceramic capacitors.

Figure 6–9. Programming Station



† Notch in lower left corner of dip switches. Up is open = 1, down is closed = 0. All the chips are bypassed with 0.1-mF (C7 – C20) ceramic capacitors.

Figure 6–9. Programming Station (continued)

6.8 TMS3637 Programming Station Parts Lists

Table 6–8 contains a listing of the parts that compose the TMS3637 programming stations (see Figure 6–9 for a schematic).

Table 6–8. TMS3637 Programming Station Parts List

PART	DESCRIPTION		FUNCTION
R1	Resistor, 1 kΩ,, 1/4 watt		R1 is an isolation resistor
R2	Resistor, 1 kΩ,, 1/4 watt		With C1 and R4, R2 sets U8 discharge time
R4	Resistor, 1 kΩ,, 1/4 watt		With C1, R2 sets U8 threshold level
R5	Resistor, 1 kΩ,, 1/4 watt		R5 is the output pullup resistor for U8
R6	Resistor, 1 kΩ,, 1/4 watt		With C3, R6 sets time constant for U5 CLR terminal
R7	Resistor, 1 kΩ,, 1/4 watt		With C4, R7 sets time constant for U5 CERT terminal
R8	Resistor, 1 kΩ,, 1/4 watt		R8 couples U5 dc output to base of Q2
R9	Resistor, 1 kΩ,, 1/4 watt		R9 is the load resistor for Q2
R10	Resistor, 1 kΩ,, 1/4 watt		With C5, R10 sets programming pulse ramp time
R11	Resistor, 1 kΩ,, 1/4 watt		R11 is the output pullup resistor for U14
R12–R21	Resistor, 1 kΩ,, 1/4 watt		R12–R21 are load resistors for the shift register data input
RN1–RN3	Resistor, 10 kΩ,, 1/4-watt 16-Pin DIP		RN1–RN3 are Load resistors for the shift register data
C1	Ceramic Capacitor, 0.01-µF		With R4, C1 sets U8 threshold level
C2	Ceramic Capacitor, 0.1-µF		C2 sets control voltage level on U8
C3	Electrolytic Capacitor, 0.22-µF		With R6, C3 prevents generation of program pulse during initial power up
C4	Electrolytic Capacitor, 0.47-µF		With R7, C4 sets time constant for U5 CEXT terminal
C5	Ceramic Capacitor, 0.1-µF		C5 couples high voltage programming pulse to OSCC
C6	Electrolytic Capacitor, 1-µF		C6 is +5-V supply filter capacitor
C7–C19	Ceramic Capacitor, 0.01-µF		C7–C15 are bypass capacitors
U1	TI SN74LS279	Quadruple S-R Latches	The U1 latch acts as debouncer during reset
U2	TI SN74HC74	Dual D-Type Positive-Edge-Triggered Flip-Flops with Clear and Preset	U2 enables U3 to pass the 8-kHz clock
U3	TI SN74HC21	Dual 4-Input Positive-AND Gates	U3 is an 8-kHz gate to shift register and to U6
U4	TI SN7404	Hex Inverters	U4 is a buffer and inverter
U5	TI SN74LS123	Retriggerable Monostable Multivibrators	U5 is a one-shot timer; its output enables EEPROM programming pulse from Q1 and Q2
U6	TI SN47HC393	Dual 4-Bit Binary Counters	U6 is a dual binary 4-bit sequential counter
U7	TI SN74HC682	8-Bit Magnitude Counter Comparators	U7 outputs low when the count reaches 35 clock pulses as set by Q inputs
U8	TI TLC555I	Astable/Monostable Timer	U8 is a free-running timer (astable at 8 kHz)
U9–U13	TI SN74HC165	Parallel-Load 8-Bit Shift Registers	U3–U13 shift programming data into the TMS3637

Table 6–8 TMS3637 Programming Station Parts List (continued)

PART	DESCRIPTION		FUNCTION
U14	TMC3637	Remote Control Transmitter/Receiver	U14 transmits or receives specific user-configuration code
Q1, Q2	TI 2N2222	npn Transistor	Q1 and Q2 are emitter followers that output the programming pulse
CR1	1N4148	Silicon Diode	CR1 is a blocking diode when an external oscillator is used
SW1 – SW4		16-Pin DIP switch	SW1 – SW4 select input coding
SW5		SPST Momentary Switch	SW5 when closed resets the device

6.9 TMS3637 Connector Pinout

TI recommends a ZIF socket to be used at location U14 for ease of programming the TMS3637. For TMS3637P (DIP) packages, a 16-pin ZIF can be used (lower portion unused). For TMS3637N surface-mount packages, use a clamshell with a latch cover and DIP footprint. This can be purchased from EmMulation Technology (408-982-0660) part # AS-0808-015-3. The edge connector that is compatible with the TMS3637 PCB is a Sullins part # EZC10DRTH or the equivalent as shown in Table 6–9. Ground terminals A1, A6, and B1 are common, so only one is needed for ground connection.

Table 6–9. Edge-Connector Pinout

EDGE CONNECTOR	FUNCTION
A1	Ground
A2	N/C
A3	N/C
A4	N/C
A5	N/C
A6	Ground
A7	N/C
A8	N/C
A9	5 Vdc
A10	N/C
B1	Ground
B2	17 Vdc
B3	N/C
B4	N/C
B5	N/C
B6	N/C
B7	See Note 1
B8	See Note 1
B9	5 Vdc
B10	N/C (see Note 2)

NOTES: 1. Other edge connections are connected to various parts of circuit. These are for testing purposes only.
2. N/C = Not connected

PACKAGING INFORMATION

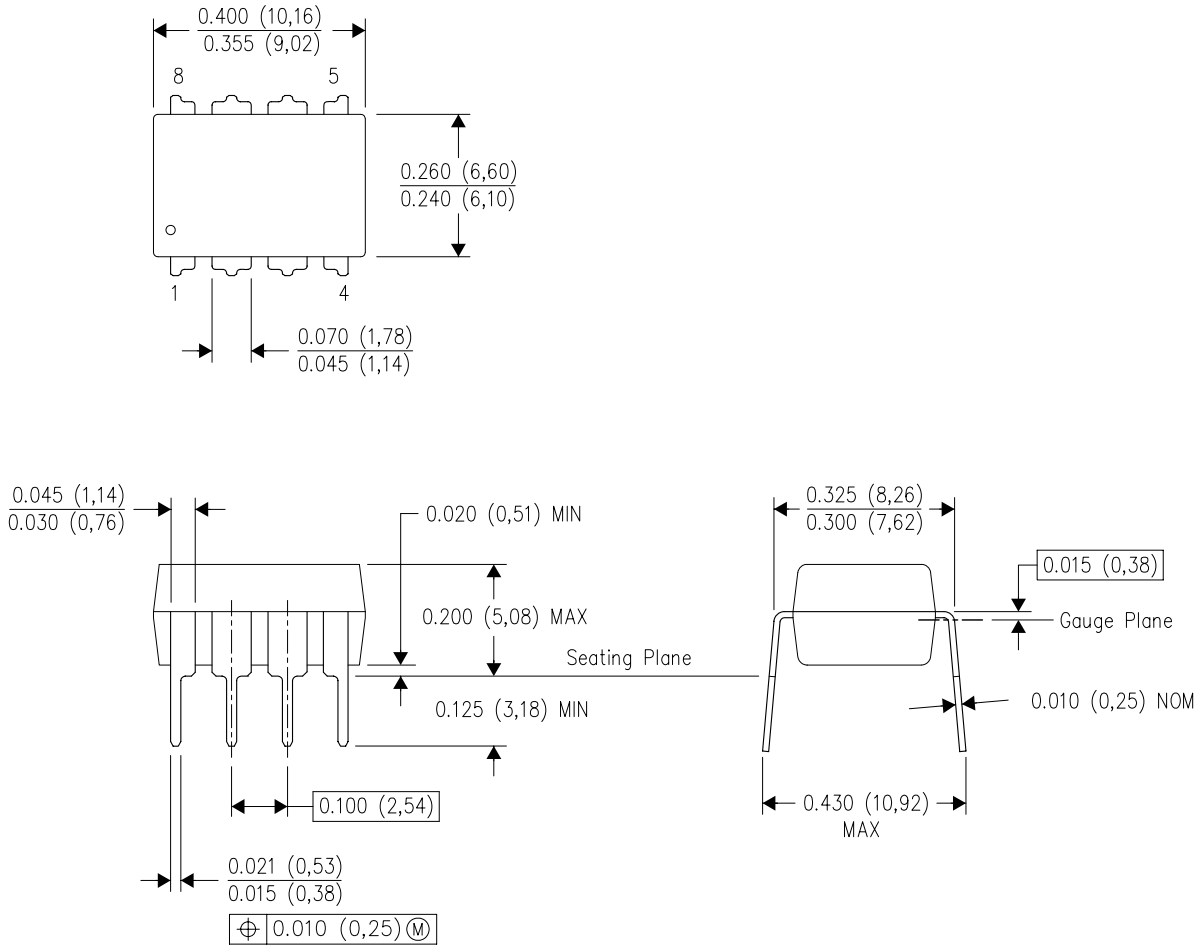
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS3637D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
TMS3637P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

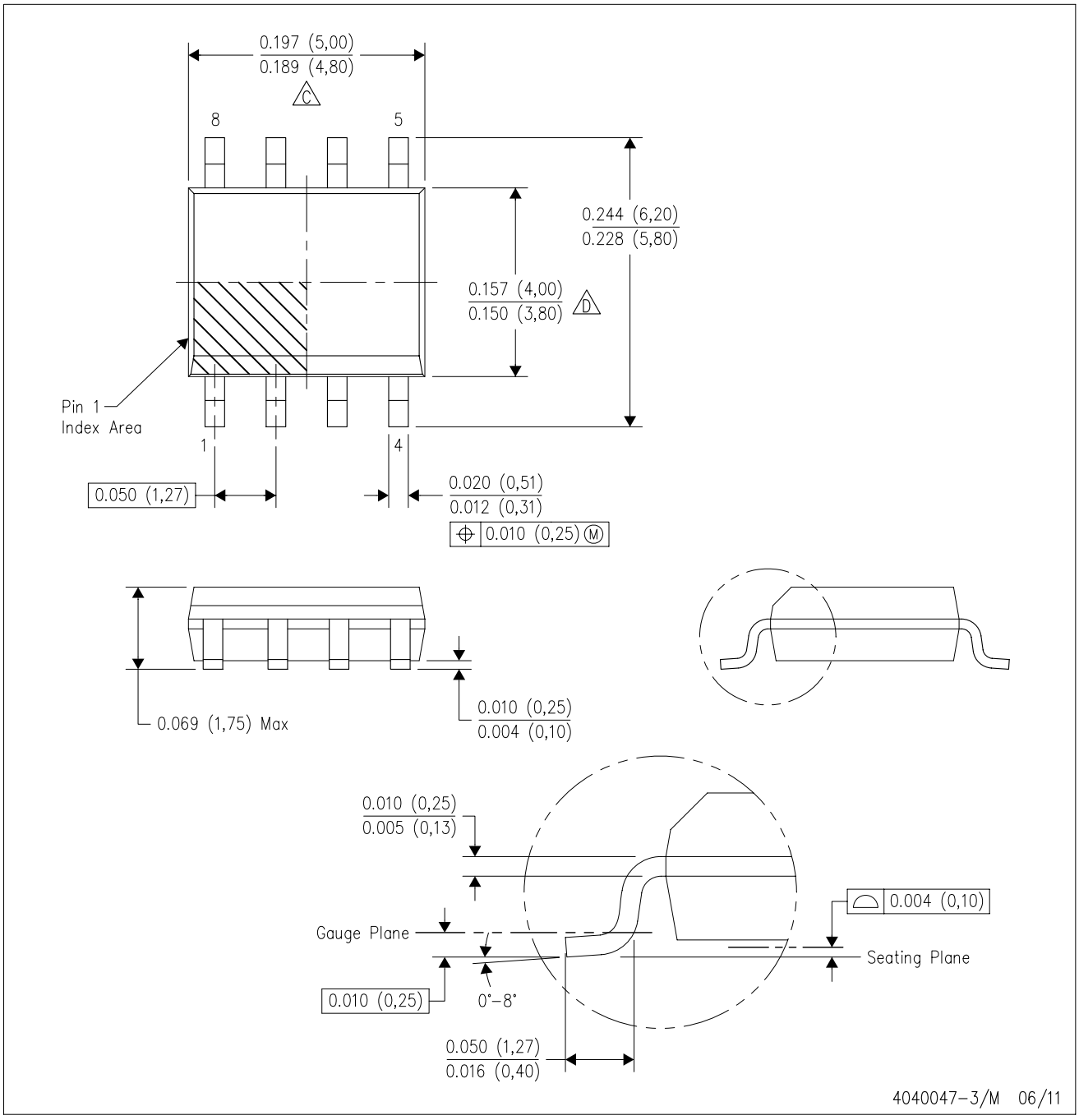
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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