User's Guide

TPS25985 evaluation module for eFuse User's Guide

ABSTRACT

This user's guide describes the evaluation module (EVM) for the TPS25985 eFuse. The TPS25985 device is a 4.5-V to 16-V and 60-A (RMS) stackable eFuse with an accurate and fast current monitoring capability. This device supports the parallel connection of multiple eFuses for higher current designs by actively synchronizing the device states and sharing the loads during start-up and steady state. The TPS25985 eFuse has an integrated FET with ultra-low ON resistance of 0.59-mΩ, adjustable and robust overcurrent and short-circuit protections, precise load current monitoring, fast overvoltage protection (fixed 16.7-V threshold), adjustable output slew rate control for inrush current protection, and built-in overtemperature protection to ensure FET safe operating area (SOA). TPS25985 eFuse also has an adjustable overcurrent transient blanking timer to support load transients, adjustable under-voltage protection, integrated FET health monitoring, and reporting, analog die temperature monitor output, dedicated fault and power good indication pins, and an uncommitted general-purpose fast comparator.

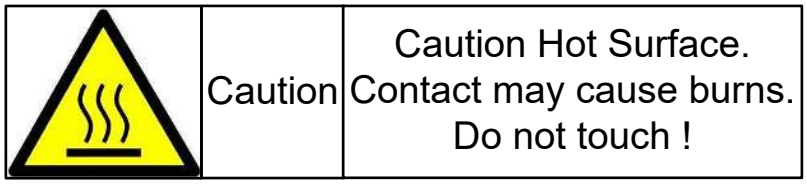

Table of Contents

List of Figures

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List of Tables

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1 Introduction

The *TPS25985EVM eFuse Evaluation Board* allows reference circuit evaluation of Texas Instruments (TI) TPS25985 eFuse. The TPS25985 device is a 4.5-V to 16-V and 60-A (RMS) stackable eFuse with an accurate and fast current monitoring capability. This device supports the parallel connection of multiple eFuses for higher current designs by actively synchronizing the device states and sharing the loads during start-up and steady state. The TPS25985 eFuse has an integrated FET with ultra-low ON resistance of 0.59-mΩ, adjustable and robust overcurrent and short-circuit protections, precise load current monitoring, fast overvoltage protection (fixed 16.7-V threshold), adjustable output slew rate control for inrush current protection, and built-in overtemperature protection to ensure FET safe operating area (SOA). TPS25985 eFuse also has an adjustable overcurrent transient blanking timer to support load transients, adjustable under-voltage protection, integrated FET health monitoring, and reporting, analog die temperature monitor output, dedicated fault and power good indication pins, and an uncommitted general-purpose fast comparator.

1.1 EVM Features

TPS25985EVM comes with two (2) TPS25985 eFuses connected in parallel to evaluate a 12-V (typical) and 120-A (steady state) design. General TPS25985EVM eFuse evaluation board features include:

- 5-V to 16-V (typical) operation
- 28-A to 170-A programmable circuit breaker threshold using onboard jumpers
- Adjustable reference voltage for overcurrent protection and active current sharing blocks
- Adjustable output voltage slew rate control
- Adjustable transient current blanking timer
- Adjustable current limit during start-up and active current sharing threshold using onboard jumpers
- TVS diode for input and Schottky diode for output transient protections
- LED status for power good and fault indications
- Onboard test points and associated circuitry to implement the system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc using the general-purpose comparator built into the TPS25985 eFuse
- Options to engage the enable power cycle and the quick output discharge (QOD)
- Option to apply custom load transients using onboard MOSFETs, gate drive circuit, and load resistors

1.2 EVM Applications

This EVM can be used on the following applications:

- Input hotswap and hotplug
- Server and high performance computing
- Network interface cards
- Graphics and hardware accelerator cards
- Datacenter switches and routers
- Fan trays
- Switches/routers

2 Description

The TPS25985EVM enables the evaluation of TPS259850x and TPS259851x eFuses from TPS25985 family. This EVM has two (2) TPS259850x eFuses connected in parallel. The input power is applied across the connectors T1 and T3, while T2 and T3 provide the output connection for the EVM; refer to the schematic in Figure 3-1 and EVM test setup in Figure 5-1. TVS diodes D1 and D2 provide the input protection from transient overvoltages. Schottky diodes D3 and D4 protect the output by clamping the negative voltage excursion at the OUT pins of TPS25985 eFuses within the maximum absolute rating.

SW1 allows to do the input power cycle and SW2 enables the quick output discharge (QOD). Power Good (PG) and fault (FLTb & FLTb2) indicators are provided by LED DG1, DR1, and DR2 respectively.

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Table 2-1. TPS25985EVM eFuse Evaluation Board Options and Setting

EVM Function	Vin UVLO Threshold	Vin OVLO Threshold	ITIMER	Output Slew Rate (dv/dt)	IMON	ILIM	ILIM2	IREF
Performance evaluation of TPS25985, 4.5-V to 16-V, 60-A eFuse	5 V	16.7 V	Selectable - 1.4-ms and 14-ms	Selectable - 1.2-V/ms, 1.8-V/ms, and 12-V/ms	Selectable - 170-A, 100-A, and 70-A with VREF of 1-V	Selectable - 32-A and 22-A of inrush current limit and 50-A and 35-A of active current sharing threshold with VREF of 1-V	Selectable - 32-A and 22-A of inrush current limit and 50-A and 35-A of active current sharing threshold with VREF of 1-V	Selectable - 1-V and 0.8-V

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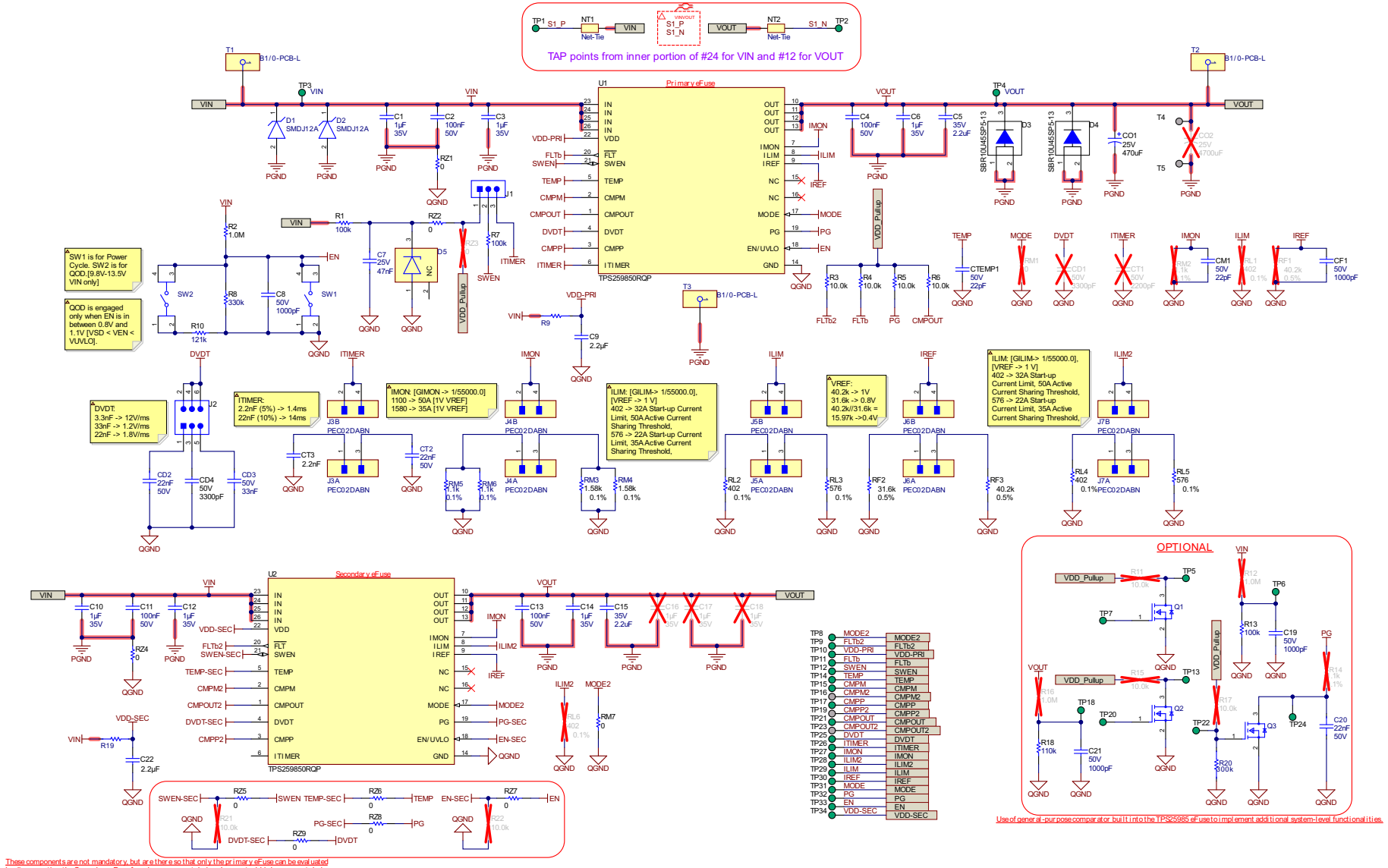
3 Schematic

Figure 3-1 illustrates the EVM schematic.



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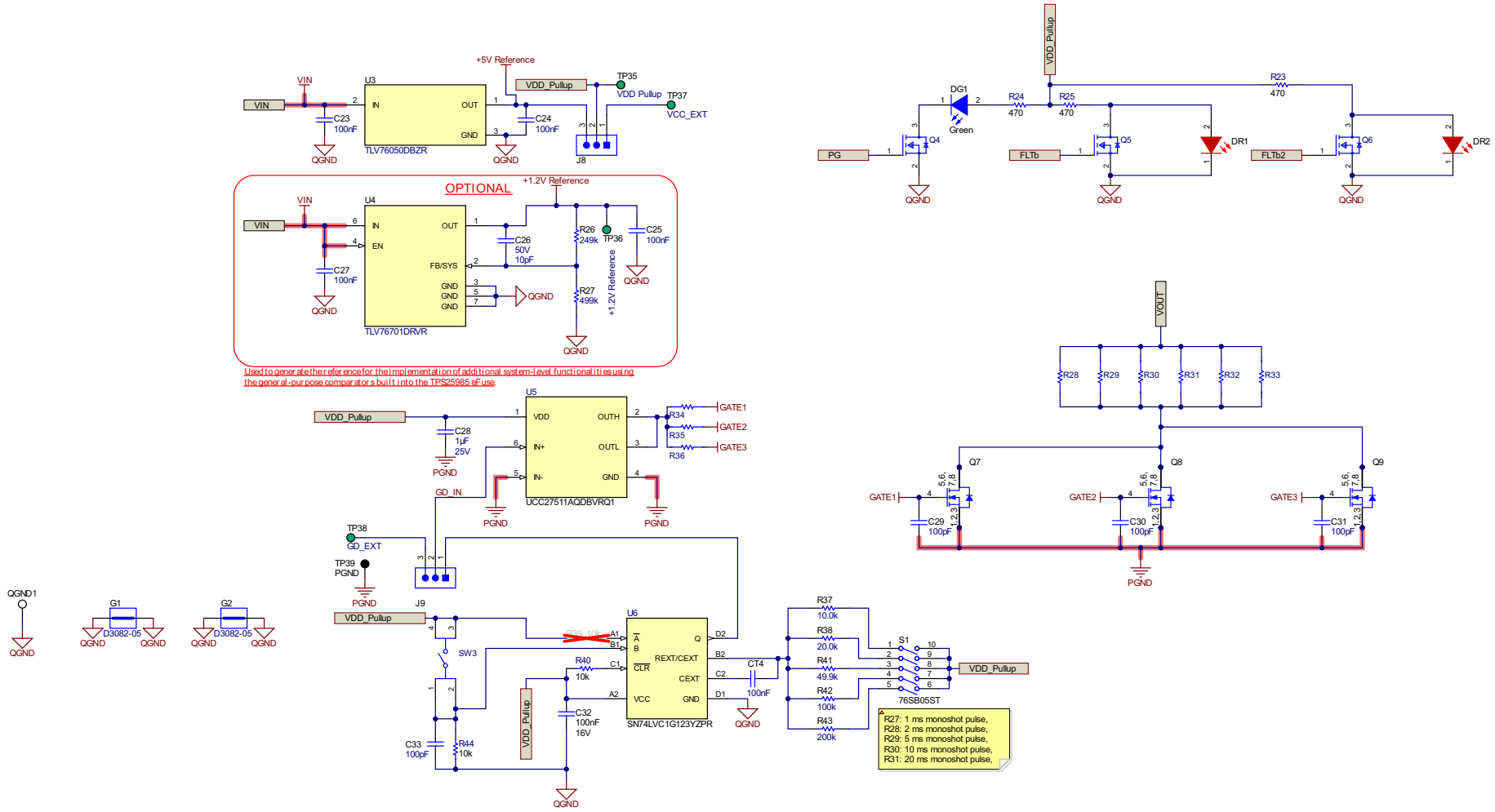

Figure 3-1. TPS25985EVM eFuse Evaluation Board Schematic

Note

- To evaluate the performance of one (1) TPS25985 eFuse at lower currents (< 60 A), RZ5, RZ6, RZ7, RZ8, & RZ9 resistors need to be depopulated, and R21 & R22 resistors should be populated to disable the secondary eFuse.
- The ground connections for the various components around the TPS25985 eFuses should be wired directly to each other and the GND pins of respective eFuses. This should be followed by connecting them to the system ground at one point, as implemented using RZ1 and RZ4 resistors in the EVM schematic. Do not connect the various component grounds through the high current system ground line.

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4 General Configurations

4.1 Physical Access

Table 4-1 lists the TPS25985EVM eFuse Evaluation Board input and output connectors functionalities. Table 4-2 and Table 4-3 describe the availability of test points and the functionalities of the jumpers. Table 4-4 presents the function of the signal LED indicators.

Table 4-1. Input and Output Connector Functionality

Connector	Label	Description
T1	VIN (+)	Positive terminal for the input power to the EVM
T2	VOUT (+)	Positive terminal for the output power from the EVM
T3	PGND (–)	Negative terminal for the EVM (Common for both input and output)

Table 4-2. Test Points Description

Test Points	Label	Description
TP1	S1_P	Kelvin sensing points to measure • Combined on-resistance with both TPS25985 eFuses enabled • On-resistance of the primary device (U1) when the secondary device (U2) disabled
TP2	S1_N	
TP3	VIN	Input Voltage
TP4	VOUT	Output Voltage
TP5	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP6	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP7	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP8	MODE2	MODE selection: Secondary Device
TP9	FLTb2	Open-drain active low fault indication: Secondary Device
TP10	VDD-PRI	Controller input power: Primary Device
TP11	FLTb	Open-drain active low fault indication: Primary Device
TP12	SWEN	Open-drain signal to indicate and control power switch ON and OFF status
TP13	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP14	TEMP	Maximum device die temperature monitor analog voltage output with two (2) TPS25985 eFuses in parallel
TP15	CMPM	General-purpose comparator negative input: Primary Device
TP16	CMPM2	General-purpose comparator negative input: Secondary Device
TP17	CMPP	General-purpose comparator positive input: Primary Device
TP18	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP19	CMPP2	General-purpose comparator positive input: Secondary Device
TP20	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP21	CMPOUT	General-purpose comparator open-drain output: Primary Device
TP22	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator

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Table 4-2. Test Points Description (continued)

Test Points	Label	Description
TP23	CMPOUT2	General-purpose comparator open-drain output: Secondary Device
TP24	OPTIONAL	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP25	DVDT	Start-up output slew rate control
TP26	ITIMER	Overcurrent blanking timer
TP27	IMON	Load current monitor and overcurrent & fast-trip thresholds during steady state
TP28	ILIM2	Current limit and fast-trip threshold during start-up: Secondary Device
TP29	ILIM	Current limit and fast-trip threshold during start-up: Primary Device
TP30	IREF	Reference voltage for overcurrent & short-circuit protections, and active current sharing blocks
TP31	MODE	MODE selection: Primary Device
TP32	PG	Open-drain active high power good indication
TP33	EN	Active high enable input
TP34	VDD-SEC	Controller input power: Secondary Device
TP35	+5V Pullup	5 V pullup power supply generated using a LDO from VIN
TP36	+1.2V Reference	Used to implement system level functionalities such as adjustable overvoltage protection, PROCHOT#™, load handshake, power good with adjustable thresholds, etc. using the built-in general-purpose comparator
TP37	VCC EXTERNAL	External pullup power supply
TP38	GD EXTERNAL	External gate signal for custom load transient
TP39	PGND	Supply ground
QGND1	QGND	Device ground
G1	QGND	Device ground
G2	QGND	Device ground

Table 4-3. Jumper Descriptions and Default Positions

Jumper	Label	Description	Default Jumper Position
J1	SWEN	1-2 Position: The SWEN pullup supply is generated from VIN using a Zener diode (RZ2 populated & RZ3 depopulated) or using a LDO (RZ2 depopulated & RZ3 populated)	1-2
		2-3 Position: The SWEN pin is connected to the ITIMER pin of the Primary Device through a 100-kΩ resistor	
J2	DVDT	1-2 Position sets the output slew rate to 1.8-V/ms	5-6
		3-4 Position sets the output slew rate to 12-V/ms	
		5-6 Position sets the output slew rate to 1.2-V/ms	
J3	ITIMER	1-2 Position sets the overcurrent blanking timer to 1.4-ms	3-4
		3-4 Position sets the overcurrent blanking timer to 14-ms	
J4	IMON	1-2 Position sets the circuit breaker threshold to 100-A with V_{IREF} of 1-V	1-2
		3-4 Position sets the circuit breaker threshold to 70-A with V_{IREF} of 1-V	
J5	ILIM	1-2 Position sets the inrush current limit to 32-A and the active current sharing threshold to 50-A with V_{IREF} of 1-V: Primary Device	1-2
		3-4 Position sets the inrush current limit to 22-A and the active current sharing threshold to 35-A with V_{IREF} of 1-V: Primary Device	
J6	IREF	1-2 Position sets the reference voltage for overcurrent, short-circuit protection, and active current sharing blocks to 0.8-V	3-4
		3-4 Position sets the reference voltage for overcurrent, short-circuit protection, and active current sharing blocks to 1-V	

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Table 4-3. Jumper Descriptions and Default Positions (continued)

Jumper	Label	Description	Default Jumper Position
J7	ILIM2	1-2 Position sets the inrush current limit to 32-A and the active current sharing threshold to 50-A with V_{IREF} of 1-V: Secondary Device	1-2
		3-4 Position sets the inrush current limit to 22-A and the active current sharing threshold to 35-A with V_{IREF} of 1-V: Secondary Device	
J8	VDD PULLUP POWER SUPPLY	1-2 Position provides the VDD pullup supply from the external power source	2-3
		2-3 Position provides the VDD pullup supply from the onboard 12-V to 5-V LDO	
J9	EXTERNAL GATE SIGNAL	1-2 Position provides the GATE signal to the MOSFETs (Q7 – Q9) from the onboard monoshot	1-2
		2-3 Position provides the GATE signal to the MOSFETs (Q7 – Q9) from the external signal generator	

Table 4-4. LED Descriptions

LED	Description
DG1	When ON, indicates that PG is asserted
DR1	When ON, indicates that FLTb is asserted
DR2	When ON, indicates that FLTb2 is asserted

4.2 Test Equipment and Setup

4.2.1 Power supplies

One adjustable power supply with 0-V to 30-V output and 0-A to 200-A output current limit

4.2.2 Meters

Two (2) Digital Multi Meters (DMM)

4.2.3 Oscilloscope

A DPO2024 or equivalent, three 10x voltage probes, and a DC current probe of 150 A rated

4.2.4 Loads

One resistive load or equivalent which can tolerate up to 200-A DC load at 24-V

5 Test Setup and Procedures

In this user's guide, the test procedure is described for TPS25985 eFuse. Make sure the evaluation board has default jumper settings as shown in Table 5-1.

Table 5-1. Default Jumper Setting for TPS25985EVM eFuse Evaluation Board

J1	J2	J3	J4	J5	J6	J7	J8	J9
1-2	5-6	3-4	1-2	1-2	3-4	1-2	2-3	1-2

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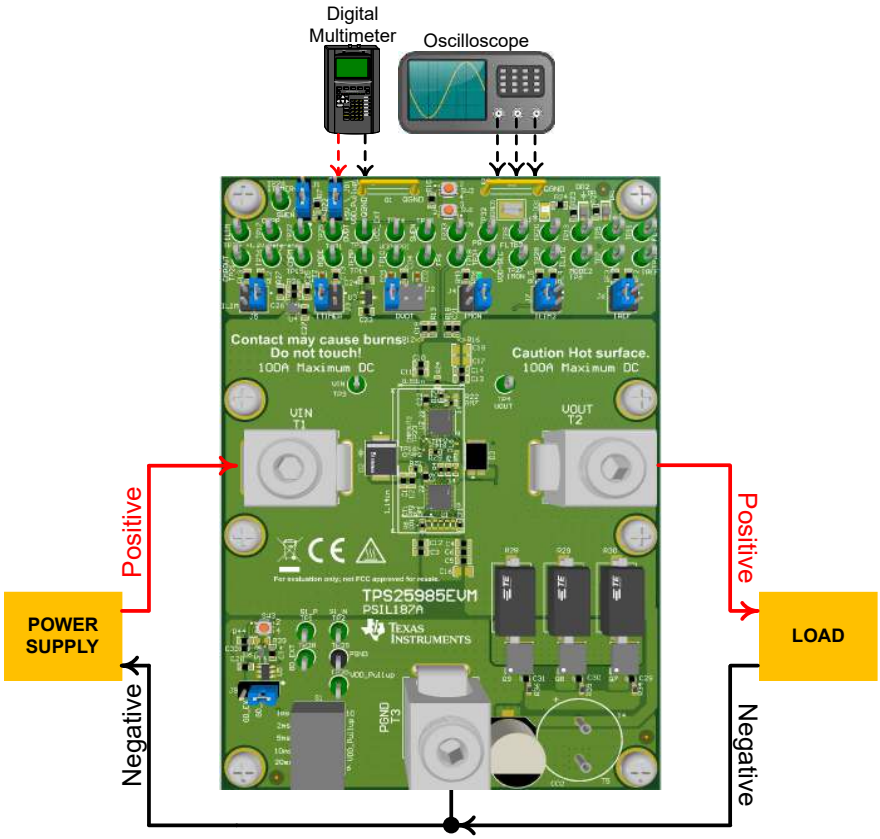

Figure 5-1. TPS25985EVM Setup with Test Equipment

Follow these instructions before starting any test and repeat again before moving to the next test:

- Set the power supply output (VIN) to zero volts.
- Turn off the power supply.
- Adjust the jumper positions on EVM to the default configuration as shown in Table 5-1.
- Turn the power supply on and set the power supply output (VIN) to 12 V, 200 A, and keep the power supply output disabled.
- Enable the power supply output so that the EVM gets the input power supply.

5.1 Hot Plug

Use the following instructions to measure the inrush current during a hot plug event:

1. Configure the jumper J2 position to the desired slew rate mentioned in Table 4-3.
2. Configure the jumpers J5 and J7 positions to the desired current limits during start-up as mentioned in Table 4-3.
3. Configure the jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as specified in Table 4-3.
4. Connect a load of 1.2 Ω between VOUT (Connector T2) and PGND (Connector T3).
5. Connect the negative terminal of the power supply to connector T3.
6. Set the input supply voltage VIN to 12 V and current limit to 100 A. Enable the power supply.
7. Hot plug the positive terminal of the power supply at connector T1.
8. Observe the waveforms at VOUT (TP4) and input current using an oscilloscope to measure the slew rate and rise time of the VOUT with a given input voltage of 12 V.

Figure 5-2 and Figure 5-3 show the examples of inrush current captured on the TPS25985EVM eFuse Evaluation Board with two (2) devices in parallel during the hot plug event.

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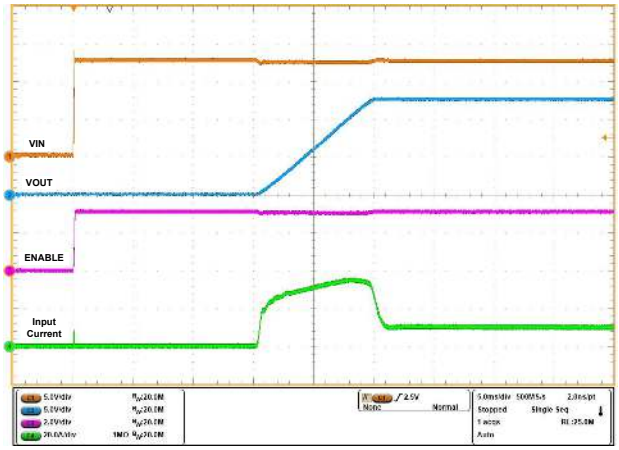

Figure 5-2. TPS25985 eFuse Hot Plug Profile (V_{IN} Stepped Up from 0 V to 12 V, C_{OUT} = 18.47 mF, C_{DVDT} = 33 nF, and R_{LOAD} = 1.2 Ω)

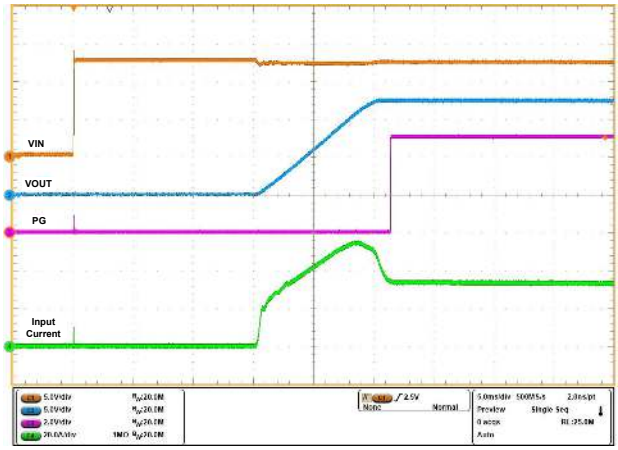

Figure 5-3. TPS25985 eFuse Hot Plug Profile (V_{IN} Stepped Up from 0 V to 12 V, C_{OUT} = 18.47 mF, C_{DVDT} = 33 nF, and R_{LOAD} = 0.37 Ω)

5.2 Start-up with Enable

Use the following instructions to power up the TPS25985 eFuse with ENABLE:

1. Configure the jumper J2 position to the desired slew rate mentioned in Table 4-3.
2. Configure the jumpers J5 and J7 positions to the desired current limits during start-up as mentioned in Table 4-3.
3. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
4. Set the input supply voltage VIN to 12 V and current limit to 100 A.
5. Connect a load of 1.2 Ω between VOUT (Connector T2) and PGND (Connector T3).
6. Connect the input supply between VIN (Connector T1) and PGND (Connector T3).
7. Turn on the power supply by keeping the device disabled using the switch SW1.
8. Enable the eFuses by releasing the switch SW1.
9. Observe the waveform at VOUT (TP4) and input current using an oscilloscope to measure the slew rate and rise time of the VOUT with a given input voltage of 12 V.

Figure 5-4 shows the start-up profile of TPS25985 eFuse with ENABLE using two (2) devices in parallel.

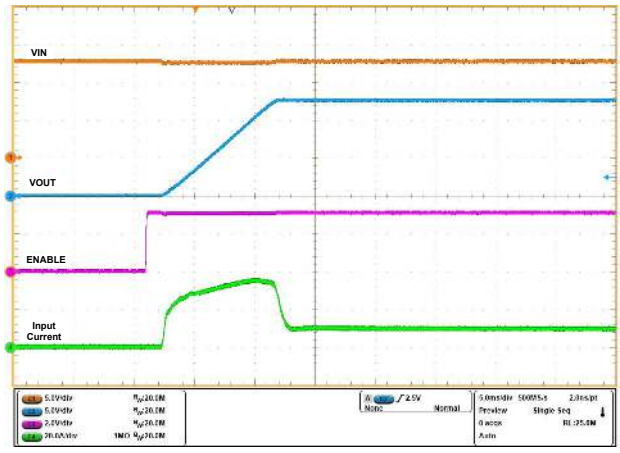

Figure 5-4. TPS25985 eFuse Start-up Profile with ENABLE (V_{IN} = 12 V, EN Stepped Up from 0 V to 3 V, C_{OUT} = 18.47 mF, R_{LOAD} = 1.2 Ω, and C_{DVDT} = 33 nF)

5.3 Difference Between Current Limit and DVDT Based Start-up Mechanisms

Use the following instructions to perform the start-up with current limit test:

1. Configure the jumper J2 position to the desired slew rate mentioned in Table 4-3.

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2. Configure the jumpers J5 and J7 positions to the desired current limits during start-up as mentioned in Table 4-3.
3. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
4. Set the input supply voltage VIN to 12 V and current limit to 100 A.
5. Connect a load of 0.9 Ω between VOUT (Connector T2) and PGND (Connector T3).
6. Connect the input supply between VIN (Connector T1) and PGND (Connector T3).
7. Turn on the power supply by keeping the device disabled using the switch SW1.
8. Enable the eFuse by releasing the switch SW1.
9. Observe the waveform at VOUT (TP4) and input current using an oscilloscope. The main intention of this experiment is to observe the output voltage & input current profiles and time required to complete the inrush with two different ILIM set points having all other test conditions identical. The inrush current hits the current limit set point in one case, but does not in the next.

Figure 5-5 and Figure 5-6 show the difference between the current limit and DVDT based start-up mechanisms on the TPS25985EVM eFuse Evaluation Board having two (2) devices in parallel for R_{ILIM} of 680 and R_{LIM2} of 680 Ω and R_{ILIM} of 402 and R_{LIM2} of 402 Ω respectively.

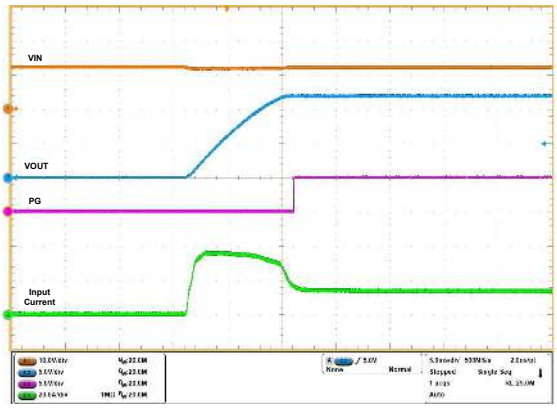

Figure 5-5. Start-up with Current Limit Response of TPS25985 eFuse (V_{IN} = 12 V, EN Stepped Up from 0 V to 3 V, R_{ILIM} = 680 Ω, R_{LIMI2} = 680 Ω, R_{IREF} = 40.2 kΩ, C_{OUT} = 18.47 mF, R_{LOAD} = 0.9 Ω, and C_{DVDT} = 33 nF)

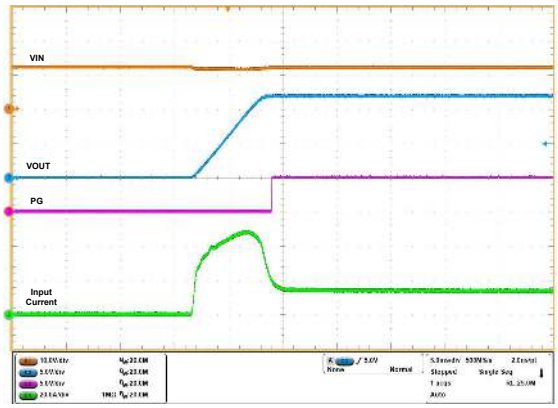

Figure 5-6. Start-up with Output Slew Rate Control (only) Response of TPS25985 eFuse (V_{IN} = 12 V, EN Stepped Up from 0 V to 3 V, R_{ILIM} = 402 Ω, R_{ILIM2} = 402 Ω, R_{IREF} = 40.2 kΩ, C_{OUT} = 18.47 mF, R_{LOAD} = 0.9 Ω, and C_{DVDT} = 33 nF)

5.4 Power-up into Short

Use the following instructions to perform the power-up into short test:

1. Set the input supply voltage VIN to 12 V and current limit to 100 A. Connect the supply between VIN (Connector T1) and PGND (Connector T3) and keep the power supply OFF.
2. Short the output of the EVM. For example, VOUT (Connector T2) to PGND (Connector T3) through a short and thick cable to make sure the short-circuited path impedance is minimum as possible.
3. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
4. Configure the jumpers J5 and J7 positions to the desired current limits during start-up as mentioned in Table 4-3.
5. Keep the TPS25985 eFuses disabled by pushing the switch SW1.
6. Turn ON the power supply.
7. Enable the TPS25985 eFuse by releasing the switch SW1.

Figure 5-7 and Figure 5-8 show the test waveforms of power up into output short on the TPS25985EVM eFuse Evaluation Board with two (2) devices in parallel.

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Note

During powerup into short, a thermal foldback will result in the current flowing through the device being less than the calculated value of the current limit during start-up.

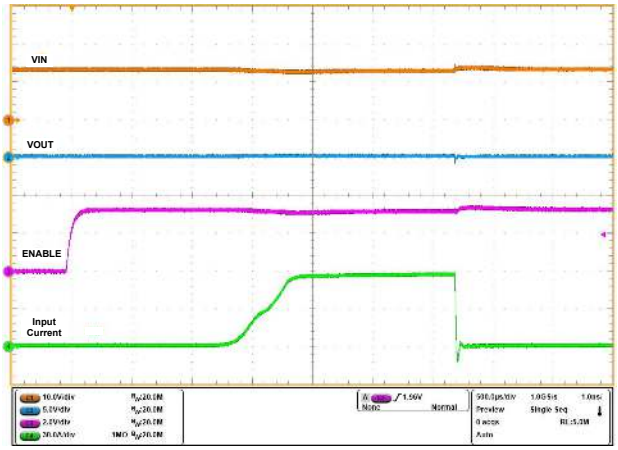

Figure 5-7. Power-up into Output Short Response of TPS25985 eFuse (V_{IN} = 12 V, EN Stepped Up from 0 V to 3 V, R_{ILIM} = 402 Ω, R_{ILIM2} = 402 Ω, R_{IREF} = 40.2 kΩ, C_{ITIMER} = 22 nF, and OUT Shorted to PGND)

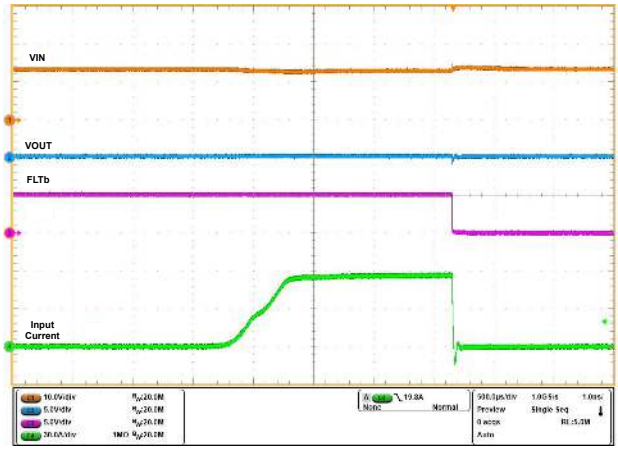

Figure 5-8. Power-up into Output Short Response of TPS25985 eFuse (V_{IN} = 12 V, EN Stepped Up from 0 V to 3 V, R_{ILIM} = 402 Ω, R_{ILIM2} = 402 Ω, R_{IREF} = 40.2 kΩ, C_{ITIMER} = 22 nF, and OUT Shorted to PGND)

5.5 Overvoltage Lockout

Use the following instructions to perform the overvoltage protection test:

1. Set the input supply voltage VIN to 12 V and current limit to 100 A. Apply the supply between VIN (Connector T1) and PGND (Connector T3) and enable the power supply.
2. Apply a load of 1.2 Ω between VOUT (Connector T2) and PGND (Connector T3).
3. Increase the input supply VIN from 12 V to 18 V and observe the waveforms using an oscilloscope.

Note

The input TVS diodes should be removed during the overvoltage protection test. **Make sure to put them back after this experiment.**

Figure 5-9 shows overvoltage lockout response of TPS25985 eFuse on TPS25985EVM eFuse Evaluation Board.

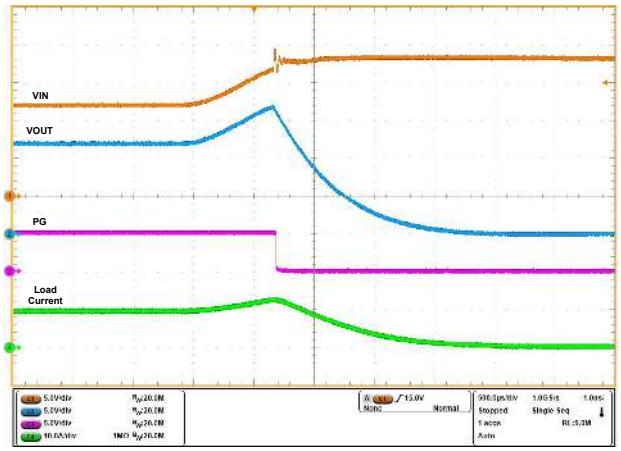

Figure 5-9. Overvoltage Lockout Response of TPS25985 eFuse (V_{IN} Ramped Up from 12 V to 18 V, C_{OUT} = 470 µF, and R_{LOAD} = 1.2 Ω)

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5.6 Transient Overload Performance

Use the following instructions to observe the transient overload performance:

1. Configure the Jumper J3 to an appropriate position to obtain required overcurrent blanking period (t_{TIMER}) as per Table 4-3.
2. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
3. Configure the Jumper J4 in a suitable position to set required circuit breaker threshold (I_{OCP}) as per Table 4-3.
4. Set the input supply voltage VIN to 12-V and current limit of 200-A.
5. Connect the power supply between VIN (Connector T1) & PGND (Connector T3) and enable the power supply.
6. Now apply an overload in the range of $I_{OCP} < I_{LOAD} < 2 \times I_{OCP}$ between VOUT (Connector T2) and PGND (Connector T3) for a time duration less than t_{TIMER} decided by using jumper J3.
7. Observe the waveforms using an oscilloscope.

Figure 5-10 shows transient overload performance of TPS25985 eFuse on TPS25985EVM eFuse Evaluation Board with two (2) devices in parallel.

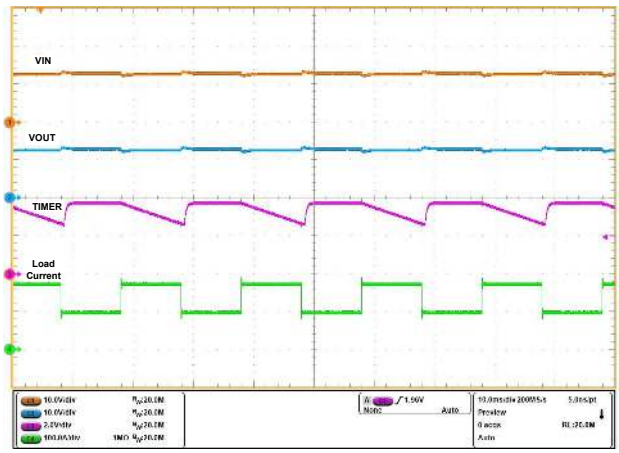

Figure 5-10. Transient Overload Performance of TPS25985 eFuse (V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 470 µF, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, I_{OUT} Ramped from 100 A to 175 A then 100 A within 10 ms)

5.7 Overcurrent Event

Use the following instructions to perform the overcurrent test on TPS25985 eFuse:

1. Configure the Jumper J3 to an appropriate position to obtain required overcurrent blanking period (t_{TIMER}) as per Table 4-3.
2. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
3. Configure the Jumper J4 in a suitable position to set required circuit breaker threshold (I_{OCP}) as per Table 4-3.
4. Set the input supply voltage VIN to 12-V and current limit of 200-A.
5. Connect the power supply between VIN (Connector T1) & PGND (Connector T3) and enable the power supply.
6. Now apply an overload in the range of $I_{OCP} < I_{LOAD} < 2 \times I_{OCP}$ between VOUT (Connector T2) and PGND (Connector T3) for a time duration more than t_{TIMER} decided by using jumper J3.
7. Observe the waveforms using an oscilloscope.

Figure 5-11 and Figure 5-12 show the circuit breaker response of TPS25985 eFuse on TPS25985EVM eFuse Evaluation Board with two (2) devices in parallel.

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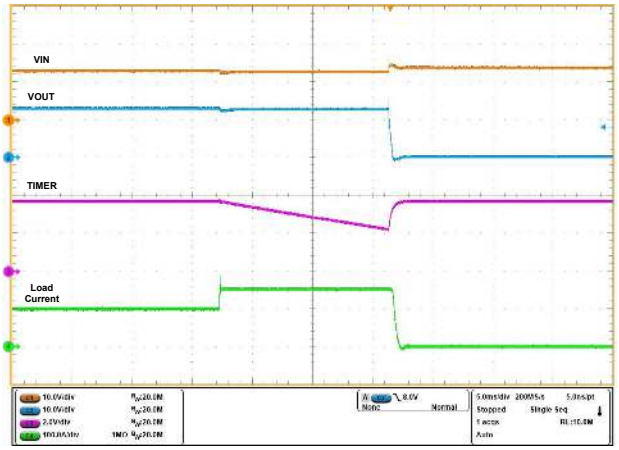

Figure 5-11. Overcurrent Performance of TPS25985 eFuse (V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 470 µF, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, I_{OUT} Ramped from 100 A to 150 A for 20 ms)

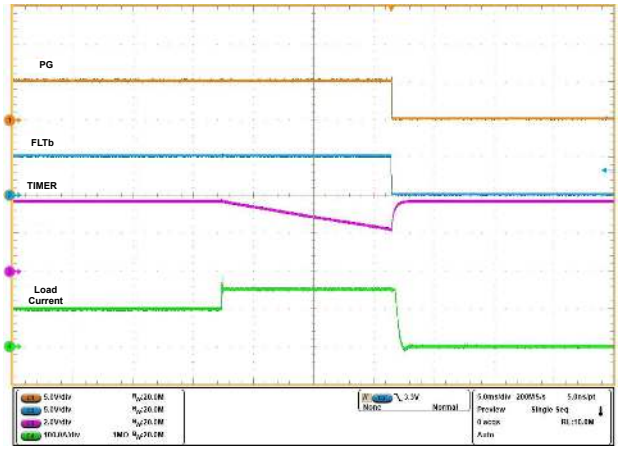

Figure 5-12. Overcurrent Performance of TPS25985 eFuse (V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 470 µF, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, I_{OUT} Ramped from 100 A to 150 A for 20 ms)

5.8 Provision to Apply Load Transient and Overcurrent Event Using an Onboard Switching Circuit

The TPS25985EVM provides an add-on circuit to facilitate load transients and persistent overcurrent events. The implementation consists of three (3) low side MOSFETs (Q7, Q8, and Q9) and a monoshot gate driver circuit (U5 and U6) as well as six (6) onboard load resistors of 1 ohm each (R28 to R33) in parallel. Using a single pole single through (SPST) switch (S1), the monoshot gate driver generates a gate signal of 1 ms, 2 ms, 5 ms, 10 ms, and 20 ms durations. By doing this, the low side MOSFETs (Q7, Q8, and Q9) are turned on for that specific duration, creating a load transient in addition to the steady-state load. Use the following instructions to apply a load transient or persistent overcurrent event using this onboard switching circuit:

1. Configure the Jumper J3 to an appropriate position to obtain required overcurrent blanking period (t_{TIMER}) as per Table 4-3.
2. Configure the Jumper J6 position to desired reference voltage for overcurrent protection and active current sharing as mentioned in Table 4-3.
3. Configure the Jumper J4 in a suitable position to set required circuit breaker threshold (I_{OCP}) as per Table 4-3.
4. Set the input supply voltage VIN to 12 V and current limit to 200 A.
5. Connect the power supply between VIN (Connector T1) and PGND (Connector T3) and enable the power supply.
6. Connect a steady state load between VOUT (Connector T2) and PGND (Connector T3).
7. Use the single pole single through (SPST) switch (S1) to configure the transient load turn on duration.
8. Press the switch SW3 to turn on the Q7, Q8, and Q9 MOSFETs, which creates a load transient of 72 A (typical) between VOUT and PGND with 12 V output.
9. Observe the waveforms of VOUT (TP4), MOSFET GATE (J9), and input current using an oscilloscope.

Another option is to apply a custom load transient using an external function generator, connected between TP38 and TP39, and the shunt of jumper J9 set to "2-3".

CAUTION

In that case, make sure to limit the transient load current magnitude to a safe level for reliable operation of the load resistors (R28 to R33) based on their maximum permissible peak pulse power vs pulse duration plot.

Figure 5-13 and Figure 5-14 show the test waveforms of transient overload and persistent overload events respectively using the onboard switching circuit.

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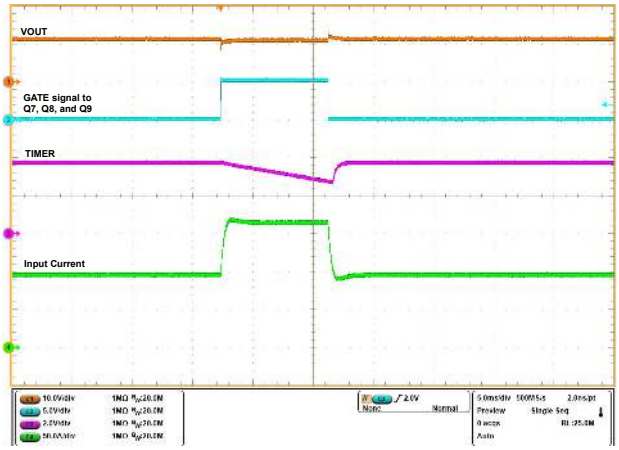

Figure 5-13. Transient Overload Performance in TPS25985EVM Using the Onboard Switching Circuit (V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 470 µF, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, $I_{OUT(Steady-State)}$ = 100 A, and $I_{OUT(Transient)}$ = 69 A for 9 ms)

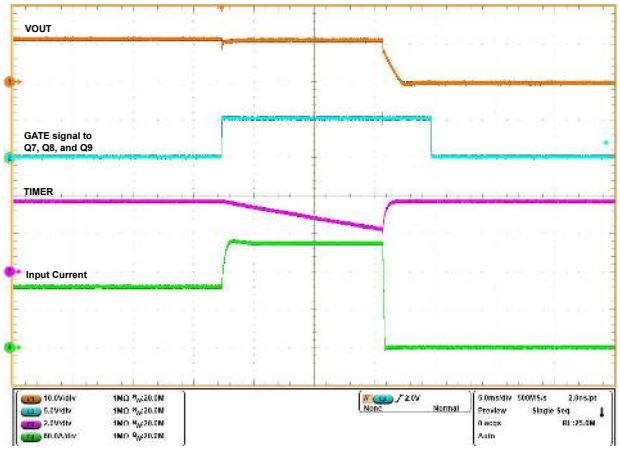

Figure 5-14. Persistent Overload Performance in TPS25985EVM Using the Onboard Switching Circuit (V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 470 µF, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, $I_{OUT(Steady-State)}$ = 100 A, and $I_{OUT(Transient)}$ = 69 A for 18 ms)

5.9 Output Hot Short

Use the following instructions to perform the output hot short test:

1. Set the input supply voltage VIN to 12 V and connect the power supply between VIN (Connector T1) and PGND (Connector T3).
2. Turn ON the power supply.
3. Short the output of the device for example, VOUT (Connector T2) to PGND (Connector T3) through a shorter cable, which is just enough to insert a 150 A current probe.
4. Observe the waveforms using an oscilloscope.

Figure 5-15 shows the test waveforms of output hot short on the TPS25985EVM with two (2) TPS25985 eFuses in parallel.

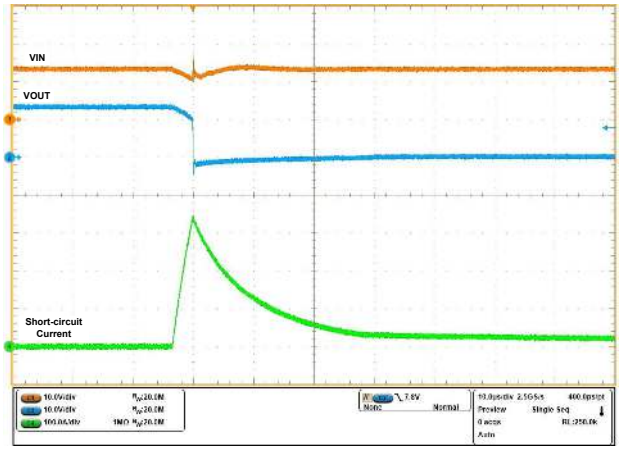

Figure 5-15. Output Hot Short Response in TPS25985EVM (V_{IN} = 12 V, R_{IMON} = 1.11 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, and C_{OUT} = 10 µF)

Make sure there is sufficient input capacitor to eliminate voltage dips at the input. A combination of electrolytic and ceramic capacitors are preferred. With these capacitors, a large current can be provided for a short period of time during short-circuit.

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Note

It is very difficult to obtain repeatable and similar short-circuit testing results. The following contributes to the variation in results:

- Source bypassing
- Input leads
- Board layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Hence, do not expect to see waveforms exactly like the waveforms in this user's guide because every setup is different.

5.10 PROCHOT#™ Implementation Using General-Purpose Comparator

Use the following instructions to implement PROCHOT#™ functionality using in-built general-purpose comparator:

1. Configure the Jumper J3 to an appropriate position to obtain required overcurrent blanking period (t_{TIMER}) as per Table 4-3.
2. Configure the Jumper J6 position to desired reference voltage (V_{IREF}) for overcurrent protection and active current sharing as mentioned in Table 4-3.
3. Configure the jumper J4 in a suitable position to set required circuit breaker threshold (I_{OCP}) as per Table 4-3.
4. Connect the CMPM pin (TP15) to the output of LDO, U4 (TP36) and adjust the values of R26 and R27 to make the voltage at TP36 to be 80% of V_{IREF}.
5. Connect CMPP (TP17) with IMON (TP27).
6. Set the input supply voltage VIN to 12-V and connect the power supply between VIN (Connector T1) and PGND (Connector T3).
7. Now apply a transient load in the range of $0.7 \times I_{OCP} < I_{LOAD} < 0.95 \times I_{OCP}$ (as example) between VOUT (Connector T2) and PGND (Connector T3) for a specified time duration, as example 20-ms, which is less than $2 \times t_{TIMER}$ decided by using jumper J3.
8. Observe the waveforms of CMPM (TP15), CMPP (TP17), CMPOUT (TP21), and load current using an oscilloscope.

Figure 5-16 shows the experimental waveforms of PROCHOT#™ implementation on the TPS25985EVM eFuse Evaluation Board.

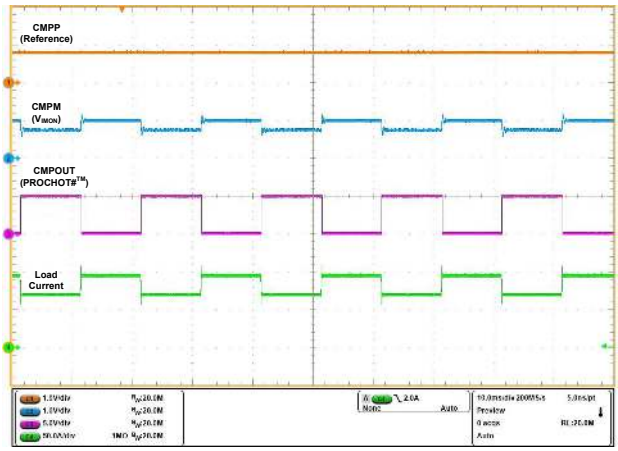

Figure 5-16. PROCHOT#™ Implementation on TPS25985 eFuse (V_{IN} = 12 V, R_{IMON} = 1.1 ‖ 1.1 kΩ, R_{IREF} = 40.2 kΩ, V_{CMPM} = 0.8 V, and I_{OUT} Ramped from 70 A to 95 A then 70 A within 20 ms)

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5.11 Quick Output Discharge (QOD)

Use the following instructions to observe the Quick Output Discharge (QOD) functionality:

1. Set the input supply voltage VIN to-12 V and current limit to 10-A. Turn ON the power supply.
2. Use the switch SW1 to connect the EN/UVLO pin to ground to do power cycling.
3. Use the switch SW2 to enable the QOD by making the voltage at EN/UVLO pin in the range of 0.8-V to 1.1-V with the input voltage of 9.8-V to 13.5-V.
4. Observe the waveforms of VIN (TP3), VOUT (TP4), PG(TP32), and EN(TP33) using an oscilloscope.

In Figure 5-17, the turn-off performance of the TPS25985 eFuse with QOD enabled is shown, whereas Figure 5-18 illustrates the turn-off performance with QOD disabled on the TPS25985EVM eFuse Evaluation Board.

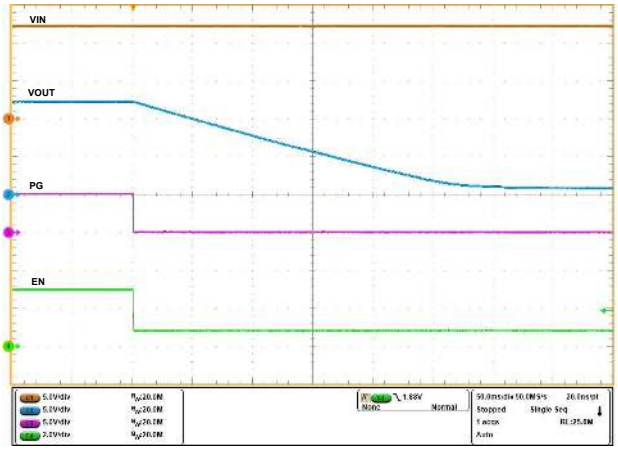

Figure 5-17. QOD Enabled on TPS25985 eFuse (V_{IN} = 12 V, C_{OUT} = 470 µF, and EN Pulled Low to 0.8 V)

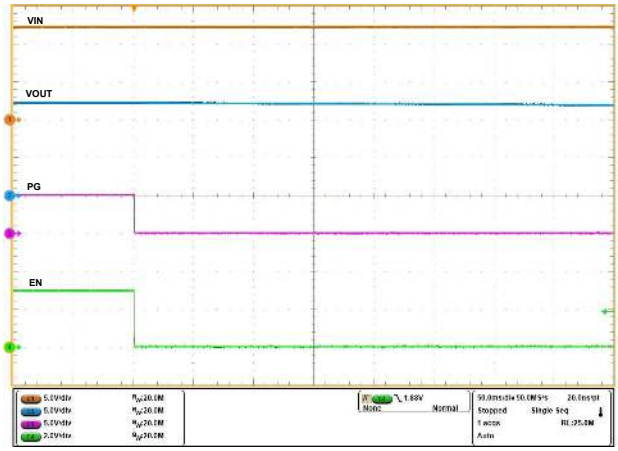

Figure 5-18. QOD Disabled on TPS25985 eFuse (V_{IN} = 12 V, C_{OUT} = 470 µF, and EN Pulled Low to 0 V)

5.12 Thermal Performance of TPS25985EVM

Use the following instructions to evaluate the thermal performance of TPS25985EVM:

1. Configure the Jumper J6 position to desired reference voltage (V_{IREF}) for overcurrent protection and active current sharing as mentioned in Table 4-3. The "3-4" position of the jumper J6 is selected in this experiment, which makes V_{IREF} as 1 V (typical).
2. Configure the jumper J4 in a suitable position to set required circuit breaker threshold (I_{OCP}) as per Table 4-3. Both the "1-2" and "3-4" positions of the jumper J4 are selected in this experiment, which makes I_{OCP} as 170 A (typical) with V_{IREF} as 1 V (typical).
3. Set the input supply voltage VIN to 12 V and current limit of 110 A.
4. Connect the power supply between VIN (Connector T1) and PGND (Connector T3) and enable the power supply.
5. Now apply a load of 100 A (DC) between VOUT (Connector T2) and PGND (Connector T3) for half an hour or more to reach the thermal equilibrium point.
6. Capture the thermal image of the EVM or monitor the voltage at TEMP (TP14) pin using a digital multimeter. Voltage at the TEMP (V_{TEMP}) pin reports the maximum die temperature between two (2) TPS25985 eFuses, which can be obtained using Equation 1.

$$T_J(°C) = \left[25 + \left\{\frac{V_{TEMP}(mV) - 677.6}{2.72\ (mV/°C)}\right\}\right] \quad (1)$$

Figure 5-19 shows the thermal performance of TPS25985EVM with two (2) TPS25985 eFuses in parallel.

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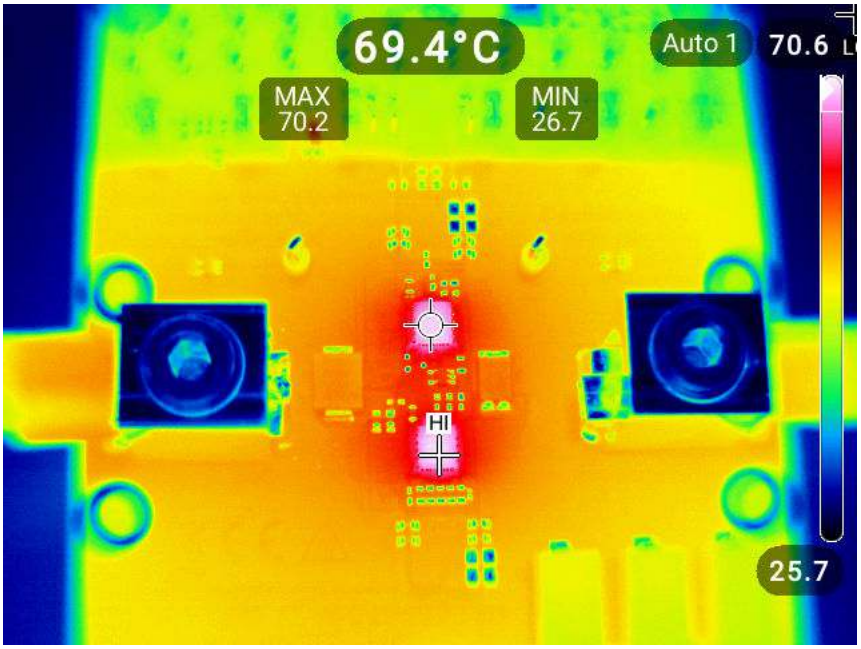

Figure 5-19. Thermal Performance of TPS25985EVM (V_{IN} = 12 V, I_{OUT} = 100 A, T_A = 25 ºC, and no external air flow)

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6 EVAL Board Assembly Drawings and Layout Guidelines

6.1 PCB Drawings

Figure 6-1 and Figure 6-2 show the component placements of the EVM. A pictorial representation of the TPS25985EVM PCB layers can be found in Figure 6-3 to Figure 6-10.

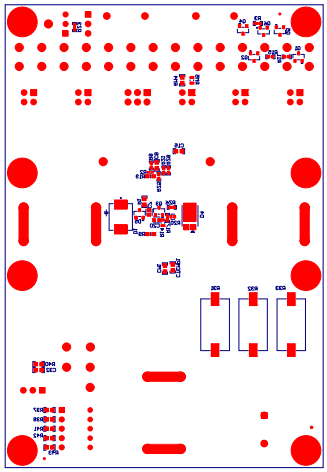

Figure 6-1. TPS25985EVM Board: Top Assembly

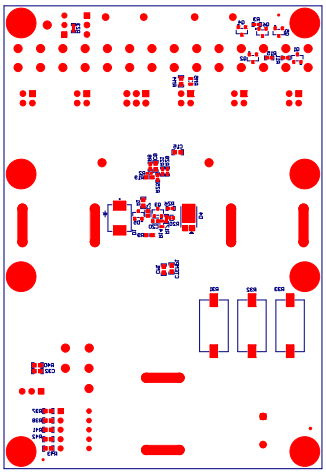

Figure 6-2. TPS25985EVM Board: Bottom Assembly

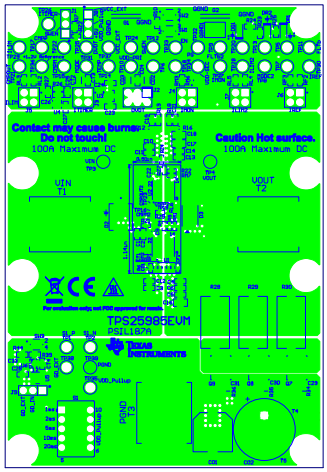

Figure 6-3. TPS25985EVM Board: Top Layer

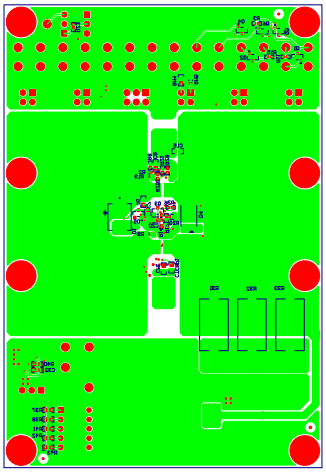

Figure 6-4. TPS25985EVM Board: Bottom Layer

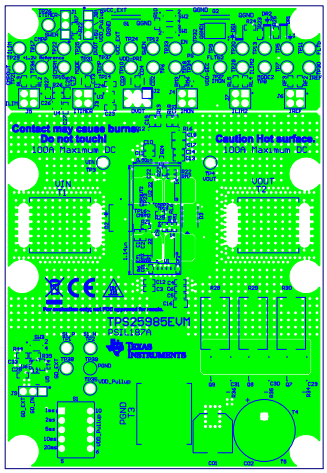

Figure 6-5. TPS25985EVM Board: Layer 2 (Power)

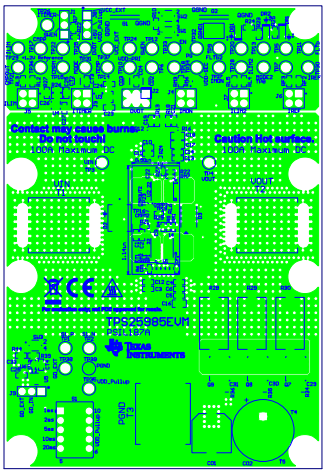

Figure 6-6. TPS25985EVM Board: Layer 3 (Power)

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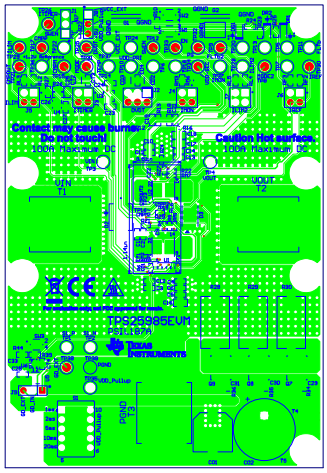

Figure 6-7. TPS25985EVM Board: Layer 4 (Signal)

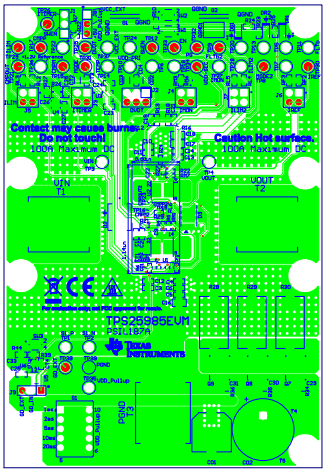

Figure 6-8. TPS25985EVM Board: Layer 5 (Signal)

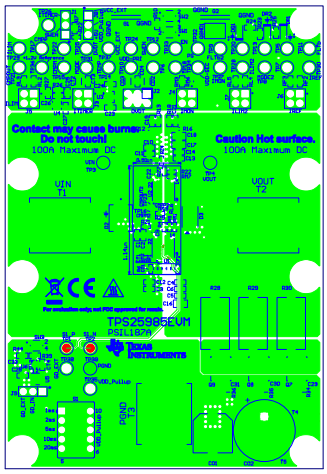

Figure 6-9. TPS25985EVM Board: Layer 6 (Power)

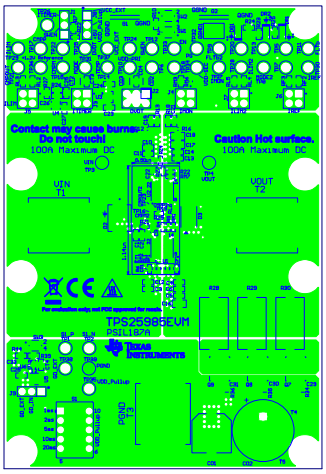

Figure 6-10. TPS25985EVM Board: Layer 7 (Power)

Note

Analog signal nets, such as IREF, IMON, and TEMP, should be routed away as much as possible from power nets, such as VIN, VOUT, and PGND.

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7 Bill Of Materials (BOM)

Table 7-1 lists the EVM BOM.

Table 7-1. TPS25985EVM Bill of Materials

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
!PCB1	1		Printed Circuit Board		PSIL187	Any	
C1, C3, C6, C10, C12, C14	6	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, 0603	0603	C1608X7R1V105K080AC	TDK	
C2, C4, C11, C13, CT4	5	0.1uF	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603C104K5RACAUTO	Kemet	
C5, C15	2	2.2uF	CAP, CERM, 2.2 uF, 35 V, +/- 10%, X5R, 0603	0603	GRM188R6YA225KA12D	MuRata	
C7	1	47nF	Cap Ceramic 0.047uF 25V X7R 5% SMD 0603 125°C Paper T/R	FP-C0603C473J3RAC7867_0603-MFG	C0603C473J3RAC7867	KEMET	
C8, C19, C21	3	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H102JA01D	MuRata	
C9, C22	2	2.2uF	CAP, CERM, 2.2 µF, 25 V,+/- 10%, X7S, 0603	0603L	GRM188C71E225KE11D	MuRata	
C20, CD2, CT2	3	22nF	Cap Ceramic 22000pF 50V X7R 10% Pad SMD 0603 Soft Termination +125°C Automotive T/R	FP-GCJ188R71H223KA01D_0603-MFG	GCJ188R71H223KA01D	Murata	
C23, C24, C25, C27	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	06035C104KAT2A	AVX	
C26	1	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H100JA01D	MuRata	
C28	1	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71E105KA64D	MuRata	
C29, C30, C31, C33	4	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603S	885012006057	Wurth Elektronik	

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
C32	1	0.1uF	CAP, CERM, 0.1 µF, 16 V,+/- 10%, X7R, 0603	0603	CL10B104KO8WPNC	Samsung Electro-Mechanics	
CD3	1	33nF	Cap Ceramic 33000pF 50V X7R 10% Pad SMD 0603 Soft Termination +125°C Automotive T/R	FP-GCJ188R71H333KA12D_0603-MFG	GCJ188R71H333KA12D	Murata	
CD4	1	3300pF	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H332JA01D	MuRata	
CF1	1	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402	CGA2B2C0G1H102J050BA	TDK	
CM1	1	22pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H220JA01D	MuRata	
CO1	1	470uF	CAP, AL, 470 uF, 25 V, +/- 20%, SMD	CAPSMT_62_JA0	EMVE250ADA471MJA0G	Chemi-Con	
CT3	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata	
CTEMP1	1	22pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A220JAT2A	AVX	
D1, D2	2		19.9V Clamp 150.8A Ipp Tvs Diode Surface Mount DO-214AB (SMCJ)	FP-SMDJ12A_DO214AB-MFG	SMDJ12A	Littelfuse Inc	
D3, D4	2	45V	Diode, Super Barrier Rectifier, 45 V, 10 A, PowerDI5	POWERDI5	SBR10U45SP5-13	Diodes Inc.	
D5	1		Zener Diode 4.7 V 250 mW ±1% Surface Mount TO-236AB	FP-BZX84-A4V7,215_SOT23-3-MFG	BZX84-A4V7,215	Nexperia	
DG1	1	Green	LED, Green, SMD	LG_R971_Green	LG R971-KN-1	OSRAM	
DR1, DR2	2	Red	LED, Red, SMD	LS_R976_Red	LS R976-NR-1	OSRAM	
G1, G2	2		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Harwin_D3082-05	D3082-05	Harwin	

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
H1, H2, H3, H4, H9, H10, H11, H12	8		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	NY PMS 440 0025 PH	B&F Fastener Supply	
H5, H6, H7, H8, H13, H14, H15, H16	8		Standoff, Hex, 0.5"L #4-40 Nylon	Keystone_1902C	1902C	Keystone	
J1, J8, J9	3		Header, 100mil, 3x1, Tin, TH	CONN_PEC03SAAN	PEC03SAAN	Sullins Connector Solutions	
J2	1		Header, 100mil, 3x2, Tin, TH	SULLINS_PEC03DAAN	PEC03DAAN	Sullins Connector Solutions	
J3, J4, J5, J6, J7	5			FP-PEC02DABN_HDR4-MFG	PEC02DABN	Sullins Connector Solutions	
Q1, Q2, Q3, Q4, Q5, Q6	6		N-Channel 30 V 3.16A (Ta) 750mW (Ta) Surface Mount SOT-23-3 (TO-236)	FP-SI2306BDS-T1-GE3_SOT23-3-MFG	SI2306BDS-T1-GE3	Vishay Siliconix	
Q7, Q8, Q9	3	40V	MOSFET, N-CH, 40 V, 42 A, DNK0008A (VSON-CLIP-8)	DNK0008A	CSD18510Q5B	Texas Instruments	
QGND1	1		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone	
R1	1	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo	
R2	1	1.0Meg	RES, 1.0 M, 5%, 0.063 W, 0402	0402L	CRCW04021M00JNED	Vishay-Dale	
R3, R4, R5, R6	4	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America	
R7, R13, R42	3	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale	
R8	1	330k	RES, 330 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330KFKED	Vishay-Dale	
R9, R19, R34, R35, R36	5	10	Res General Purpose Thick Film 0603 10 Ohm 5% 1/10W ±200ppm/°C Molded SMD Paper T/R	FP-RC0603JR-0710RL_0603-MFG	RC0603JR-0710RL	Yageo	
R10	1	121k	RES, 121 k, 1%, 0.1 W, 0603	0603	RC0603FR-07121KL	Yageo	

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
R18	1	110k	RES, 110 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603110KFKEA	Vishay-Dale	
R20	1	300k	300 kOhms ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Moisture Resistant Thick Film	FP-RC0402JR-07300KL_0402-MFG	RC0402JR-07300KL	Yageo	
R23, R24, R25	3	470	RES, 470, 5%, 0.1 W, 0603	0603	RC0603JR-07470RL	Yageo	
R26	1	249k	RES, 249 k, 1%, 0.1 W, 0603	0603	CRCW0603249KFKEA	Vishay-Dale	
R27	1	499k	RES, 499 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF4993V	Panasonic	
R28, R29, R30, R31, R32, R33	6	1	Res Wirewound 1 Ohm 5% 5W ±200ppm/°C Molded SMD T/R	FP-SMW51R0JT_5329-IPC_C	SMW51R0JT	TE Connectivity	
R37	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale	
R38	1	20.0k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	CRCW060320K0FKEA	Vishay-Dale	
R40, R44	2	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC0603JR-0710KL	Yageo	
R41	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale	
R43	1	200k	RES, 200 k, 1%, 0.1 W, 0603	0603	CRCW0603200KFKEA	Vishay-Dale	
RF2	1	31.6k	RES, 31.6 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE0731K6L	Yageo America	
RF3	1	40.2k	RES, 40.2 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE0740K2L	Yageo America	
RL2, RL4	2	402	RES, 402, 0.1%, 0.1 W, 0603	0603	RT0603BRD07402RL	Yageo America	
RL3, RL5	2	576	RES, 576, 0.1%, 0.1 W, 0603	0603	RT0603BRD07576RL	Yageo America	
RM3, RM4	2	1.58k	RES, 1.58 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD071K58L	Yageo America	

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
RM5, RM6	2	1.1k	1.1 kOhms ±0.1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant Thin Film	FP-TNPW06031K10BYEN_0603-MFG	TNPW06031K10BYEN	Vishay	
RM7	1	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale	
RZ1, RZ2, RZ4, RZ5, RZ6, RZ7, RZ8, RZ9	8	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale	
S1	1		Switch, SPST 5Pos, Rocker, TH	SW_76SB05	76SB05ST	Grayhill	
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9	9		Shunt, 2.54mm, Gold, Blue	Wurth_60900213621	60900213621	Wurth Elektronik	
SW1, SW2, SW3	3		Tactile Switch SPST-NO Top Actuated Surface Mount	FP-PTS830GM140SMTRLFS_SMT_3MM05_2MM6-MFG	PTS830GM140SMTRLFS	C&K Components	
T1, T2, T3	3		1/0 AWG High AMP PCB Wire Lugs 1/0-8 AWG	FP-B1-0-PCB-L_WIRE_LUG_150A_1-0AWG-MFG	B1/0-PCB-L	INTERNATIONAL HYDRAULICS	
T4, T5	2		Connector, Receptacle, Pin, TH	CONN_0300-2-15-01-47-01-10-0	0300-2-15-01-47-01-10-0	Mill-Max	
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP17, TP18, TP20, TP21, TP22, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38	35		Test Point, Multipurpose, Green, TH	Keystone5126	5126	Keystone	
TP39	1		Test Point, Multipurpose, Black, TH	Keystone5011	5011	Keystone	
U1, U2	2		TPS259850RQP	RQP0026A-MFG	TPS259850RQP	Texas Instruments	Do Not Procure

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
U3	1		100-mA, 30-V, Fixed-Output, Linear-Voltage Regulator, DBZ0003A (SOT-23-3)	DBZ0003A_N	TLV76050DBZR	Texas Instruments	
U4	1		1-A, Positive Voltage Regulator, DRV0006A (WSON-6)	DRV0006A	TLV76701DRVR	Texas Instruments	
U5	1		Single-Channel High-Speed Low-Side Gate Driver with 5V Negative Input Voltage Handling Ability, DBV0006A (SOT-23-6)	DBV0006A_N	UCC27511AQDBVRQ1	Texas Instruments	
U6	1		Single Retriggerable Monostable Multivibrator with Schmitt-Trigger Inputs, YZP0008ADAD, LARGE T&R	YZP0008ADAD	SN74LVC1G123YZPR	Texas Instruments	
C16, C17, C18	3	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, 0805	0805_HV	GMK212B7105KG-T	Taiyo Yuden	DNL
CD1	1	3300pF	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603S	GRM1885C1H332JA01D	MuRata	DNL
CO2	1	4700uF	CAP, AL, 4700 uF, 25 V, +/- 20%, TH	KMQ_1600x2500	EKMQ250EIV472ML25S	Chemi-Con	DNL
CT1	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603S	GRM1885C1H222JA01D	MuRata	DNL
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial6.4-20	N/A	N/A	Do Not Procure
R11, R15, R17, R21, R22	5	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America	DNL
R12, R16	2	1.0Meg	RES, 1.0 M, 5%, 0.063 W, 0402	0402L	CRCW04021M00JNED	Vishay-Dale	DNL

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Table 7-1. TPS25985EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Footprint	Part Number	Manufacturer	Comments
R14, RM2	2	1.1k	1.1 kOhms ±0.1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant Thin Film	FP-TNPW06031K10BYEN_0603-MFG	TNPW06031K10BYEN	Vishay	DNL
R39	1	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC0603JR-0710KL	Yageo	DNL
RF1	1	40.2k	RES, 40.2 k, 0.5%, 0.1 W, 0603	0603S	RT0603DRE0740K2L	Yageo America	DNL
RL1, RL6	2	402	RES, 402, 0.1%, 0.1 W, 0603	0603S	RT0603BRD07402RL	Yageo America	DNL
RM1	1	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale	DNL
RZ3	1	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale	DNL

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (September 2022)	Page
• Updated document title	1
• Updated *Schematic* section	6
• Updated *PCB Drawings* section	21
• Updated TPS25985EVM Bill of Materials table	23

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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