

# SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276 – DECEMBER 1994

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

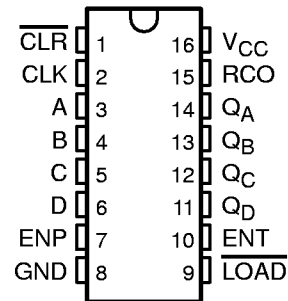
These synchronous, presettable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The ALS161B, ALS163B, AS161, and AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they may be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

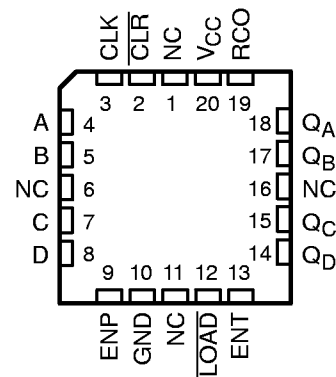
The clear function for the ALS161B and AS161 is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK,  $\overline{\text{LOAD}}$ , or enable inputs. The clear function for the SN54ALS162B, ALS163B, and AS163 is synchronous, and a low level at  $\overline{\text{CLR}}$  sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to  $\overline{\text{CLR}}$  to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161,  
SN54AS163 . . . J PACKAGE  
SN74ALS161B, SN74ALS163B, SN74AS161,  
SN74AS163 . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161,  
SN54AS163 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

# SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

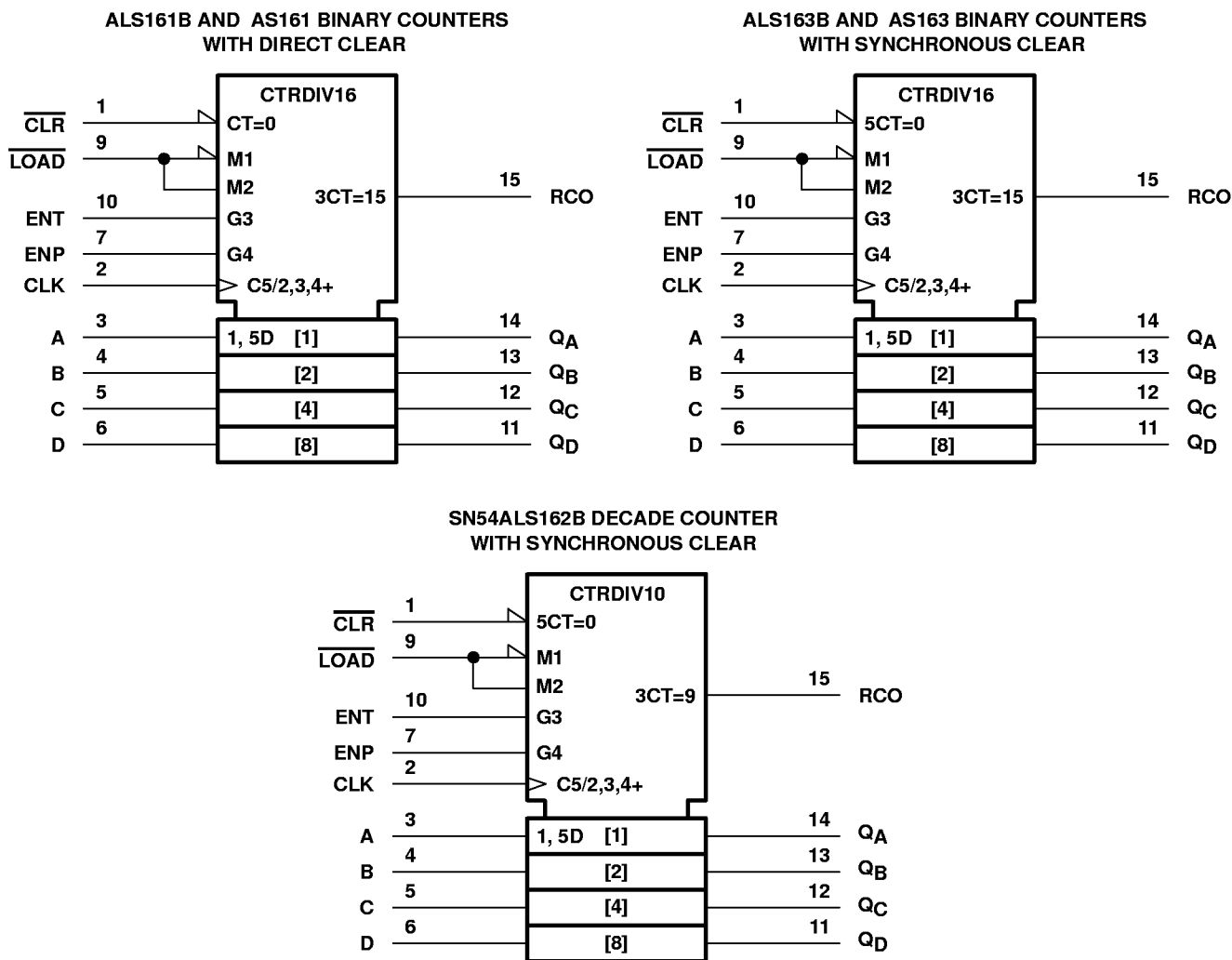
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## description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## logic symbol†

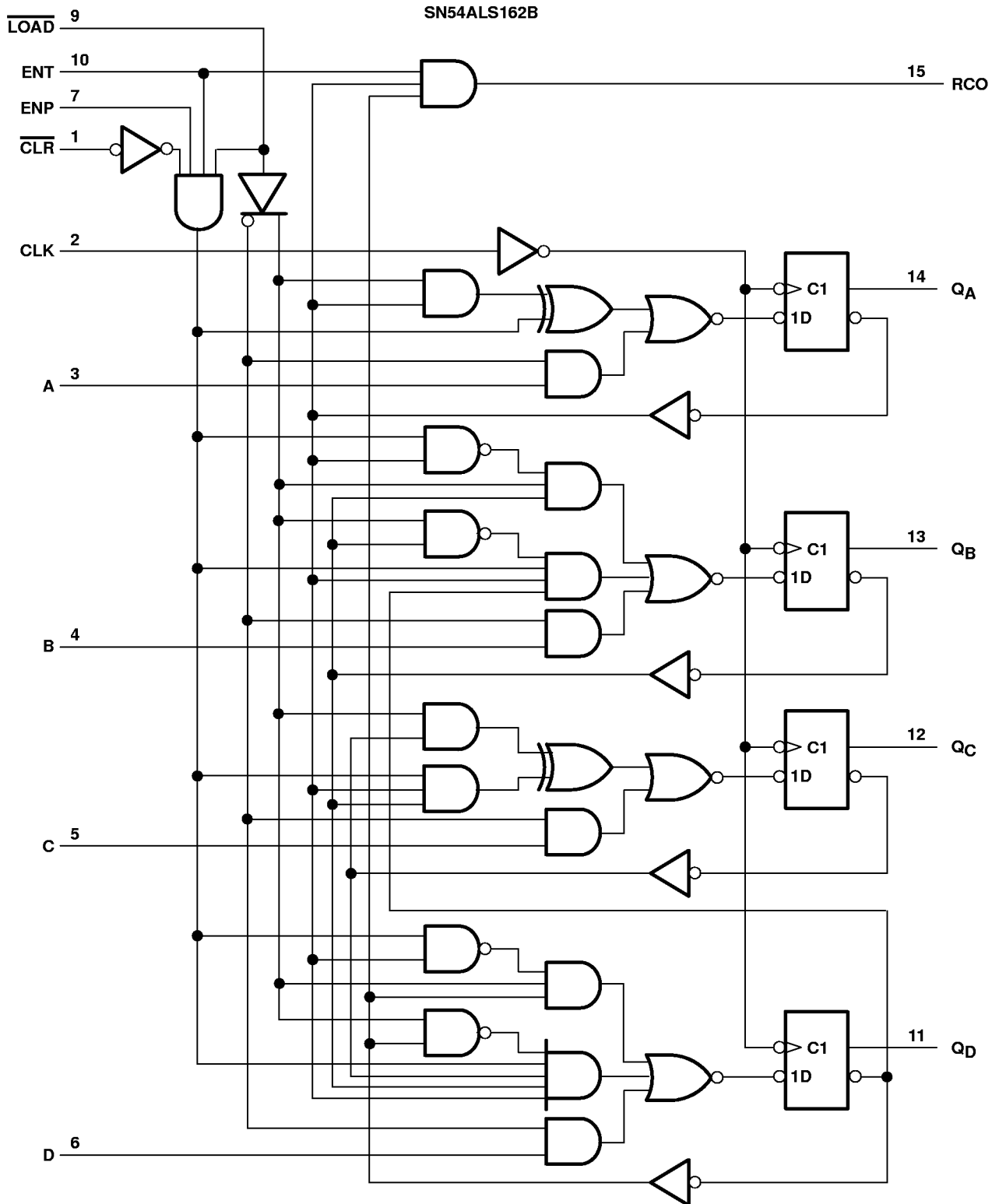


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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logic diagram (positive logic)



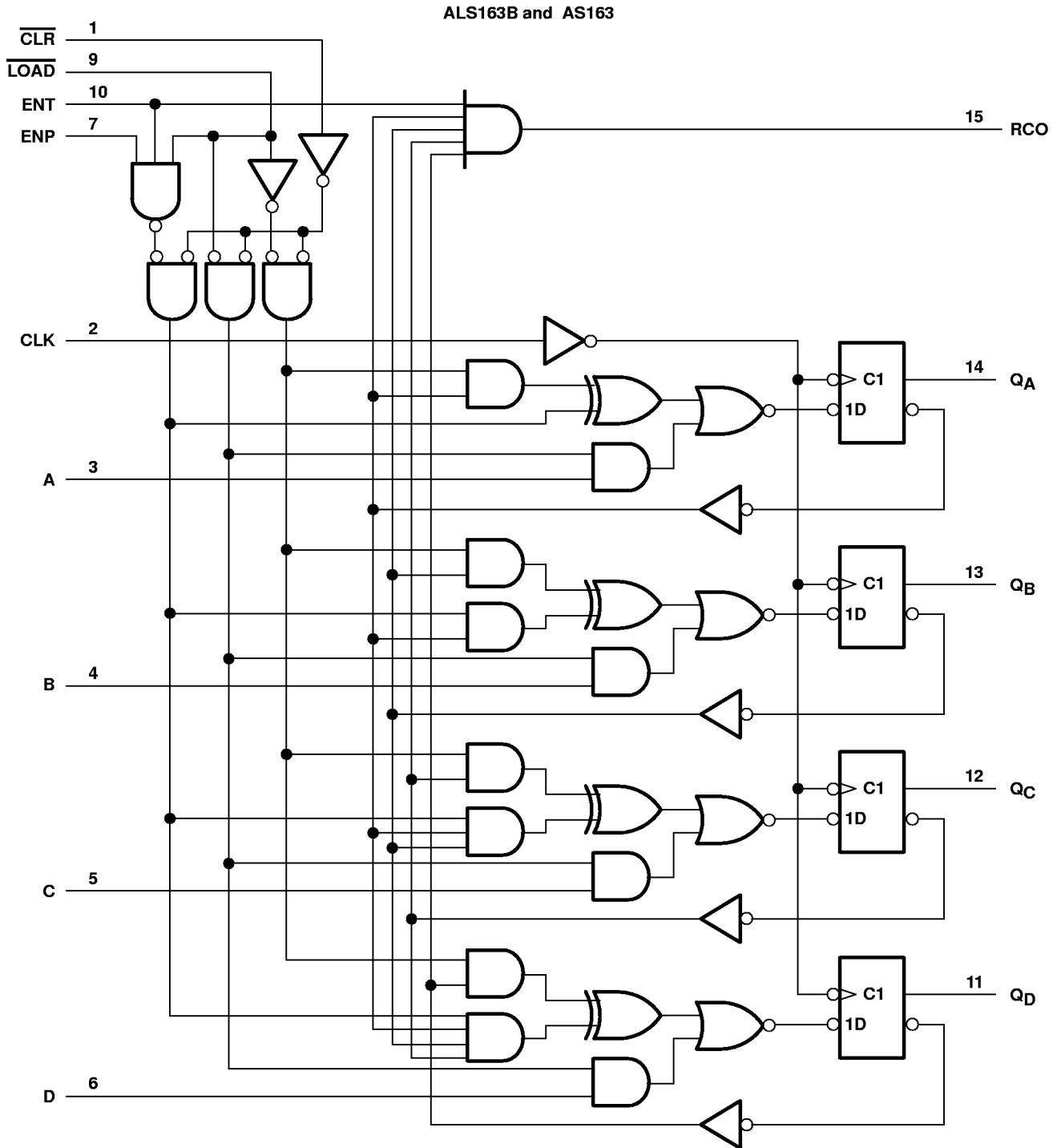
Pin numbers shown are for the J package.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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**logic diagram (positive logic)**



Pin numbers shown are for the D, J, and N packages.

ALS161B and AS161 synchronous binary counters are similar; however,  $\overline{\text{CLR}}$  is asynchronous.



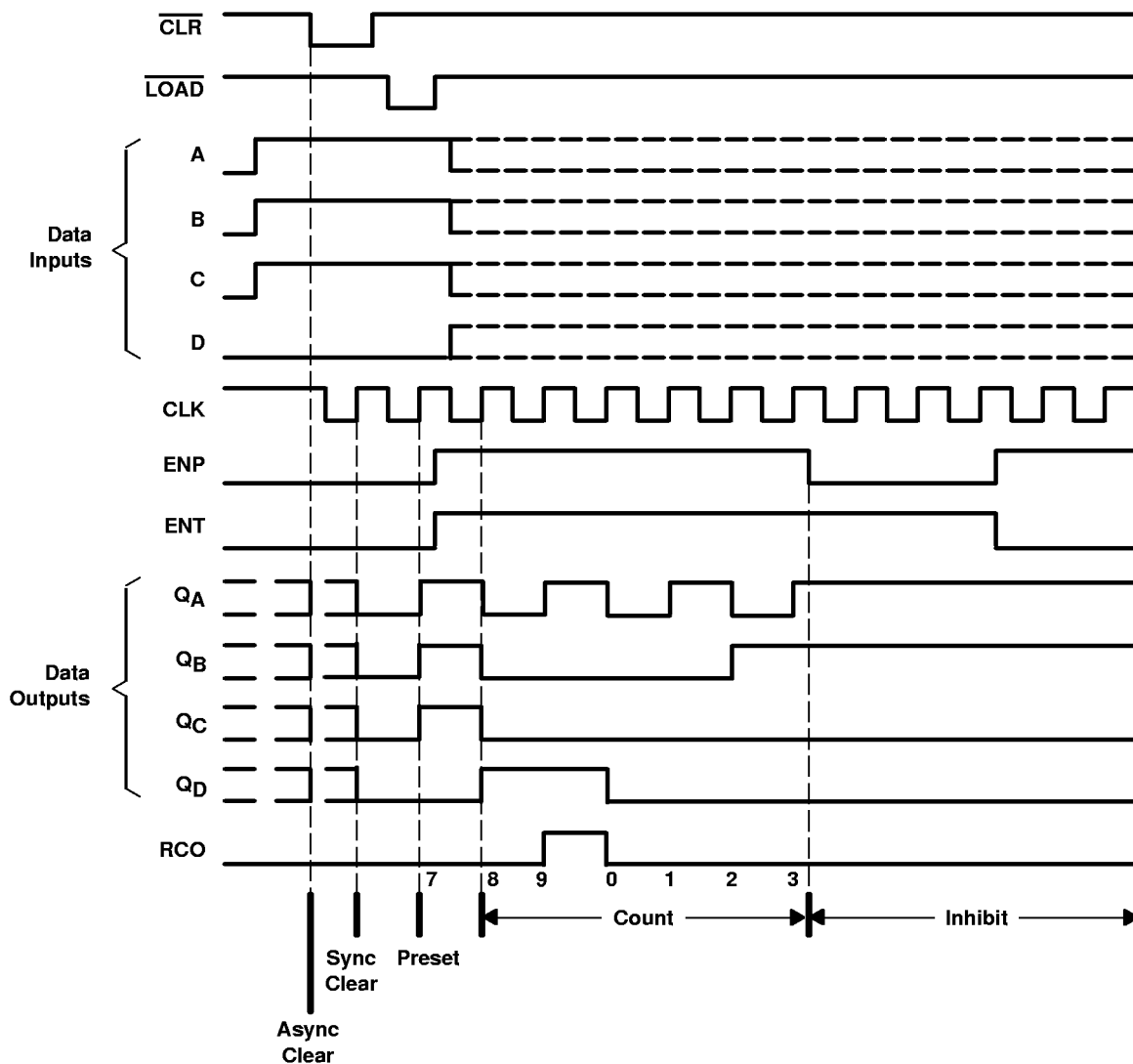
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typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

1. Clear outputs to zero (SN54ALS162B is synchronous)
2. Preset to BCD 7
3. Count to 8, 9, 0, 1, 2, and 3
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

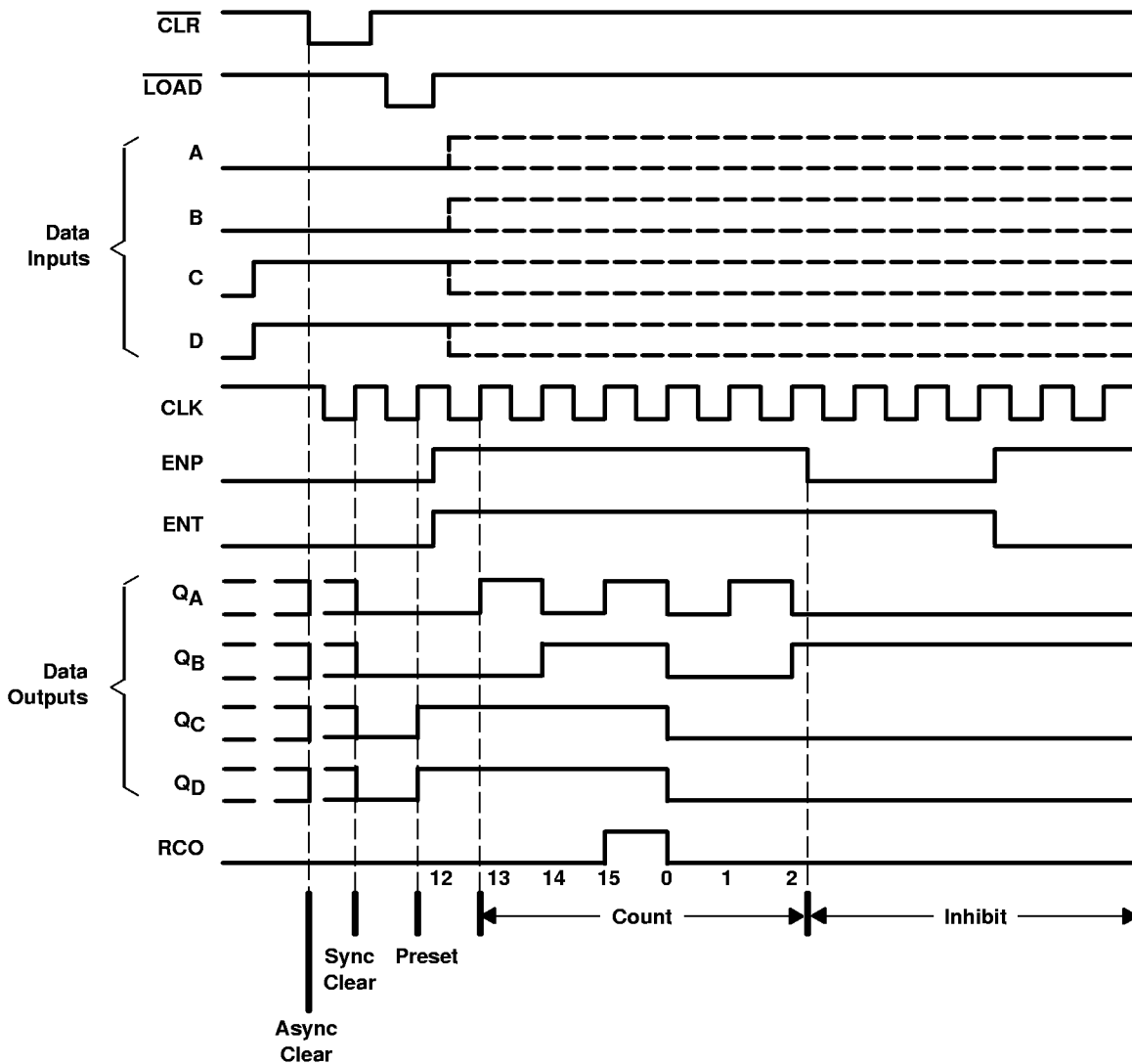
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**typical clear, preset, count, and inhibit sequences**

ALS161B, AS161, ALS163B, and AS163

The following sequence is illustrated below:

1. Clear outputs to zero ( ALS161B and AS161 are asynchronous; ALS163B and AS163 are synchronous.)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Operating free-air temperature range, $T_A$ : SN54ALS161B, SN54ALS162B, SN54ALS163B .....	–55°C to 125°C
SN74ALS161B, SN74ALS163B .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–0.4			–0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		22	0		40	MHz
$t_w$	Pulse duration	$\overline{CLR}$ high or low		20		12.5		ns
		ALS161B	$\overline{CLR}$ low	20		15		
$t_{su}$	Setup time before CLK↑	A, B, C, D		50		15		ns
		$\overline{LOAD}$		20		15		
		ALS161B	ENP, ENT	25		15		
		SN54ALS162B, ALS163B		20		15		
		ALS161B	$\overline{CLR}$ inactive	10		10		
		SN54ALS162B, ALS163B	$\overline{CLR}$ low	20		15		
$\overline{CLR}$ high	20			10				
$t_h$	Hold time, all synchronous inputs after CLK↑	0			0			ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25 0.4			0.25 0.4			V
		$I_{OL} = 8\text{ mA}$				0.35 0.5			
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$				0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$				20			$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$				-0.2			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-20		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$			12	21		12	21	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS161B		SN74ALS161B		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			22		40		MHz
$t_{PLH}$	CLK	RCO	5	34	5	20	ns
$t_{PHL}$			5	27	5	20	
$t_{PLH}$	CLK	Any Q	4	19	4	15	ns
$t_{PHL}$			6	25	6	20	
$t_{PLH}$	ENT	RCO	3	18	3	13	ns
$t_{PHL}$			3	17	3	13	
$t_{PHL}$	$\overline{\text{CLR}}$	Any Q	8	27	8	24	ns
		RCO	11	32	11	23	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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**switching characteristics (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS162B SN54ALS163B		SN74ALS163B		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			35		40		MHz
t <sub>PLH</sub>	CLK	RCO	5	25	5	20	ns
t <sub>PHL</sub>			5	25	5	20	
t <sub>PLH</sub>	CLK	Any Q	4	18	4	15	ns
t <sub>PHL</sub>			6	25	6	20	
t <sub>PLH</sub>	ENT	RCO	3	16	3	13	ns
t <sub>PHL</sub>			3	16	3	13	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Operating free-air temperature range, T <sub>A</sub> : SN54AS161, SN54AS163	-55°C to 125°C
SN74AS161, SN74AS163	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-2			-2	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
f <sub>clock</sub> *	Clock frequency	0		65	0		75	MHz
t <sub>w</sub> *	Pulse duration	CLR high or low		7.7	6.7		ns	
		AS161	CLR low	10	8			
t <sub>su</sub> *	Setup time before CLK↑	A, B, C, D		10	8		ns	
		LOAD		10	8			
		ENP, ENT		10	8			
		AS161	CLR inactive	10	8			
		AS163	CLR low	14	12			
AS163	CLR high (inactive)	10	9					
t <sub>h</sub> *	Hold time, all synchronous inputs after CLK↑	2			0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS161 SN54AS163		SN74AS161 SN74AS163		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 2		V <sub>CC</sub> - 2			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA	0.25	0.5	0.25	0.5		V
I <sub>I</sub>	LOAD			0.3	0.3		mA
	ENT	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.2	0.2		
	All others			0.1	0.1		
I <sub>IH</sub>	LOAD			60	60		μA
	ENT	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		40	40		
	All others			20	20		
I <sub>IL</sub>	LOAD			-1.5	-1.5		mA
	ENT	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-1	-1		
	All others			-0.5	-0.5		
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30	-112	-30	-112		mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	35	53	35	53		mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

**switching characteristics (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54AS161		SN74AS161		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			65		75	MHz	
t <sub>PLH</sub>	CLK	RCO (with LOAD high)	1	8.5	1	8	ns
		RCO (with LOAD low)	3	17.5	3	16.5	
t <sub>PHL</sub>		RCO	2	14	2	12.5	
t <sub>PLH</sub>	CLK	Any Q	1	7.5	1	7	ns
t <sub>PHL</sub>			2	14	2	13	
t <sub>PLH</sub>	ENT	RCO	1.5	10	1.5	9	ns
t <sub>PHL</sub>			1	9.5	1	8.5	
t <sub>PHL</sub>	CLR	Any Q	2	14	2	13	ns
		RCO	2	14	2	12.5	

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
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SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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**switching characteristics (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS163		SN74AS163		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			65		75		MHz
t <sub>PLH</sub>	CLK	RCO (with $\overline{\text{LOAD}}$ high)	1	8.5	1	8	ns
		RCO (with $\overline{\text{LOAD}}$ low)	3	17.5	3	16.5	
t <sub>PHL</sub>		RCO	2	14	2	12.5	
t <sub>PLH</sub>	CLK	Any Q	1	7.5	1	7	ns
t <sub>PHL</sub>			2	14	2	13	
t <sub>PLH</sub>	ENT	RCO	1.5	10	1.5	9	ns
t <sub>PHL</sub>			1	9.5	1	8.5	

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



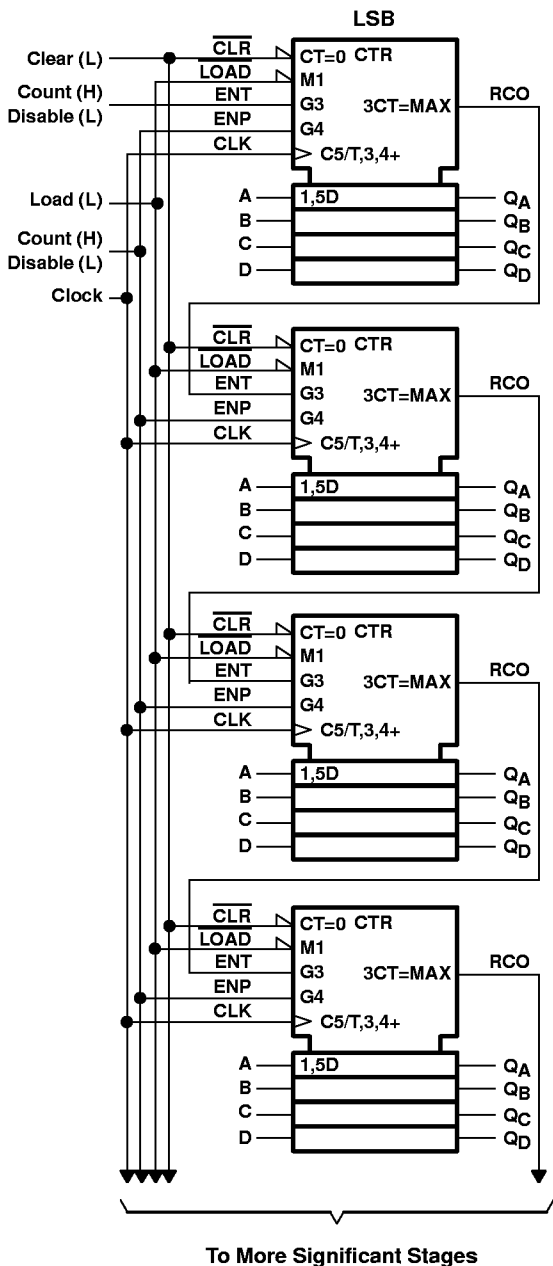
# SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

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## APPLICATION INFORMATION

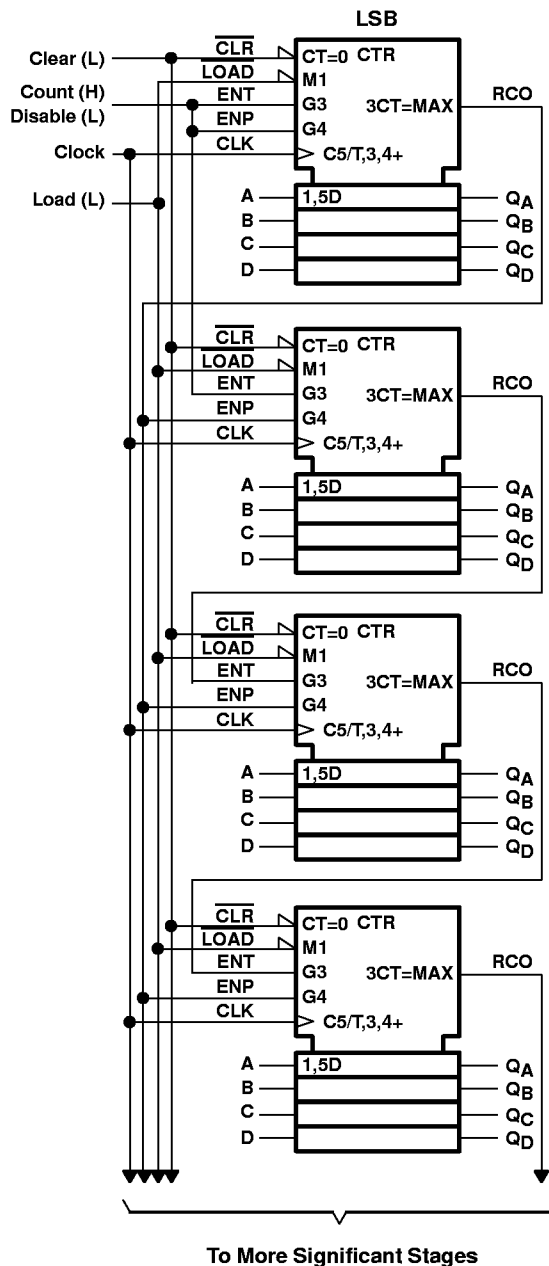
### n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 1) and the carry-look-ahead circuit (see Figure 2) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The ALS161B, AS161, ALS163B, and AS163 count in binary. When additional stages are added, the  $f_{max}$  decreases in Figure 1, but remains unchanged in Figure 2.



$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH}) (N - 2) + (\text{ENT } t_{su})$$

Figure 1. Ripple-Mode Carry Circuit

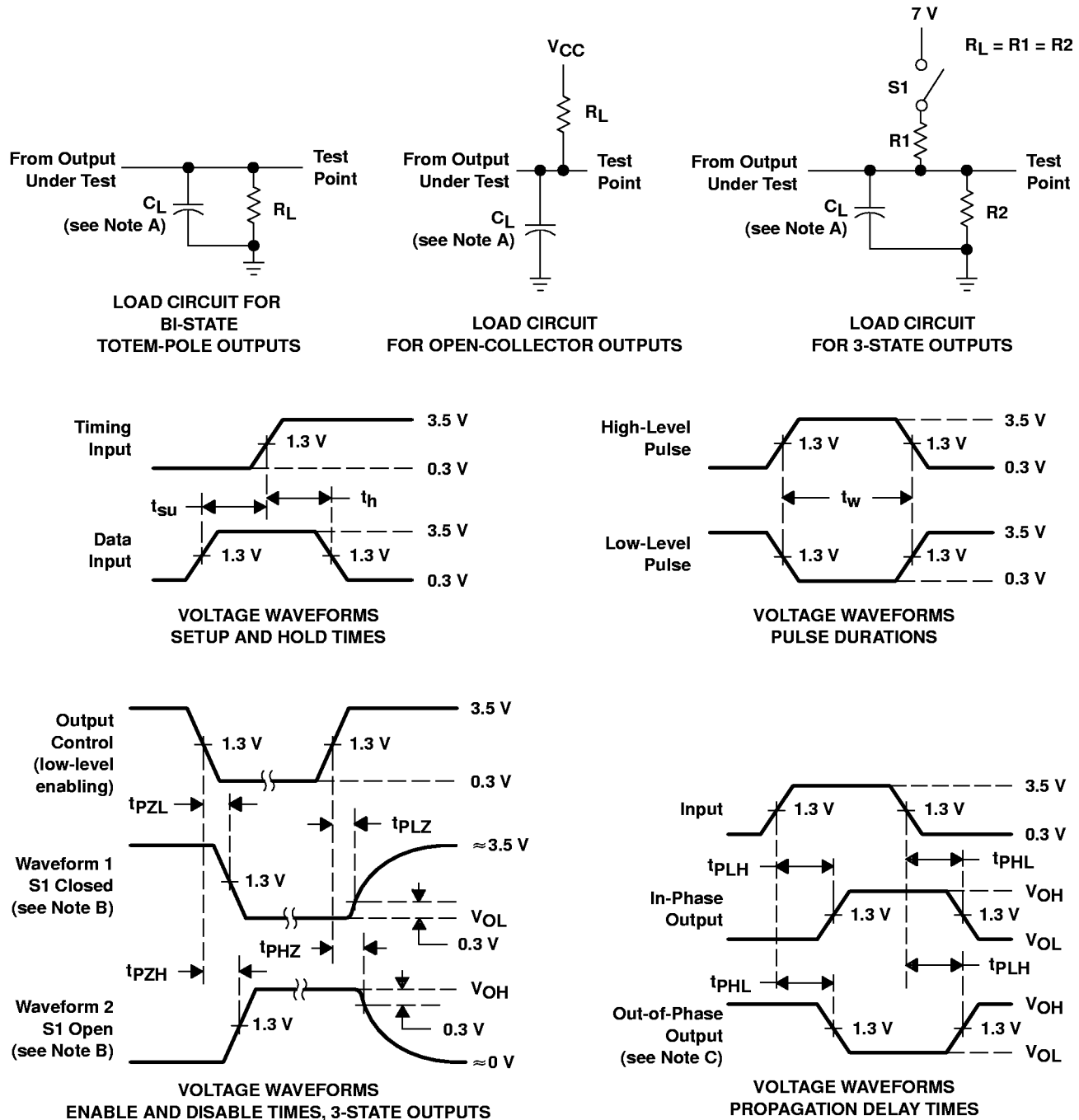


$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENP } t_{su})$$

Figure 2. Carry-Look-Ahead Circuit



PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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