

# Octal Line Receiver

## FEATURES

- Meets EIA 232E/423A/422A and CCITT V.10,V.11, V.28, X.26, X.27
- Single +5V Supply--TTL Compatible Outputs
- Differential Inputs Withstand  $\pm 25V$
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current--35 mA Max
- Input Noise Filter
- Internal Hysteresis

## DESCRIPTION

The UC5180C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA423A, EIA422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180C includes an input noise filter and is intended for applications employing data rates up to 200 KBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

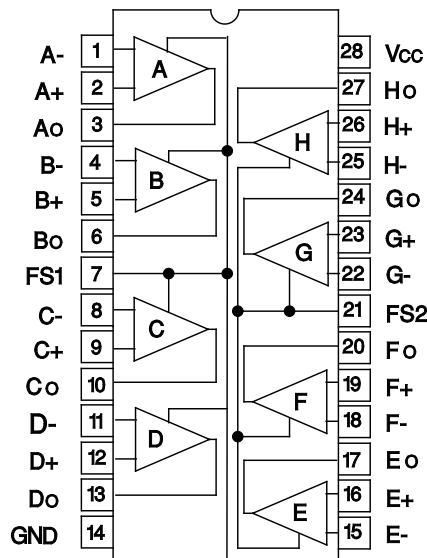
Supply Voltage, Vcc	7V
Output Sink Current	50 mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to Vcc
PLCC Power Dissipation, TA = 25°C (Note 2)	1000 mW
DIP Power Dissipation, TA = 25°C (Note 2)	1200 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	-300°C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive into, negative out of the specified terminal

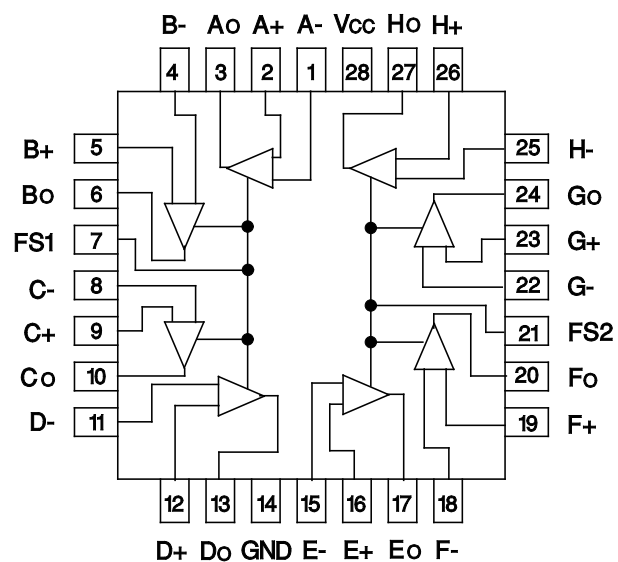
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

## CONNECTION DIAGRAMS

**DIL-28 (TOP VIEW)**



**PLCC-28 (TOP VIEW)**



**DC ELECTRICAL CHARACTERISTICS:** Unless otherwise stated these specifications apply for  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ , Input Common Mode Range  $\pm 7V$ ,  $T_A = T_J$

PARAMETERS	SYMBOL	TEST CONDITIONS	UC5180C		UNITS	
			MIN	MAX		
DC Input Resistance	$R_{IN}$	$3V \leq  V_{IN}  \leq 25V$	3	7	$k\Omega$	
Failsafe Output Voltage	$V_{OFS}$	Inputs Open or Shorted Together, or One Input Open and One Grounded	$0 \leq I_{OUT} \leq 8mA$ , $V_{FAILSAFE} = 0V$		0.45	V
			$0 \geq I_{OUT} \geq -400\mu A$ , $V_{FAILSAFE} = V_{CC}$	2.7		
Differential Input High Threshold	$V_{TH}$	$V_{OUT} = 2.7V$ , $I_{OUT} = 440\mu A$ (See Figure 1)	$R_s = 0$ (Note 2)	50	200	mV
			$R_s = 500$ (Note 2)		400	
Differential Input Low Threshold	$V_{TL}$	$V_{OUT} = 0.45V$ , $I_{OUT} = 440\mu A$ (See Figure 1)	$R_s = 0$ (Note 2)	-200	-50	mV
			$R_s = 500$ (Note 2)	-400		
Hysteresis	$V_H$	$F_s = 0V$ or $V_{CC}$ (See Figure 1)	50	140	mV	
Open Circuit Input Voltage	$V_{ICC}$			75	mV	
Input Capacitance	$C_i$			20	pF	
High Level Output Voltage	$V_{CH}$	$V_{ID} = 1V$ , $I_{OUT} = -440\mu A$	2.7		V	
Low Level Output Voltage	$V_{OL}$	$V_{ID} = -1V$ (Note 3)	$I_{OUT} = 4mA$		0.4	V
			$I_{OUT} = 8mA$		0.45	
Short Circuit Output Current	$I_{OS}$	Note 4	20	100	mA	
Supply Current	$I_{CC}$	$4.75V \leq V_{CC} \leq 5.25V$		35	mA	
Input Current	$I_{IN}$	Other Inputs Grounded	$V_{IN} = +10V$		3.25	mA
			$V_{IN} = -10V$	-3.25		

Note 2:  $R_s$  is a resistor in series with each input.

Note 3: Measured after 100ms warm up (at  $0^\circ\text{C}$ )

Note 4: Only 1 output may be shorted at one time and then only for a maximum of 1 sec.

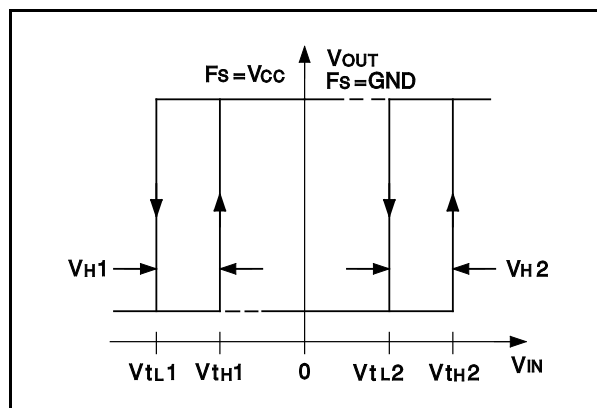


Figure 1.  $V_{tL}$ ,  $V_{tH}$ ,  $V_H$  Definition

**AC ELECTRICAL CHARACTERISTICS:**  $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , Figure 2,  $T_A = T_J$ .

PARAMETERS	SYMBOL	TEST CONDITIONS	UC5180C		UNITS
			MIN	MAX	
Propagation Delay - Low to High	$t_{PLH}$	$C_L = 50pF$ , $V_{IN} = \pm 500mV$		550	ns
Propagation Delay - High to Low	$t_{PHL}$	$C_L = 50pF$ , $V_{IN} = \pm 500mV$		550	ns
Acceptance Input Frequency	$f_A$	Unused Input Grounded, $V_{IN} = \pm 200mV$		0.1	MHz
Rejectable Input Frequency	$f_R$	Unused Input Grounded, $V_{IN} = \pm 500mV$	5.5		MHz

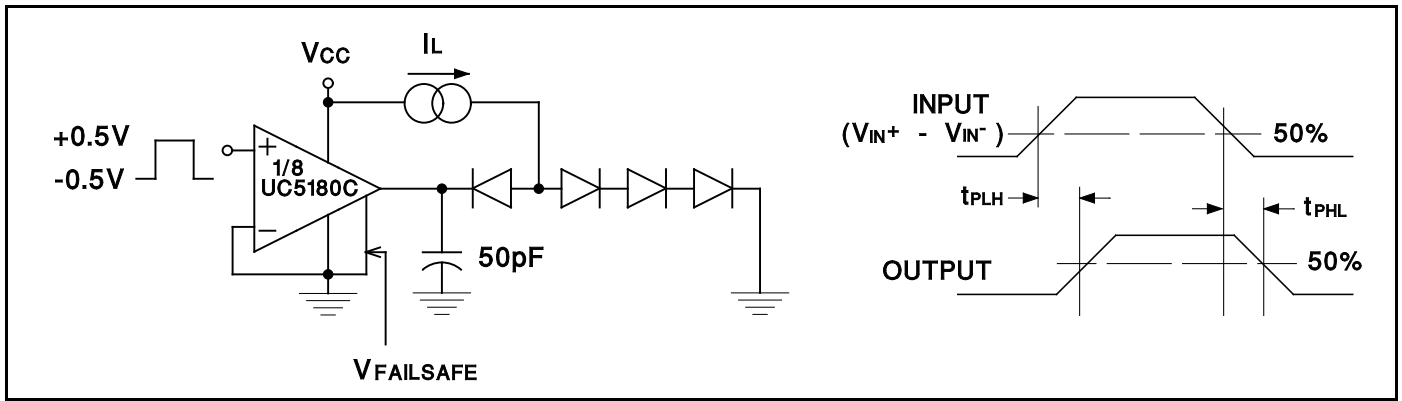


Figure 2. AC Test Circuit

**APPLICATIONS INFORMATION**

**Failsafe Operation**

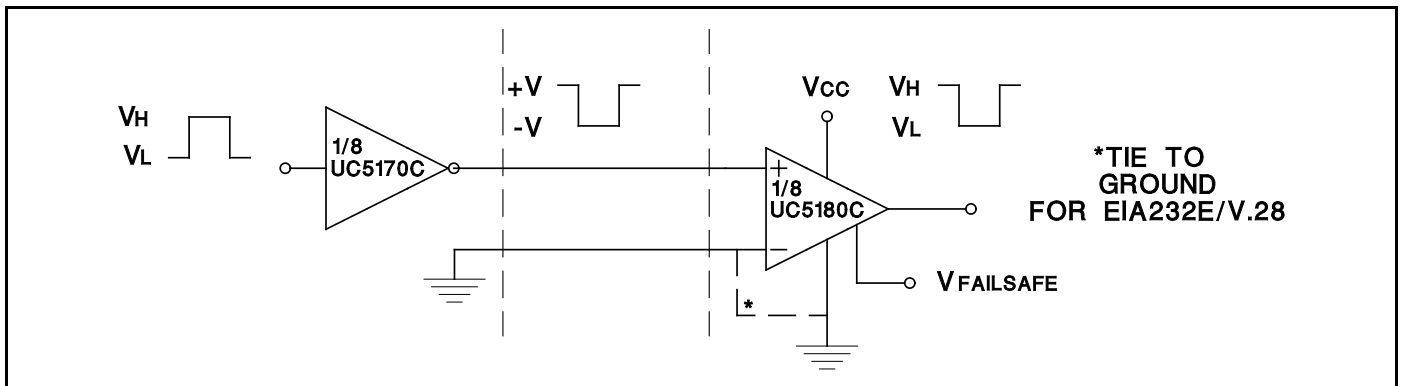
These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) drive in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to Vcc or ground. A connection to Vcc provides a logic "1" output

under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (Fs1 and Fs2) on the UC5180C where each provides common failsafe control for four receivers.

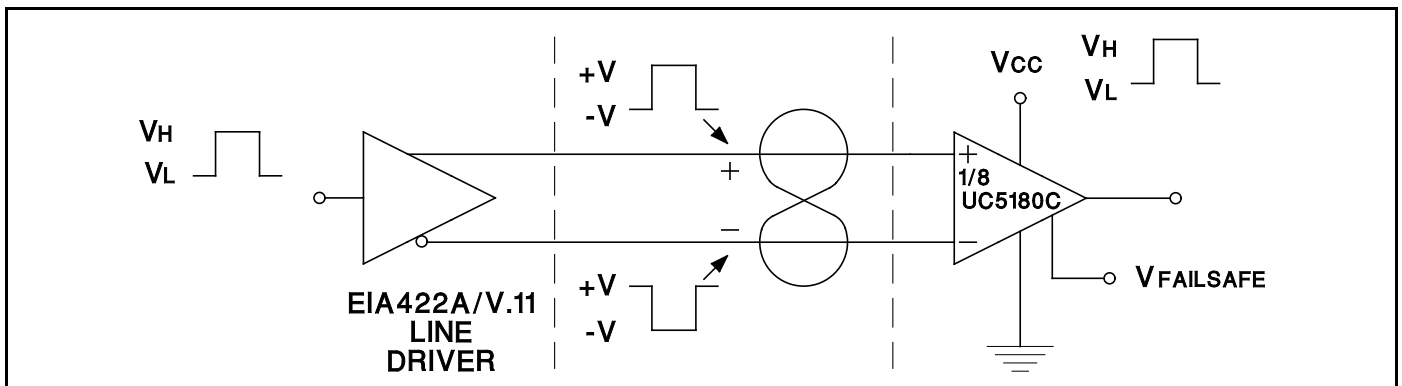
**Input Filtering (UC5180C)**

The UC5180C has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output.

**EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION**



**EIA422A/V.11 DATA TRANSMISSION**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC5180CJ	OBSOLETE		UTR			TBD	Call TI	Call TI			
UC5180CQ	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI		UC5180CQ	
UC5180CQTR	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI		UC5180CQ	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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