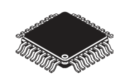
2.5 V and 3.3 V LVCMOS Clock Fanout Buffer

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016

The MPC9456 is a 2.5 V and 3.3 V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3 V, 2.5 V and dual supply voltages are supported for mixed-voltage applications. The MPC9456 offers 10 low-skew outputs and a differential LVPECL clock input. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9456 is specified for the extended temperature range of –40 to 85°C.

MPC9456

LOW VOLTAGE SINGLE OR DUAL SUPPLY 2.5 V AND 3.3 V LVCMOS CLOCK DISTRIBUTION BUFFER



AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3 V/2.5 V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports high-performance differential clocking applications
- Maximum output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32-lead LQFP package, Pb-free
- Ambient operating temperature range of –40 to 85°C
- For functional replacement use 87946AYI-147

Functional Description

The MPC9456 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks.

Each of the three output banks can be individually supplied by 2.5 V or 3.3 V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9456 can be reset and the outputs are disabled by deasserting the MR/$\overline{OE}$ pin (logic high state). Asserting MR/$\overline{OE}$ will enable the outputs.

All control inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. The clock input is low voltage PECL compatible for differential clock distribution support. Please consult the MPC9446 specification for a full CMOS compatible device. For series terminated transmission lines, each of the MPC9456 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7×7 mm^2 32-lead LQFP package.

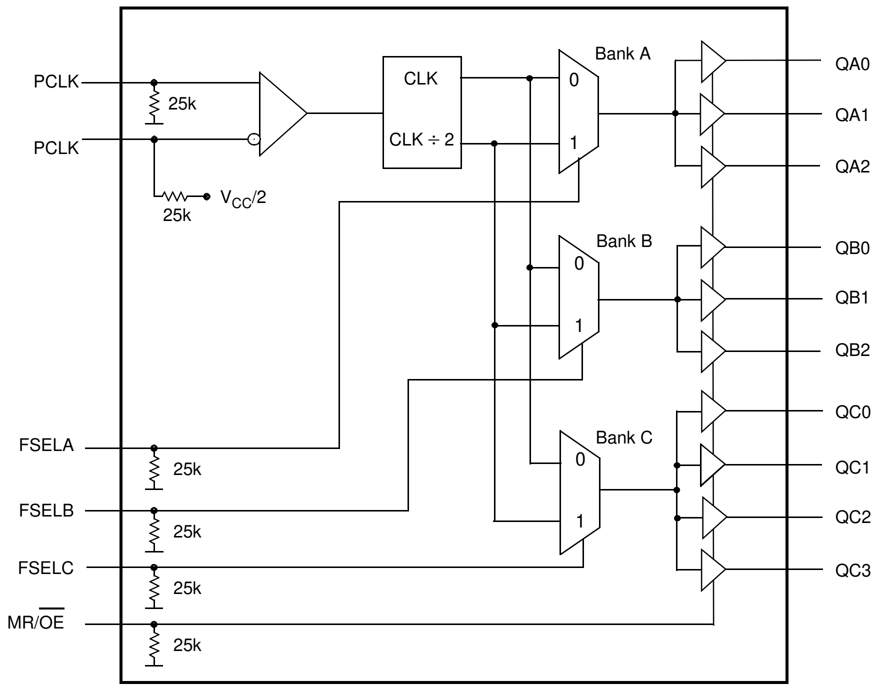
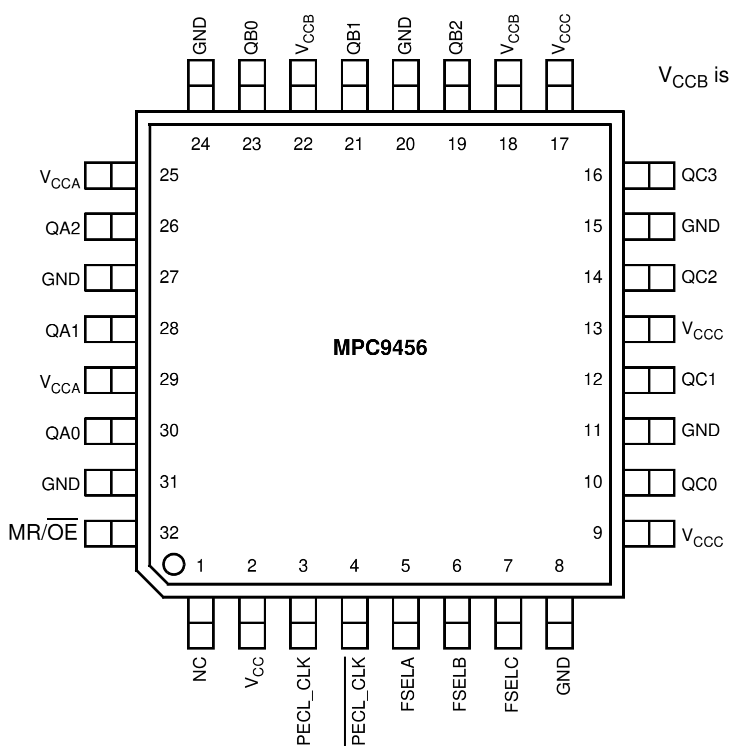


Figure 1. MPC9456 Logic Diagram



V_{CCB} is internally connected to V_{CC}

Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
PECL_CLK, $\overline{\text{PECL\_CLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
$FSEL_A$, $FSEL_B$, $FSEL_C$	Input	LVCMOS	Output bank divide select input
MR/$\overline{OE}$	Input	LVCMOS	Internal reset and output tristate control
GND		Supply	Negative voltage supply output bank (GND)
V_{CCA}, V_{CCB}(1), V_{CCC}		Supply	Positive voltage supply for output banks
V_{CC}		Supply	Positive voltage supply core (VCC)
QA0 – QA2	Output	LVCMOS	Bank A outputs
QB0 – QB2	Output	LVCMOS	Bank B outputs
QC0 – QC3	Output	LVCMOS	Bank C outputs

1. V_{CCB} is internally connected to V_{CC}.

Table 2. Supported Single and Dual Supply Configurations

Supply Voltage Configuration	V_{CC}(1)	V_{CCA}(2)	V_{CCB}(3)	V_{CCC}(4)	GND
3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
Mixed Voltage Supply	3.3 V	3.3 V or 2.5 V	3.3 V	3.3 V or 2.5 V	0 V
2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

1. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.
2. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels.
3. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC}.
4. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels.

Table 3. Function Table (Controls)

Control	Default	0	1
FSELA	0	$f_{QA0:2} = f_{REF}$	$f_{QA0:2} = f_{REF} \div 2$
FSELB	0	$f_{QB0:2} = f_{REF}$	$f_{QB0:2} = f_{REF} \div 2$
FSELC	0	$f_{QC0:3} = f_{REF}$	$f_{QC0:3} = f_{REF} \div 2$
MR/$\overline{OE}$	0	Outputs enabled	Internal reset Outputs disabled (tristate)

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	−0.3	4.6	V	
V_{IN}	DC Input Voltage	−0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	−0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	−65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	

Table 6. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 3.3 V ± 5%, T_A = –40 to + 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.1		V_{CC}–0.6	V	LVPECL
I_{IN}	Input Current[2]				200	µA	V_{IN} = GND or $V_{IN} = V_{CC}$
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[3]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA[2] I_{OL} = 12 mA
Z_{OUT}	Output Impedance			14–17		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9456 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7. AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 3.3 V ± 5%, T_A = –40 to + 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250[2]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		250[2] 125	MHz MHz	FSELx = 0 FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK	1.3		V_{CC}–0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time				1.0[4]	ns	0.8 to 2.0 V
t_{PLH} t_{PHL}	Propagation Delay	CCLK to any Q CCLK to any Q	2.2 2.2	2.8 2.8	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.25	ns	
$t_{SK(P)}$	Output Pulse Skew[5]				200	ps	
DC_Q	Output Duty Cycle	÷1 output ÷2 output	47 45	50 50	53 55	% %	DC_{REF} = 50% DC_{REF} = 25%–75%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
4. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
5. Output pulse skew $t_{SK(P)}$ is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{SK(P)} \cdot f_{OUT})$. For example at f_{OUT} = 125 MHz the output duty cycle limit is 50% ± 2.5%.

Table 8. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 2.5 V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		1.7		V_{CC}+0.3	V	LVCMOS
V_{IL}	Input low voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.1		V_{CC}–0.7	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output impedance			17–20[2]		Ω	
I_{IN}	Input current[3]				±200	μA	V_{IN} = GND or V_{IN} = V_{CC}
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9456 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.
3. Input pull-up / pull-down resistors influence input current.
4. CCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9. AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 2.5 V ± 5%, T_A = –40 to +85°C)(1)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250(2)	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		250(2) 125	MHz MHz	FSELx = 0 FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK	500		1000	mV	LVPECL
V_{CMR}(3)	Common Mode Range	PCLK	1.1		V_{CC}–0.7	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time				1.0(4)	ns	0.7 to 1.7 V
t_{PLH} t_{PHL}	Propagation Delay	PCLK to any Q PCLK to any Q	2.6 2.6		5.6 5.5	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				3.0	ns	
$t_{SK(P)}$	Output Pulse Skew(5)				200	ps	
DC_Q	Output Duty Cycle	÷1 or ÷2 output	45	50	55	%	DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
4. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
5. Output pulse skew $t_{SK(P)}$ is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{SK(P)} \cdot f_{OUT})$. For example at f_{OUT} = 125 MHz the output duty cycle limit is 50% ± 2.5%.

Table 10. AC Characteristics (V_{CC} = 3.3 V ± 5%, $V_{CCA} = V_{CCB} = V_{CCC}$ = 2.5 V ± 5% or 3.3 V ± 5%, T_A = –40 to +85°C)(1), (2)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 250 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.5	ns	
$t_{PLH,HL}$	Propagation Delay	PCLK to any Q	See 3.3 V Table				
$t_{SK(P)}$	Output Pulse Skew(3)				250	ps	
DC_Q	Output Duty Cycle	÷1 or ÷2 output	45	50	55	%	DC_{REF} = 50%

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. For all other AC specifications, refer to 2.5 V or 3.3 V tables according to the supply voltage of the output bank.
3. Output pulse skew $t_{SK(P)}$ is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$. Output duty cycle is frequency dependent: $DC_Q = (0.5 \pm t_{SK(P)} \cdot f_{OUT})$.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9456 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}÷2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9456 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9456 clock driver is effectively doubled due to its capability to drive multiple lines.

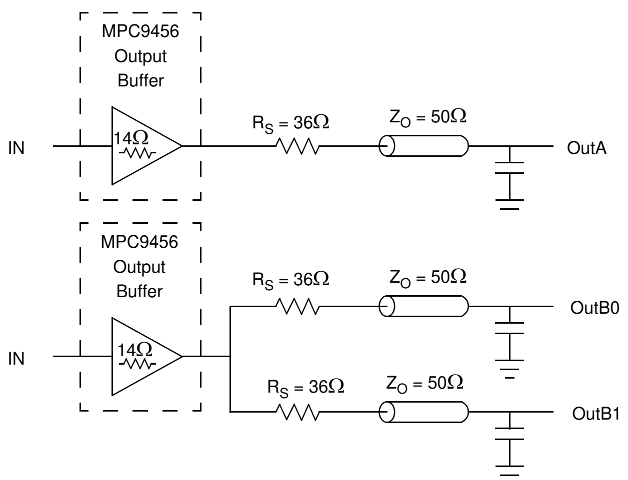


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9456 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9456. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 14 + 25)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

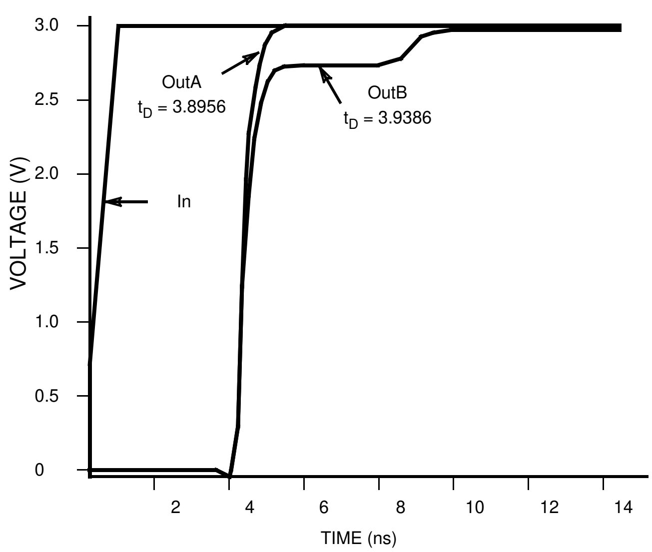


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

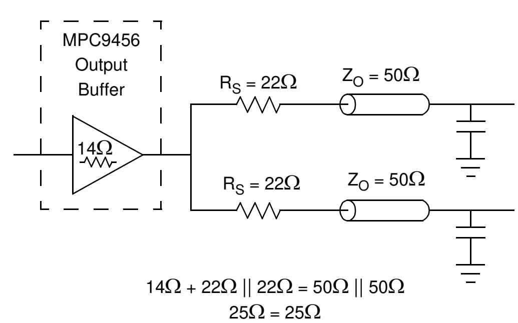


Figure 5. Optimized Dual Line Termination

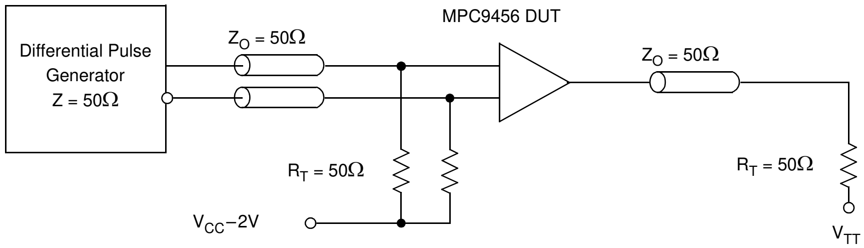


Figure 6. PCLK MPC9456 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

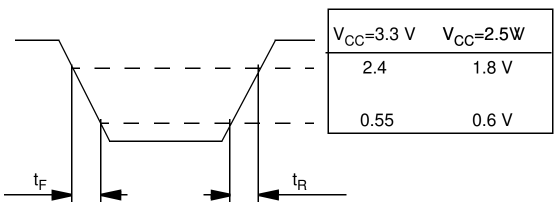


Figure 7. Output Transition Time Test Reference

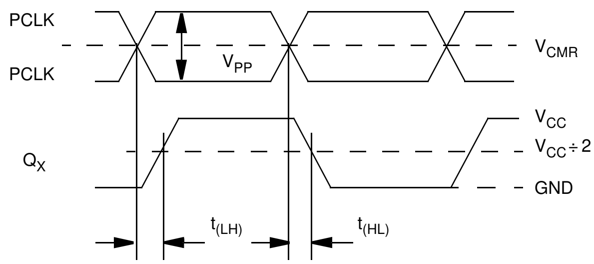
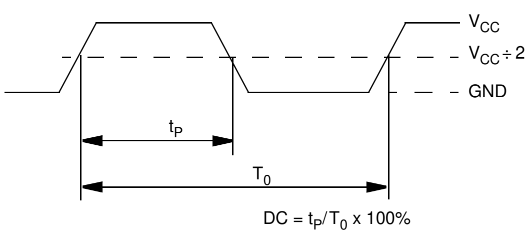
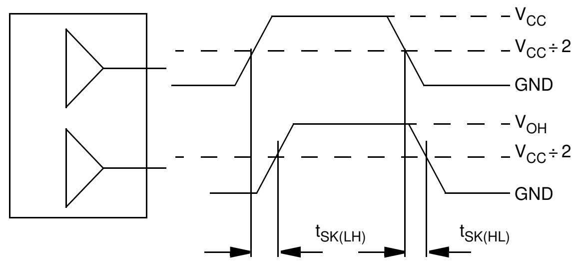


Figure 8. Propagation Delay (t_{PD}) Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

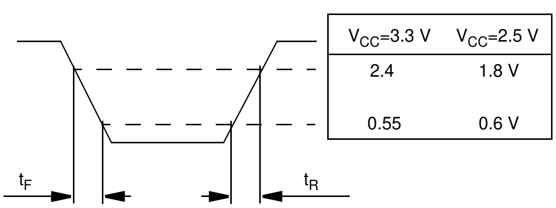
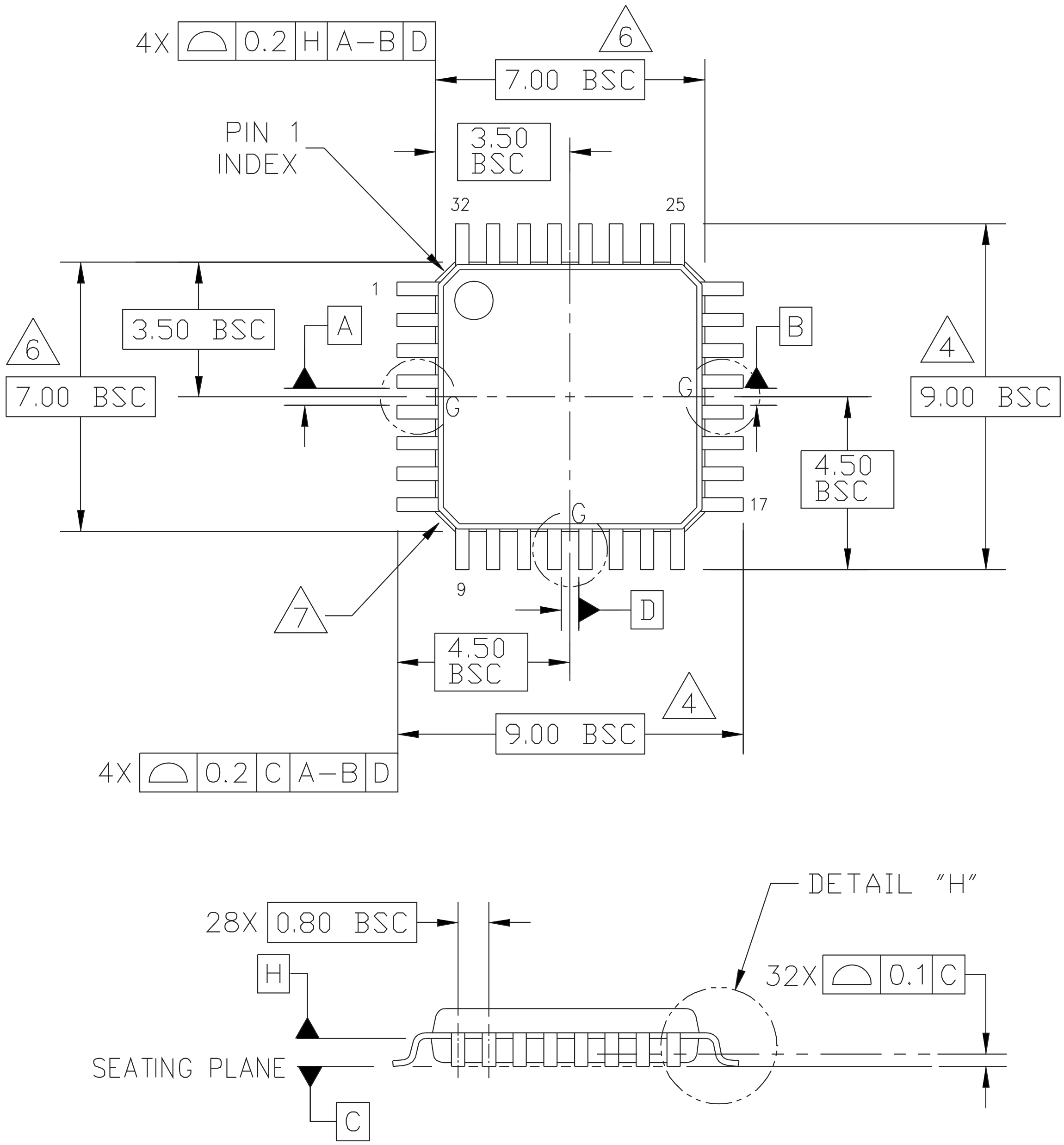


Figure 11. Output Transition Time Test Reference

PACKAGE DIMENSIONS

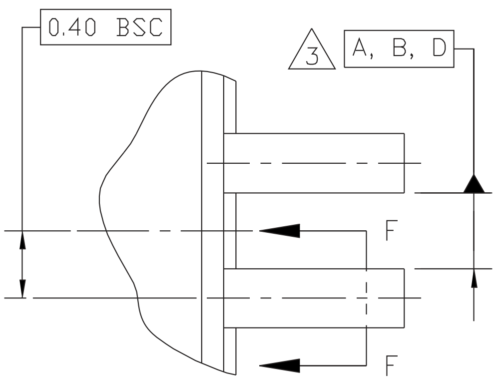


© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A		REV: C
	CASE NUMBER: 873A-04		01 APR 2005
	STANDARD: JEDEC MS-026 BBA		

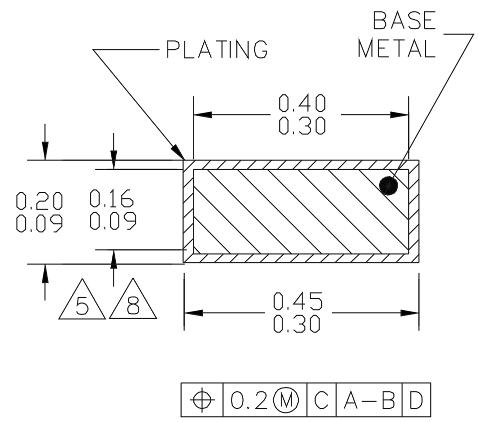
PAGE 1 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

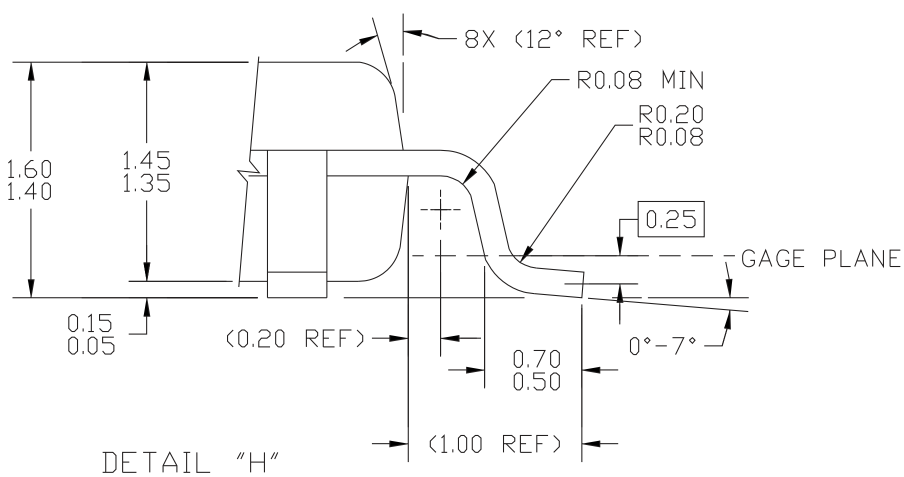
PACKAGE DIMENSIONS



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

PAGE 2 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C	
	CASE NUMBER: 873A-04	01 APR 2005	
	STANDARD: JEDEC MS-026 BBA		

PAGE 3 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
4		1	NRND – Not Recommend for New Designs	12/21/12
4		1	Removed NRND	5/5/15
4		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02	3/15/16

IMPORTANT NOTICE AND DISCLAIMER

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks