

ADS58C48EVM

This is the user's guide for the ADS58C48 EVM. The ADS58C48 is a quad 11-bit, 200 MSPS analog-to-digital converter with optional SNR boost capabilities for improving SNR within a specified bandwidth.

The schematic, BOM, and layout files can be found in the design package in the ADS58C48 EVM product folder on www.ti.com.

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1 Software Control

The ADS58C48 has many functions controlled by internal registers. The internal registers can be accessed through the device's serial port interface and written with individual code or sequence by the PC program, ADS58C48_GUI_vxpx, through on-board USB.

1.1 Installation Instructions

The control software ADS58C48_GUI_vxpx can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers to communicate to the USB port on the EVM. After the software is installed, insert the USB cable into the EVM. The PC will automatically detect the new hardware and initialize the Found New Hardware Wizard and test Windows Logo to finish the USB driver installation, shown in Figure 1 and Figure 2. The installation steps are summarized as following:

1. Open folder named ADS58C48_Installer_vxpx (xpx represents the latest version)
2. Run Setup.exe under the folder Volume and follow the on-screen instructions

At first Window displays “ADS58C48 Installer” shown box, then click “next” → on new page, select “I accept” → on new page, click “next” → on new page, click “next” → on new page, PC display “The installer has finished updating your system”, then click “next” → on new page, PC display “...has not pass windows Logo test”, then click “continue anyway” → on new page, click “continue anyway”.
3. Once installed, launch by clicking on the ADS58C48_GUI_vxpx program in Start>Texas Instruments ADCs
4. When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
 - (a) When a pop-up screen opens, select "Continue Downloading".
 - (b) Follow the on screen instructions to install the USB drivers
 - (c) If needed, you can access the drivers directly in the install directory



Figure 1. Found New Hardware



Figure 2. Window Logo Testing

1.2 Software Operation

The software allows full programming control of the ADC device. After launching the ADS58C48_GUI_vxpx program, two levels of register tab are shown on the GUI (see [Figure 3](#)). The Top Level tab provides an interface to the most used registers. The Advanced tab includes rarely used registers and an option to manually input address and data values. Click "Reset USB Port" to set up communication with USB port each time after inserting the USB or powering up the EVM.

1.2.1 Top Level

[Figure 3](#) shows the top level of the register user interface. On this panel, some common registers can be accessed by clicking the switches without typing in the register address and code. The following is a list of functions controlled by the switches or selection boxes on the Top Level panel:

- **Reset:** Device reset, click this switch on or off
- **PND Global:** Device power down, click this switch on or off
- **Data format:** Data output format, can be set into 2's or SOB by clicking this switch on or off
- **LVDS_CMOS Ctrl:** LVDS or CMOS output format, can be selected by set this box
- **Gain_chA:** Gain of Channel A, can be set by this box
- **Gain_chB:** Gain of Channel B, can be set by this box
- **Gain_chC:** Gain of Channel C, can be set by this box
- **Gain_chD:** Gain of Channel D, can be set by this box
- **Test Pattern:** Device test mode enable, can be set by this box
- **SNRBoost ChA:** Channel A SNRBoost enable switch
- **SNRBoost ChB:** Channel B SNRBoost enable switch
- **SNRBoost ChC:** Channel C SNRBoost enable switch
- **SNRBoost ChD:** Channel D SNRBoost enable switch
- **SNRboost filter Ch x:** SNRBoost filter type of channel A, B, C or D can be selected in this group of selection boxes which is located at the right side of the SNRBoost enable switches

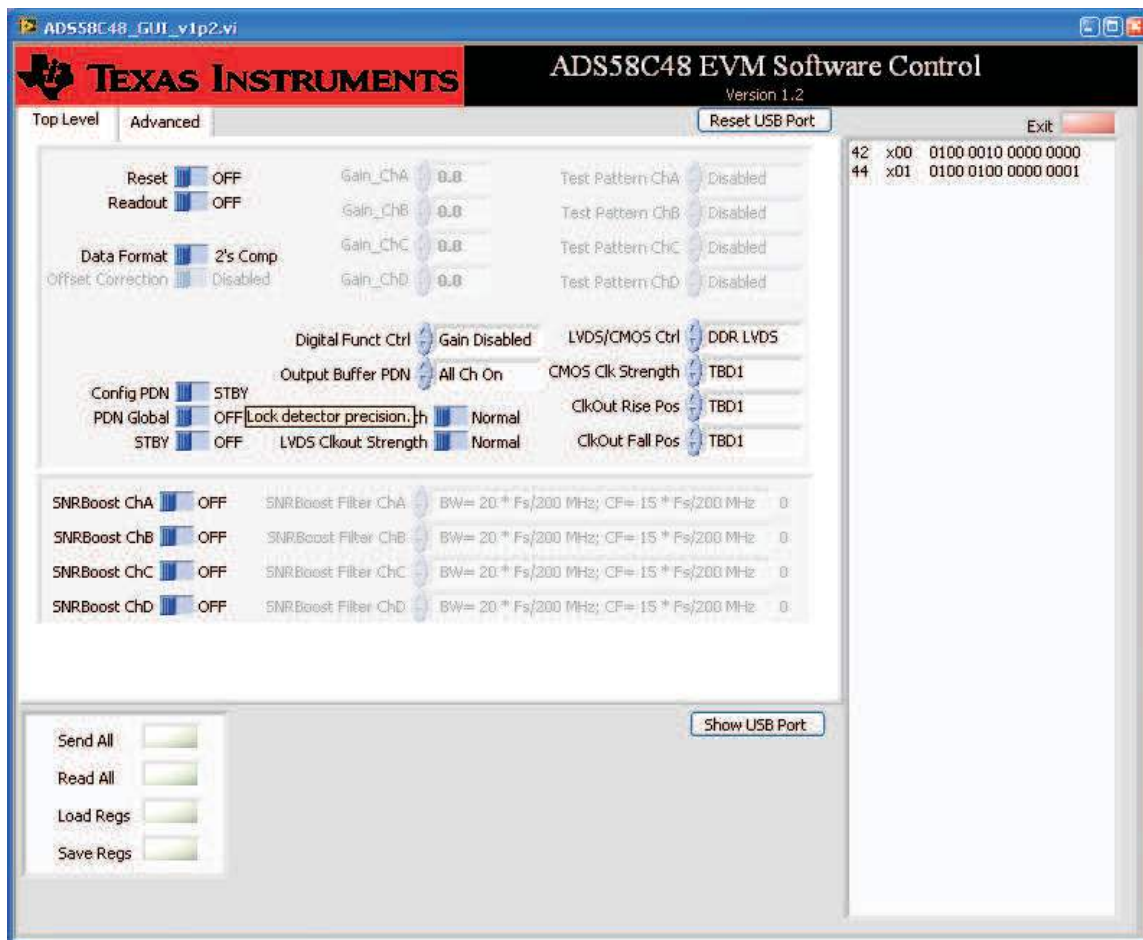


Figure 3. ADS58C48 GUI Front Panel – Top Level

1.2.2 Advanced Level

Click on the "Advanced" tab on the GUI to bring the advanced panel to the front. On this panel, a user can write address and code of the register into the address/code boxes (shown as [Figure 4](#)) then press Enter on the key board or "Send All" button on the panel to send address and code to ADC. The address and code will be shown on the display box located at the right side of the panel when it is sent to ADC. Additional settings on advanced panel can be used to set output offset functions and pin overwrite, as well as virtual LEDs to indicate the custom test pattern.

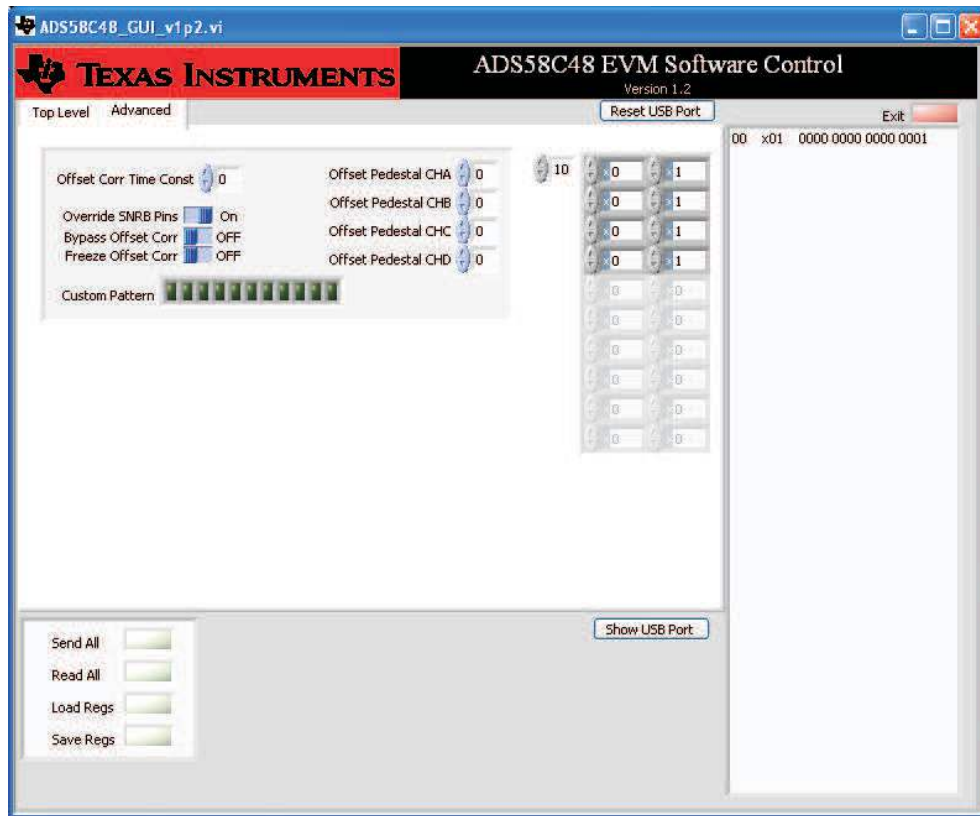


Figure 4. ADS58C48 GUI – Advanced Level

1.2.3 Register Control

- **Send All:** Sends all the register configurations on the panel to the device
- **Read All:** Reads register configuration from device
- **Save Regs:** Saves the register configuration to text file
- **Load Regs:** Loads a register file from a text file. After load register the relative switches and selecting boxes are automatically updated.
 - Select *Load Regs* button.
 - Double click on the *data* folder.
 - Double click on the desired register file.
 - Click on *Send All* to ensure all the values are loaded properly.

1.2.4 Misc Settings

- **Reset USB:** Toggle this button if the USB port is not responding. This generates a new USB handle address
- **Exit:** Stops the program

2 Basic Test Procedure

This section outlines the basic procedure for testing the EVM.

2.1 Test Block Diagram

The test set-up for general testing of the ADS58C48 with the TSW1200 capture card is shown in [Figure 5](#).

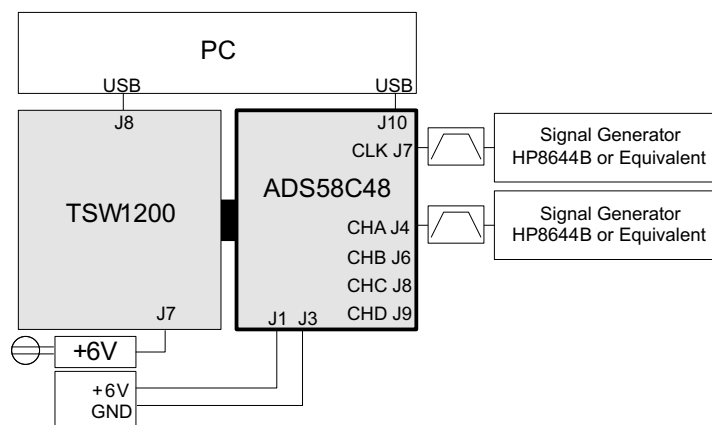


Figure 5. Test Set-up Block Diagram

2.2 Verify Board Set-up

Verify jumper settings are in the correct position as outlined in [Table 1](#).

Table 1. Default EVM Jumper Setting

| Jumper | Default Position | Function |
|--------|------------------|------------------------|
| JP4 | Short 1 - 2 | DC supply for AVdd |
| JP5 | Short 1 - 2 | DC supply for DRVdd |
| JP6 | Short 1 - 2 | USB supply 5 V from PC |
| JP7 | Short 1 - 2 | DC supply 6 V |
| JP8 | Short 1 - 2 | DC supply 3.3 V |
| JP11 | Short 1 - 2 | SNRboost off for chA,B |
| JP12 | Short 5 - 6 | PDN normal |
| JP13 | Short 1 - 2 | SNRboost off for chC,D |
| JP16 | Short 1 - 2 | OPA disable |
| JP17 | Short | OPA gain |
| JP18 | Short 1 - 2 | OPA latch mode |
| JP19 | Short 1 - 2 | OPA gain strobe |

2.3 Test Set-Up Connections

- Connect ADS58C48 EVM to TSW1200 EVM
- Connect 6V power to banana jack at J1; connect ground to J3
- Connect USB cable to programming computer at J10
- Connect USB and power supply jack to TSW1200
- Connect Clock signal through appropriate BPF to J7
- Connect input signal through appropriate BPF to J4, J6, J8 or J9

2.4 TSW1200 Quick Start Operation

For more detailed explanations please refer to the the TSW1200 User's Guide for set-up and operation. This document assumes the TSW1200 software is installed and functioning properly. The front panel of the TSW1200 is shown in [Figure 6](#). The following configuration needs to be changed from the default settings.

- Jumper setting on TSW1200 board
 - Set J11 (2-3) or High, J10 (1-2) or Low for LVDS DDR data input (default)
 - Set J11 (2-1) or Low, J10 (1-2) or Low for 1-wire serial data input
- Select ADS58C48 device name from the TI ADC Selection pull-down menu
 - If this option is not available then download the latest ini file from the product folder of the TSW1200 at www.ti.com
 - Place updated ini files in the TSW1200 product directory located at C:\Program Files\Texas Instruments\TSW1200\ADC Files
- Select Single Tone FFT from the Test pull-down menu
- Select the desired channel (i.e. Channel A, B, C, or D) from the Channel Display pull-down menu
- Change ADC sampling rate to desired value (i.e., 200 MHz)
- Change input frequency to desired value (i.e., 149 MHz or other)
- Press Ctrl-Shift-I to reset the software as needed
- Verify status display in lower left has no errors
- Press Capture button to initiate a data capture

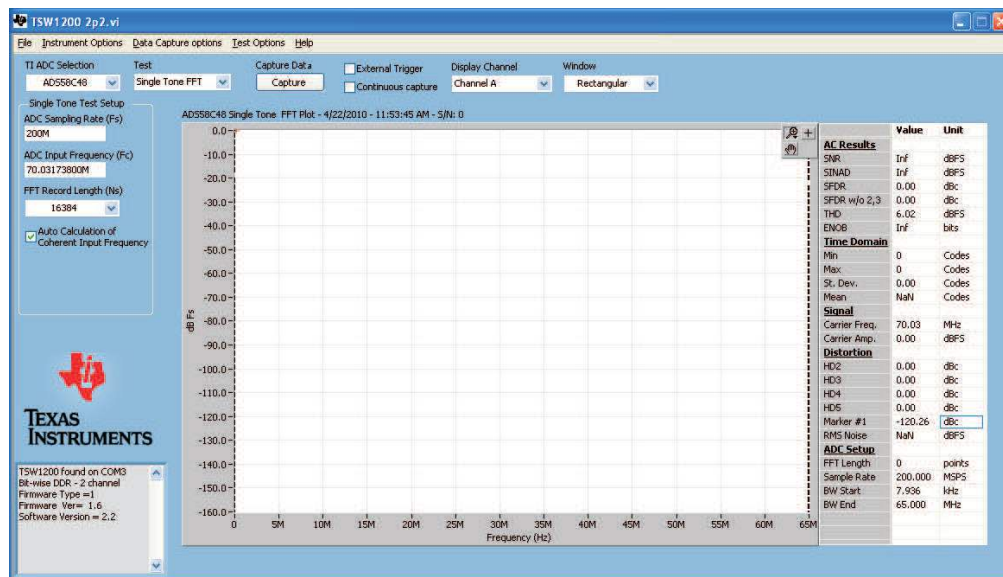


Figure 6. TSW1200 GUI

2.5 ADS58C48 Test Procedure

- Switch on 6V power supply. Verify source current is about 470 mA +/- 20 mA with clock and TSW1200 connected at SNRBoost on for 4 channels.
- Connect clock signal at J7 through an appropriate BPF.
 - Adjust the signal generator amplitude output to provide approximately 1 Vpp at J7.
 - Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Connect input signal through an appropriate BPF at either: J4, J6, J8 or J9 (Channel A, B, C or D).
 - Adjust frequency of generator to match the coherent frequency displayed in the TSW1200 GUI.
 - Select the proper Display Channel on the TSW1200 GUI software that corresponds to the input connection.
 - Adjust the signal generator amplitude output to achieve -1 dBFS.

- Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Enable SNR Boost (if desired)
 - Hardware enable by SNRBoost pins, JP11 and JP13
 - Set Digital Funct Ctrl to "Gain Enabled"
 - Select desired SNRBoost Filter Chx register
 - Set Digital Funct Ctrl to "Gain Disabled"
 - Use Hardware pins at jumper JP11 and JP13 to turn on/off SNR Boost for each pair of channels
 - Software enable by setting the GUI registers only
 - Set Digital Funct Ctrl to "Gain Enabled"
 - Set desired SNRBoost Chx to On
 - Select desired SNRBoost Filter Chx register
 - Set Digital Funct Ctrl to "Gain Disabled"
 - Set Override SNRb Pins on Advanced Tab to On
- Initiate a capture by pressing the Capture button on the TSW1200 GUI.

2.6 ADS58C48 Performance Results

Figure 7 shows the performance results with the SNR Boost disabled at 200 MSPS clock frequency and with a 149 MHz input tone. Figure 8 shows the same set-up with SNR Boost enabled using a filter register setting of 40 ($BW = 60 \times F_s/184$ MHz; $CF = 46 \times F_s/184$ MHz) corresponding roughly to 60 MHz of BW for the given clocking rate. ADC calculations related to SNR and SFDR are completed over this specified bandwidth.

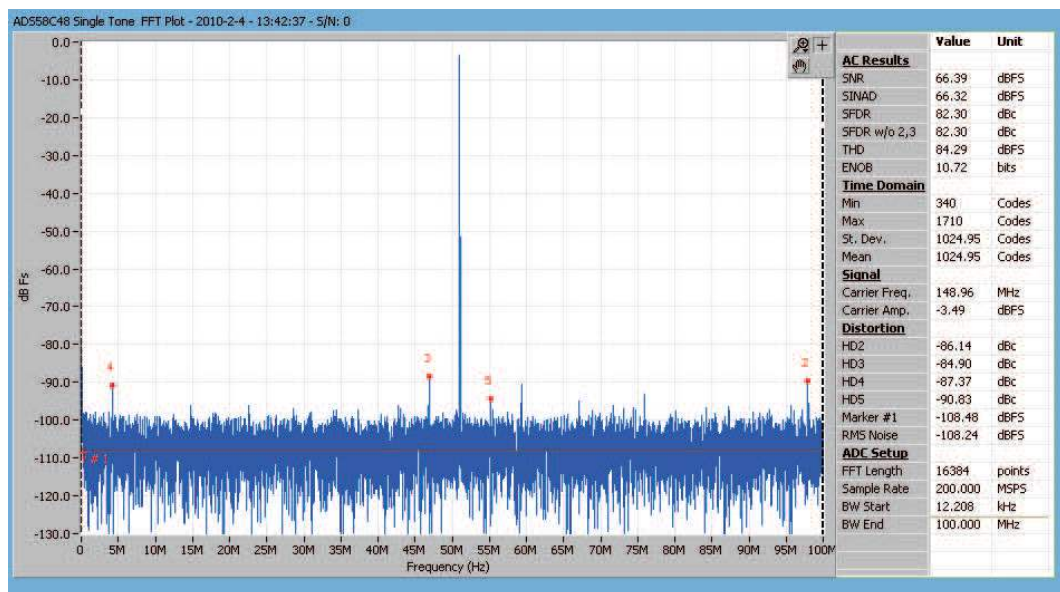


Figure 7. FFT Plot: 200 MHz Clock, 149 MHz input; SNRBOOST Disable

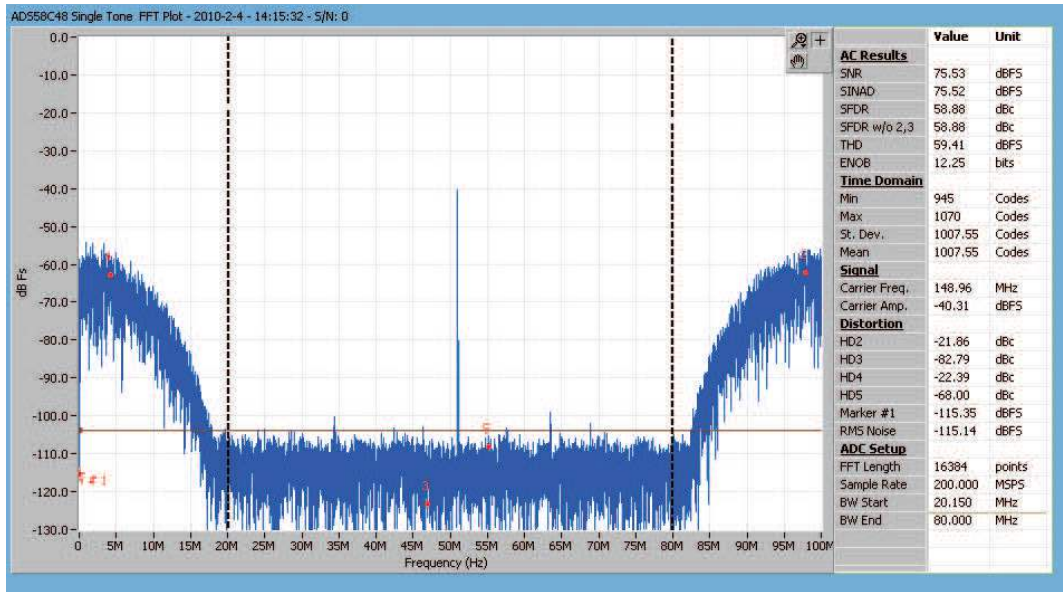


Figure 8. FFT Plot: 200 MHz clock, 149 MHz input; SNRBOOST Enabled With Filter #40

3 Optional Configuration: PGA870

Channel D input (J9) can be configured to utilize the programmable gain op-amp, PGA870. The changes required to modify the transformer coupled input to the OPA-driven input are shown in .

Table 2. Jumper Setting for Transformer-Coupled or OPA-Driven Input

| Jumpers | Transformer-Coupled Input | OPA-Driven Input |
|---------|---------------------------|--------------------|
| SJP1 | Shunt 1-2, default | Shunt 3-2 |
| SJP2 | Shunt 1-2, default | Shunt 3-2 |
| SJP3 | | Shunt 3-2, option |
| SJP4 | Shunt 1-2, default | Shunt 3-2 |
| JP16 | | Shunt 1-2 |
| JP17 | | Shunt 1-2, default |
| JP18 | | Shunt 1-2, default |
| JP19 | | Shunt 1-2, default |

Power is supplied to the device by applying 5 V to J2 and GND J3. By default the PGA870 is set as fixed gain. There is gain control available through SW2, JP18 and JP19. An on-board layout option for a LPF or BPF is available between the amplifier and the ADC. By default the filter is bypassed to allow the user flexibility to design according to desired specifications.

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