MC54/74HC160A
MC54/74HC162A

Product Preview

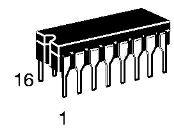
Presettable Counters

High–Performance Silicon–Gate CMOS

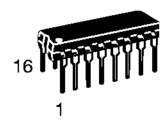
The MC54/74HC160A and HC162A are identical in pinout to the LS160 and LS162, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160A and HC162A are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively.

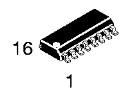
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620–10



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

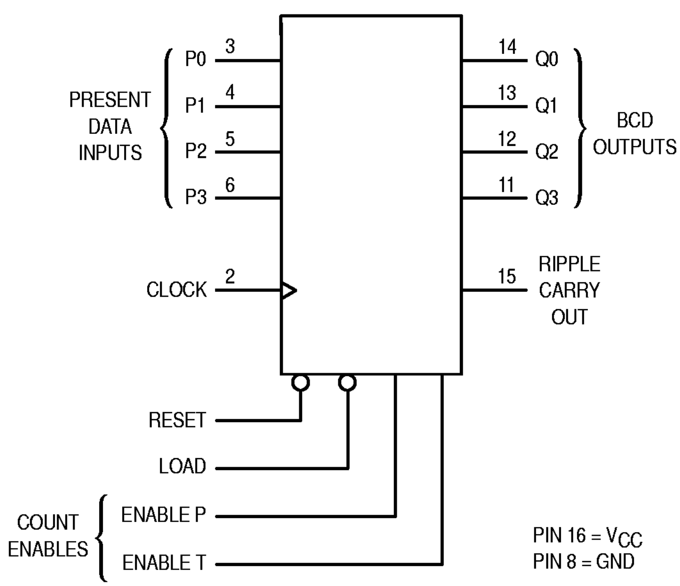


D SUFFIX
SOIC PACKAGE
CASE 751B–05

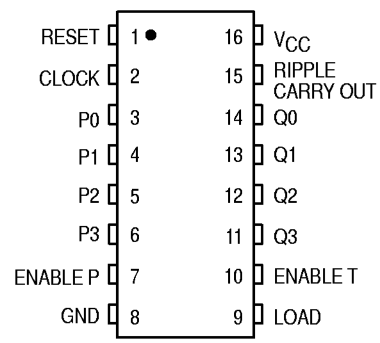
ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC

LOGIC DIAGRAM



PIN ASSIGNMENT



Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC162	BCD	Synchronous

FUNCTION TABLE

Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
↑	L	X	X	X	Reset
↑	H	L	X	X	Load Preset Data
↑	H	H	H	H	Count
↑	H	H	L	X	No Count
↑	H	H	X	L	No Count

* HC162A only. HC160A is an Asynchronous Reset Device
H = high level
L = low level
X = don't care

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \leq$ 20 µA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert \leq$ 20 µA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \leq$ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \leq$ 2.4 m $\lvert I_{out} \rvert \leq$ 4.0 mA $\lvert I_{out} \rvert \leq$ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \leq$ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \leq$ 2.4 m $\lvert I_{out} \rvert \leq$ 4.0 mA $\lvert I_{out} \rvert \leq$ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 µA	6.0	4	40	160	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)* (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 TBD 30 35	4.8 TBD 24 28	4.0 TBD 20 24	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0 3.0 4.5 6.0	170 TBD 34 29	215 TBD 43 37	255 TBD 51 43	ns
t_{PHL}		2.0 3.0 4.5 6.0	205 TBD 41 35	255 TBD 51 43	310 TBD 62 53	
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160A Only) (Figures 2 and 7)	2.0 3.0 4.5 6.0	210 TBD 42 36	265 TBD 53 45	315 TBD 63 54	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0 3.0 4.5 6.0	160 TBD 32 27	200 TBD 40 34	240 TBD 48 41	ns
t_{PHL}		2.0 3.0 4.5 6.0	195 TBD 39 33	245 TBD 49 42	295 TBD 59 50	
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0 3.0 4.5 6.0	175 TBD 35 30	220 TBD 44 37	265 TBD 53 45	ns
t_{PHL}		2.0 3.0 4.5 6.0	215 TBD 43 37	270 TBD 54 46	325 TBD 65 55	
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160A Only) (Figures 2 and 7)	2.0 3.0 4.5 6.0	220 TBD 44 37	275 TBD 55 47	330 TBD 66 56	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

* Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f_{max}. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f_{max} in the table above is applicable. See Applications Information in this data sheet.

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	60	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0 3.0 4.5 6.0	150 TBD 30 26	190 TBD 38 33	225 TBD 45 38	ns
t_{su}	Minimum Setup Time, Load to Clock (Figure 5)	2.0 3.0 4.5 6.0	135 TBD 27 23	170 TBD 34 29	205 TBD 41 35	ns
t_{su}	Minimum Setup Time, Reset to Clock (HC162A only) (Figure 4)	2.0 3.0 4.5 6.0	160 TBD 32 27	200 TBD 40 34	240 TBD 48 41	ns
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0 3.0 4.5 6.0	200 TBD 40 34	250 TBD 50 43	300 TBD 60 51	ns
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0 3.0 4.5 6.0	50 TBD 10 9	65 TBD 13 11	75 TBD 15 13	ns
t_h	Minimum Hold Time, Clock to Load (Figure 5)	2.0 3.0 4.5 6.0	3 TBD 3 3	3 TBD 3 3	3 TBD 3 3	ns
t_h	Minimum Hold Time, Clock to Reset (HC162A only) (Figure 4)	2.0 3.0 4.5 6.0	3 TBD 3 3	3 TBD 3 3	3 TBD 3 3	ns
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0 3.0 4.5 6.0	3 TBD 3 3	3 TBD 3 3	3 TBD 3 3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HC160A only) (Figure 2)	2.0 3.0 4.5 6.0	125 TBD 25 21	155 TBD 31 26	190 TBD 38 32	ns
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0 3.0 4.5 6.0	125 TBD 25 21	155 TBD 31 26	190 TBD 38 32	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	80 TBD 16 14	100 TBD 20 17	120 TBD 24 20	ns
t_w	Minimum Pulse Width, Reset (HC160A only) (Figure 2)	2.0 3.0 4.5 6.0	80 TBD 16 14	100 TBD 20 17	120 TBD 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

FUNCTION DESCRIPTION

The HC160A/162A are programmable 4–bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count–enable controls.

The HC160A and HC162A are BCD counters with asynchronous Reset, and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip–flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting (HC162A) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip–flops and appear at the counter outputs. P0 (pin 3) is the least–significant bit and P3 (pin 6) is the most–significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs (BCD or binary). Q0 (pin 14) is the least–significant bit and Q3 (pin 11) is the most–significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look–ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

Ripple Carry Out = Enable T • Q0 • $\overline{Q1}$ • $\overline{Q2}$ • Q3 for BCD counters HC160A and HC162A

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (pin 1) resets the internal flip–flops and sets the outputs (Q0 through Q3) to a low level. The HC160A resets asynchronously and the HC162A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip–flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160A and HC162A are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

Count Enable/Disable

These devices have two count–enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

Count Enable = Enable P • Enable T • Load

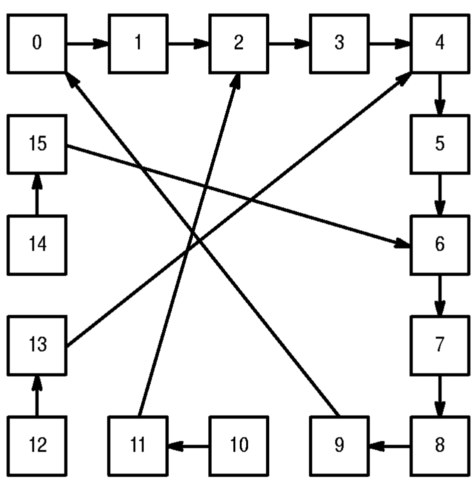
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count–enable control; Enable T is both a count–enable and a Ripple–Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0 – Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

* Q0 through Q3 are maximum for the HC160A and HC162A when Q3 Q2 Q1 Q0 = 1001.

OUTPUT STATE DIAGRAMS
HC160A and HC162A BCD Counters



SWITCHING WAVEFORMS

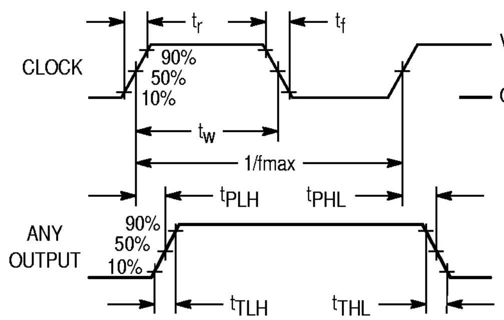


Figure 1.

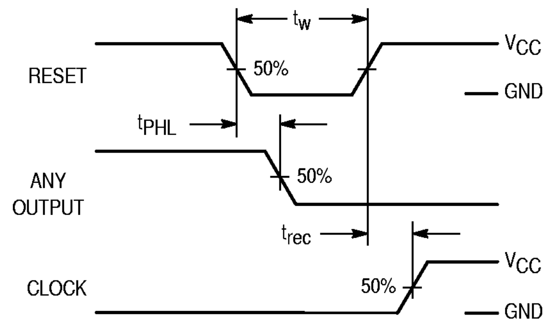


Figure 2.

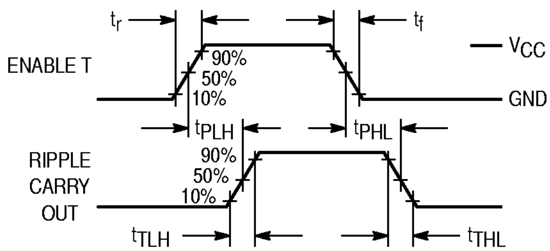


Figure 3.

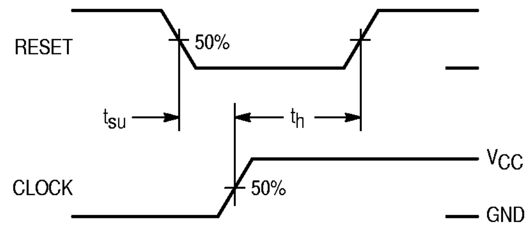


Figure 4. HC162A Only

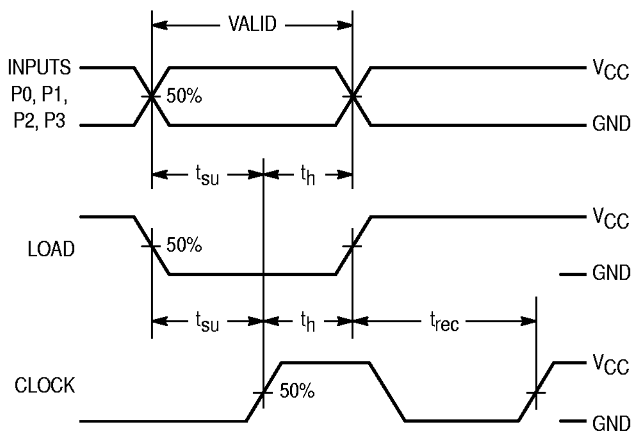


Figure 5.

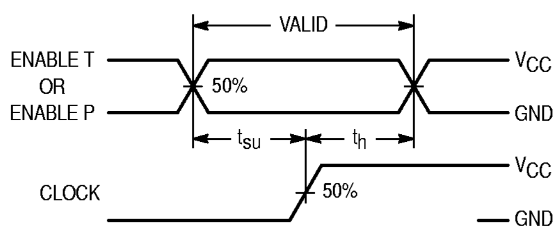
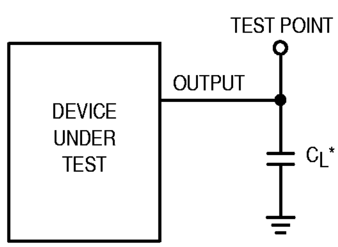


Figure 6.

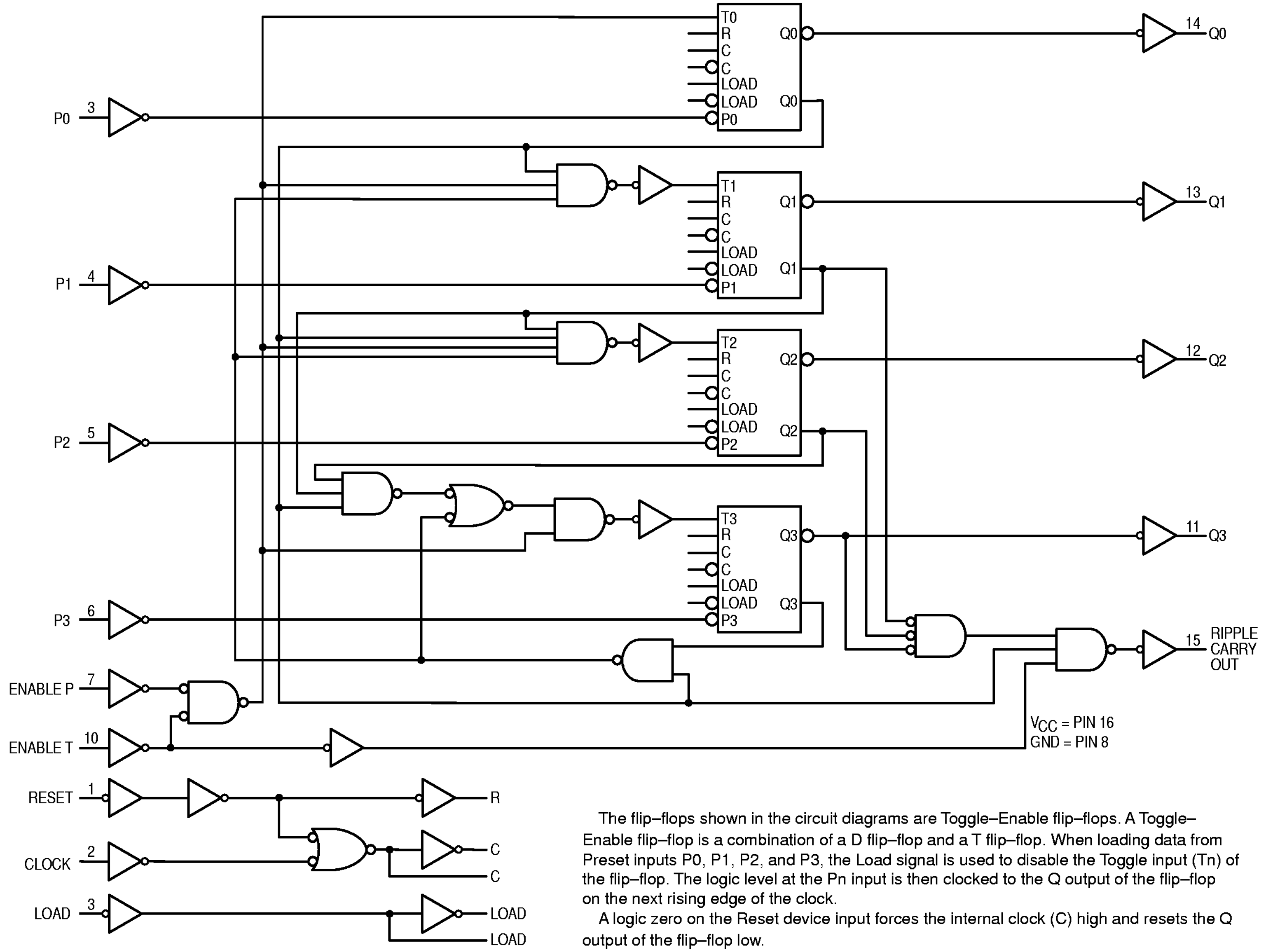
TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 7.

MC54HC160A • MC74HC160A
BCD Counter with Asynchronous Reset

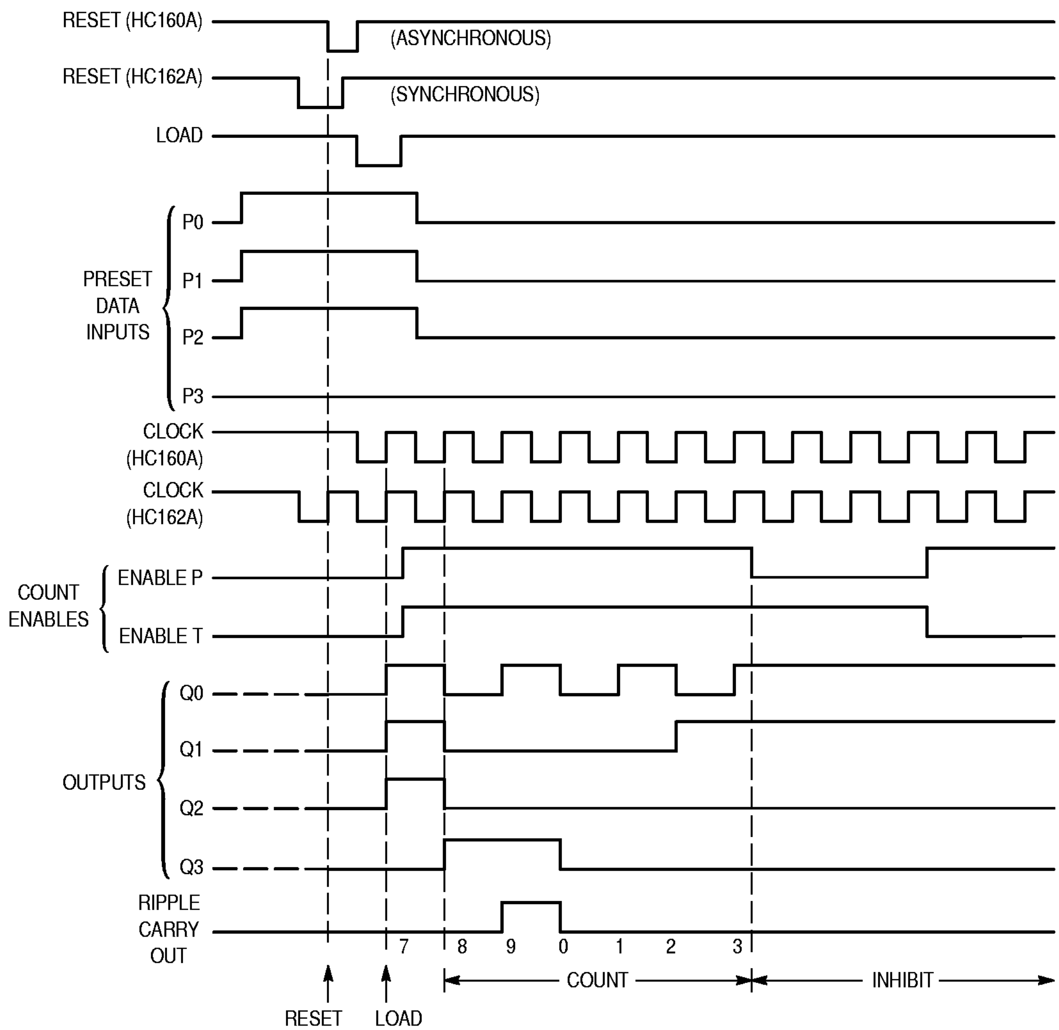


The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip–flop. The logic level at the Pn input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

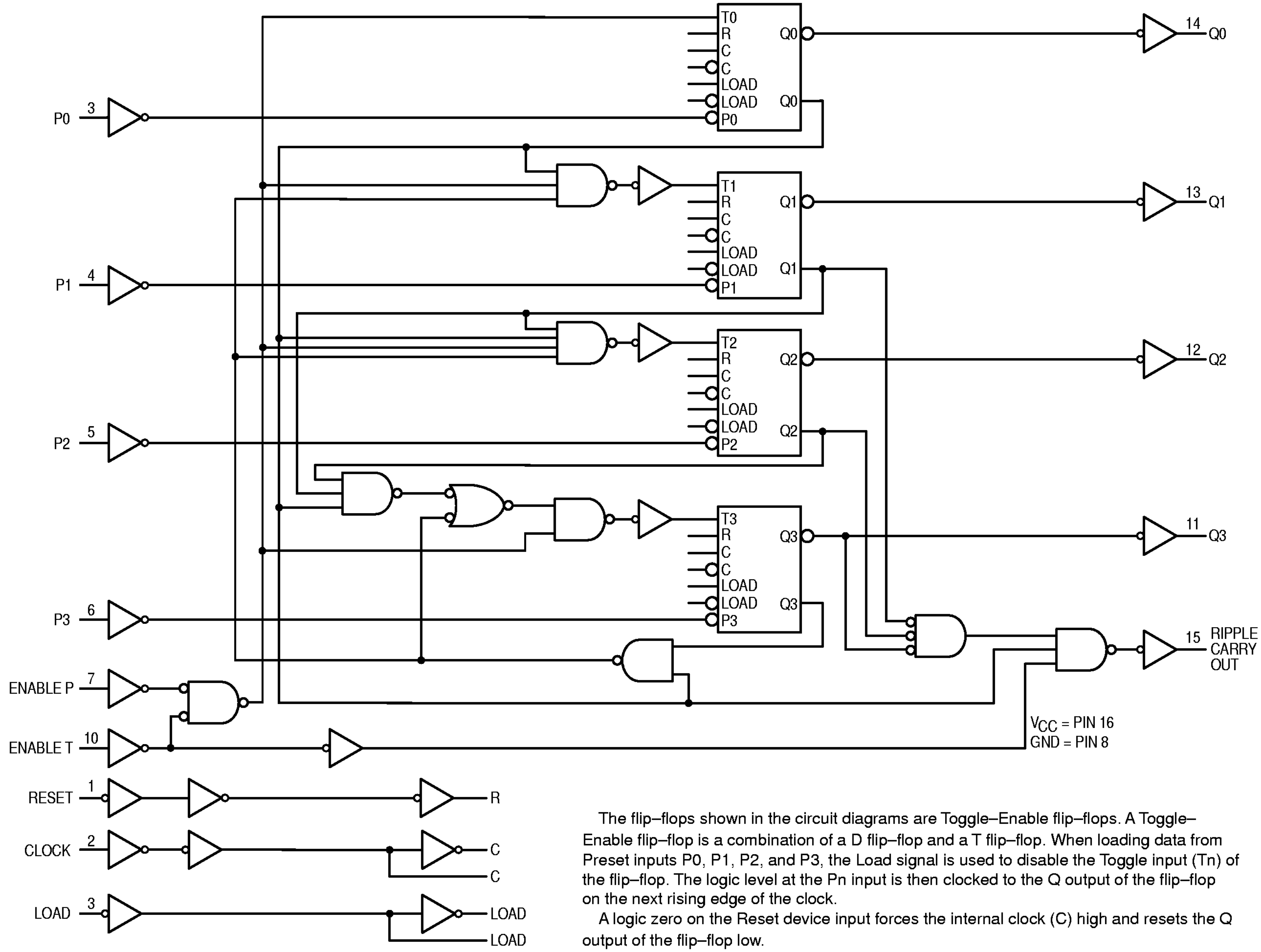
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

HC160A, HC162A TIMING DIAGRAM

Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



MC54HC160A • MC74HC160A
BCD Counter with Synchronous Reset

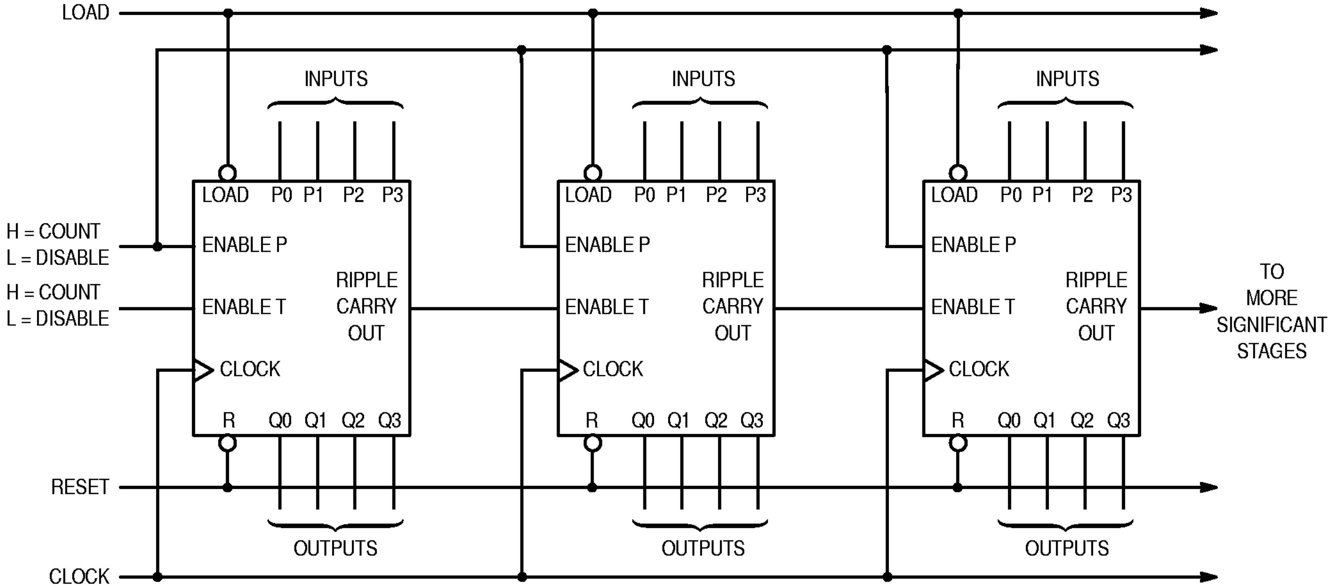


The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip–flop. The logic level at the Pn input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

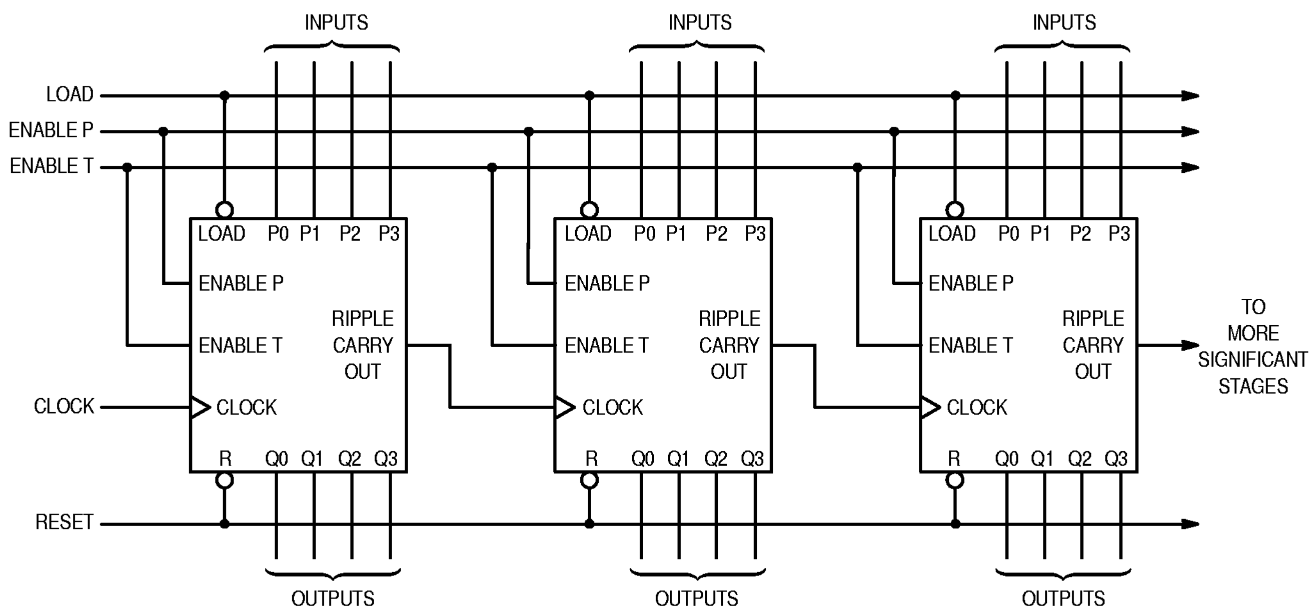
TYPICAL APPLICATIONS
CASCADING

N–Bit Synchronous Counters

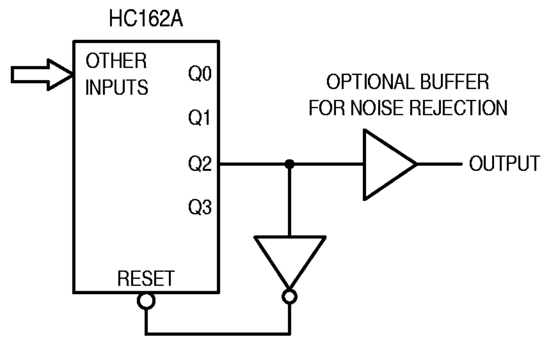


NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Nibble Ripple Counter



TYPICAL APPLICATION

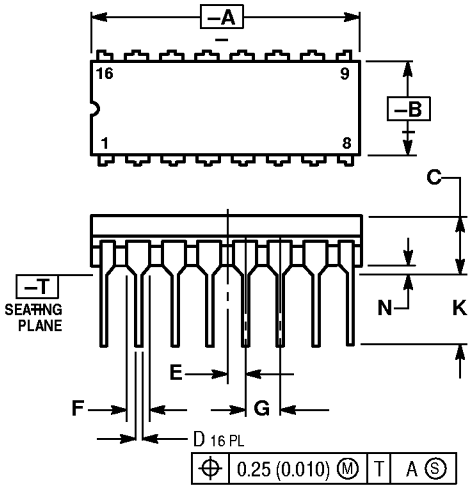


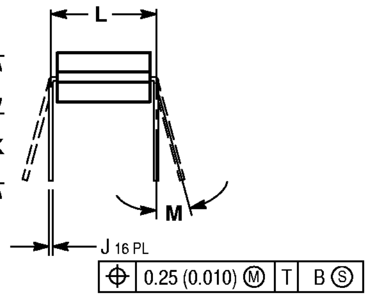
Modulo–5 Counter

The HC162A facilitates designing counters of any modulus with minimal external logic. The output is glitch–free due to the synchronous Reset.

OUTLINE DIMENSIONS

J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V

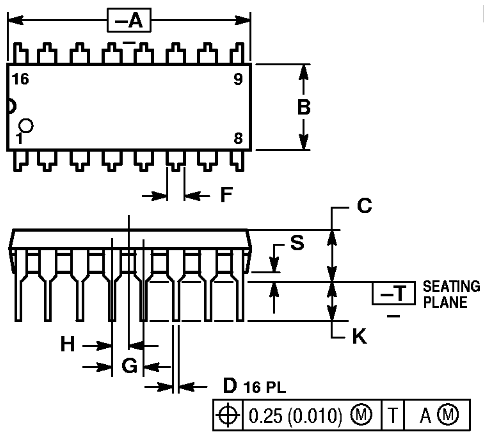


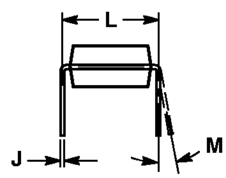


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

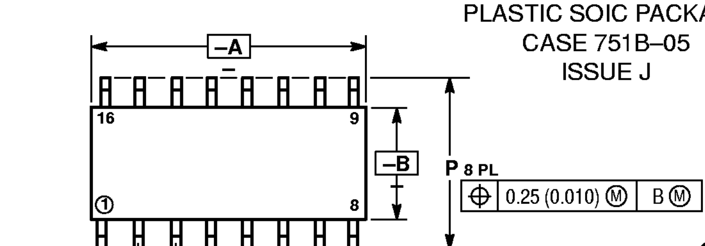


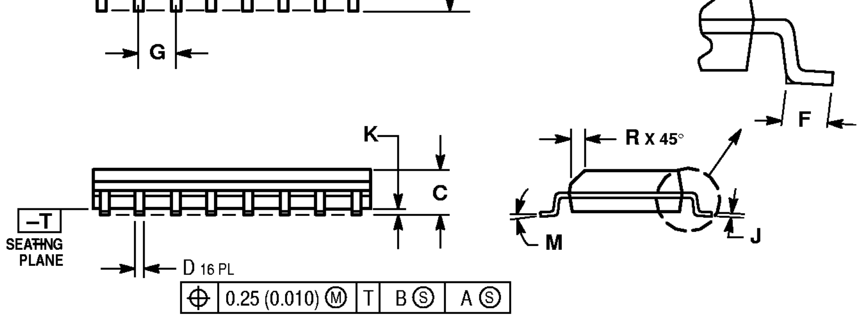


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019