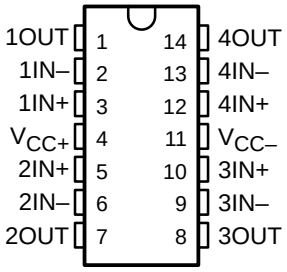
SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

- **Wide Range of Supply Voltages, Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to Be Interchangeable With Motorola MC3303, MC3403**

MC3303 . . . D, N, OR PW PACKAGE
MC3403 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the μA741, but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} – 1.5 V. Quiescent supply currents are less than one-half those of the μA741.

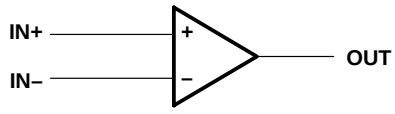
The MC3303 is characterized for operation from –40°C to 85°C, and the MC3403 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

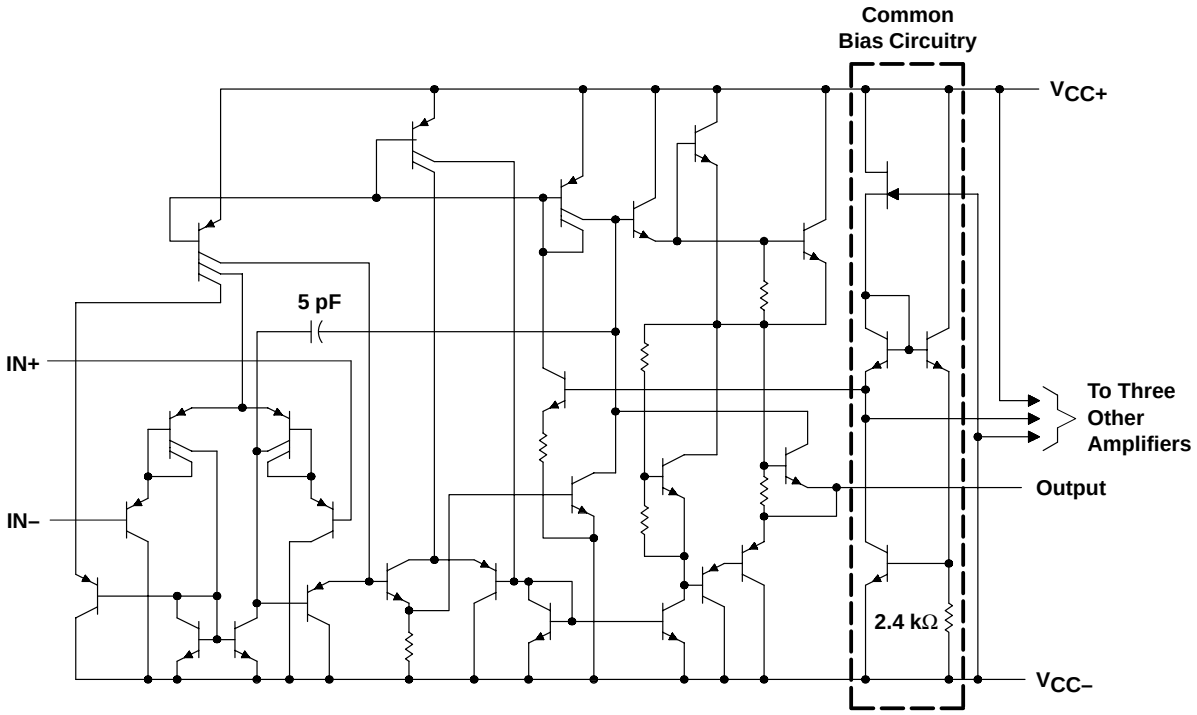
T_A	V_{IO}MAX AT 25°C	PACKAGE			
		PLASTIC SMALL OUTLINE (D, NS)	PLASTIC SHRINK SMALL OUTLINE (DB)	PLASTIC DIP (N)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)
0°C to 70°C	10 mV	MC3403D MC3403NS	MC3403DB	MC3403N	MC3403PW
–40°C to 85°C	8 mV	MC3303D	—	MC3303N	MC3303PW

The D package is available taped and reeled. Add R suffix to the device type (e.g., MC3403DR). The DB, NS, and PW packages are only available taped and reeled.

logic diagram (each amplifier)



schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}	18 V
$V_{CC–}$	–18 V
Supply voltage, V_{CC+} with respect to $V_{CC–}$	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage (see Notes 1 and 3)	±18 V
Package thermal impedance, θ_{JA} (see Note 4): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
2. Differential voltages are at IN+ with respect to IN–.
3. Neither input must ever be more positive than V_{CC+} or more negative than $V_{CC–}$.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		5	30	V
	Dual-supply voltage	V_{CC+}	2.5	15	V
		V_{CC-}	–2.5	–15	V
T_A	Operating free-air temperature	MC3303	–40	85	°C
		MC3403	0	70	

electrical characteristics at specified free-air temperature, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303, $V_{CC\pm}$ = ±15 V for MC3403 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 5	25°C		2	8		2	10	mV
			Full range			10			12	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	See Note 5	Full range		10			10		µV/°C
I_{IO}	Input offset current	See Note 5	25°C		30	75		30	50	nA
			Full range			250			200	
$\alpha_{I_{IO}}$	Temperature coefficient of input offset current	See Note 5	Full range		50			50		pA/C
I_{IB}	Input bias current	See Note 5	25°C		–0.2	–0.5		–0.2	–0.5	µA
			Full range			–1			–0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	12	12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	10	12		±10	±13		
		R_L = 2 kΩ	Full range	10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±2.5 to ±15 V	25°C		30	150		30	150	µV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 5	25°C		2.8	7		2.8	7	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is –40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡ The V_{ICR} limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V_{CC+}.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 5: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403 and V_O = 7 V for MC3303.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V			–0.5		–0.2	–0.5	µA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	V_{CC+} – 1.7			V_{CC+} – 1.7			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V			150			150	µV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		2.5	7		2.5	7	mA
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303, $V_{CC\pm}$ = ±15 V for MC3403, T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS				TYP	UNIT
SR	Slew rate at unity gain	V_I = ±10 V,	C_L = 100 pF,	R_L = 2 kΩ,	See Figure 1	0.6	V/µs
t_r	Rise time	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	0.35	µs
t_f	Fall time	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	0.35	µs
	Overshoot factor	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ,	See Figure 1	20	%
	Crossover distortion	$V_{I(PP)}$ = 30 mV,	V_{OPP} = 2 V,	f = 10 kHz		1	%

PARAMETER MEASUREMENT INFORMATION

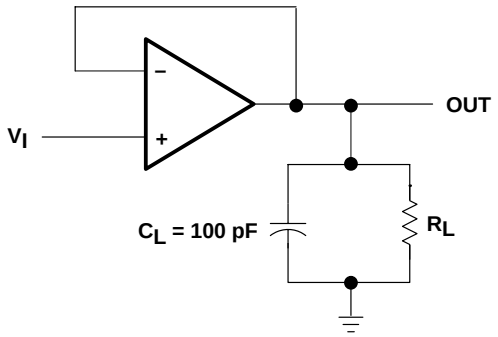


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

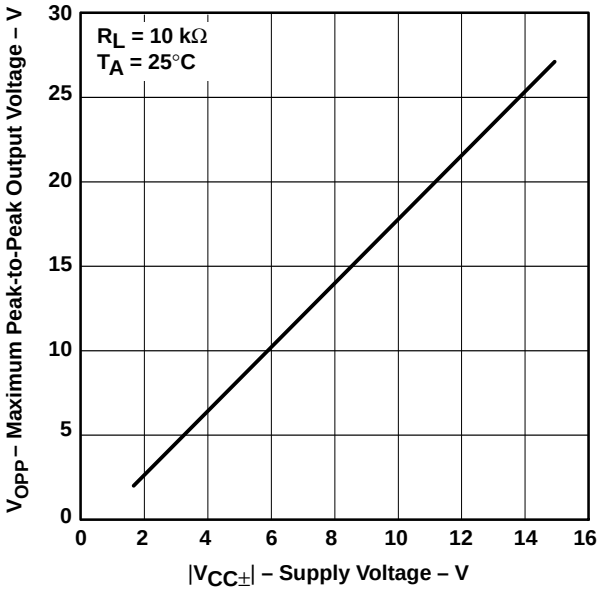


Figure 2

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

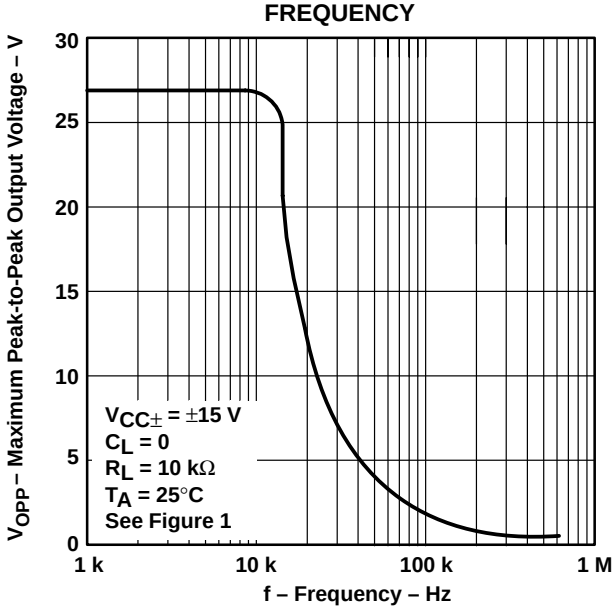


Figure 3

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

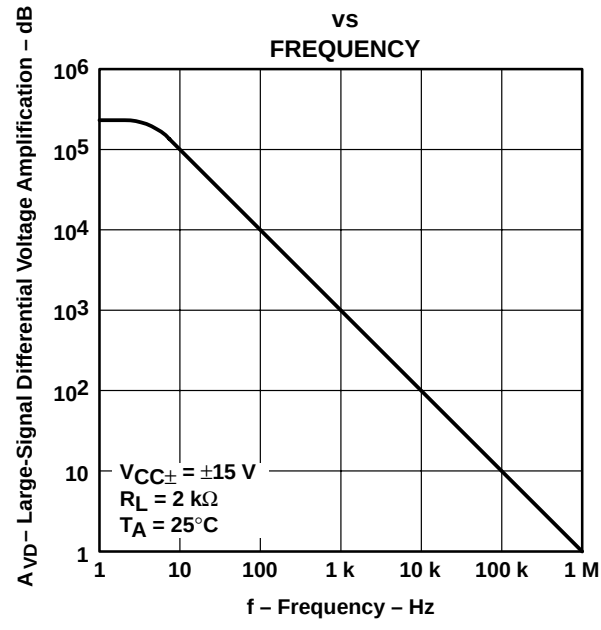


Figure 4

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

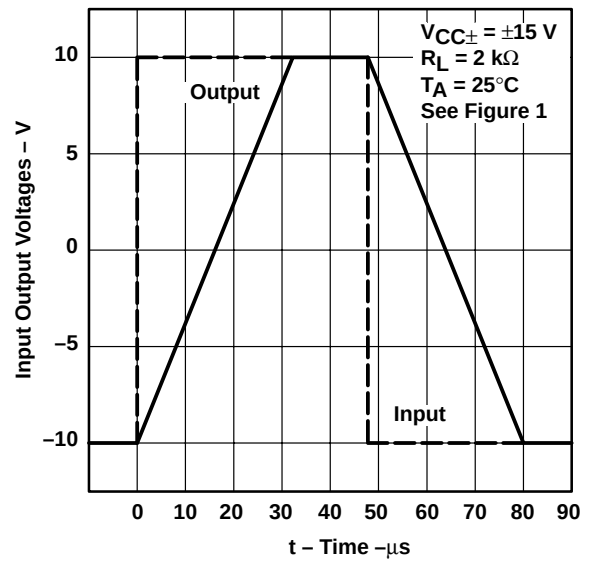


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†

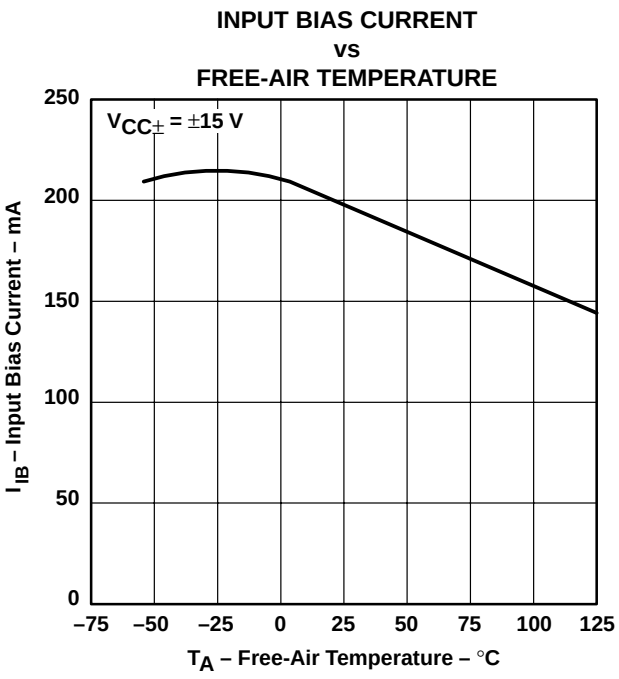


Figure 6

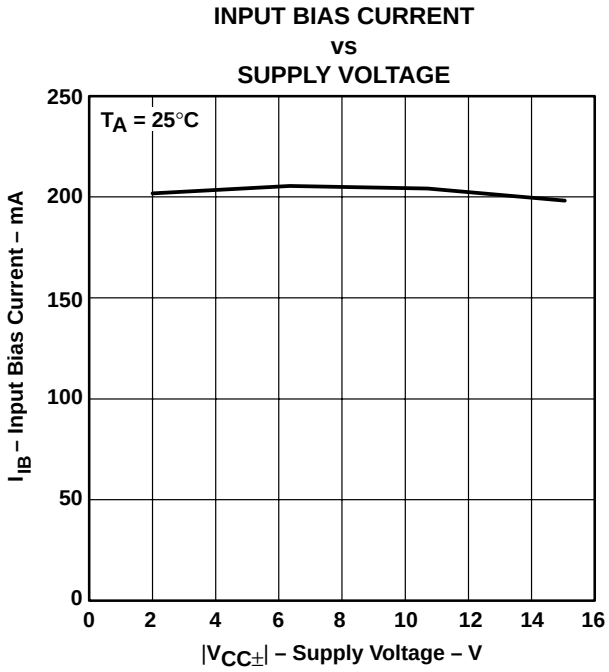


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MC3303D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3303NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3303PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3303PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3403NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3403NSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
MC3403NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

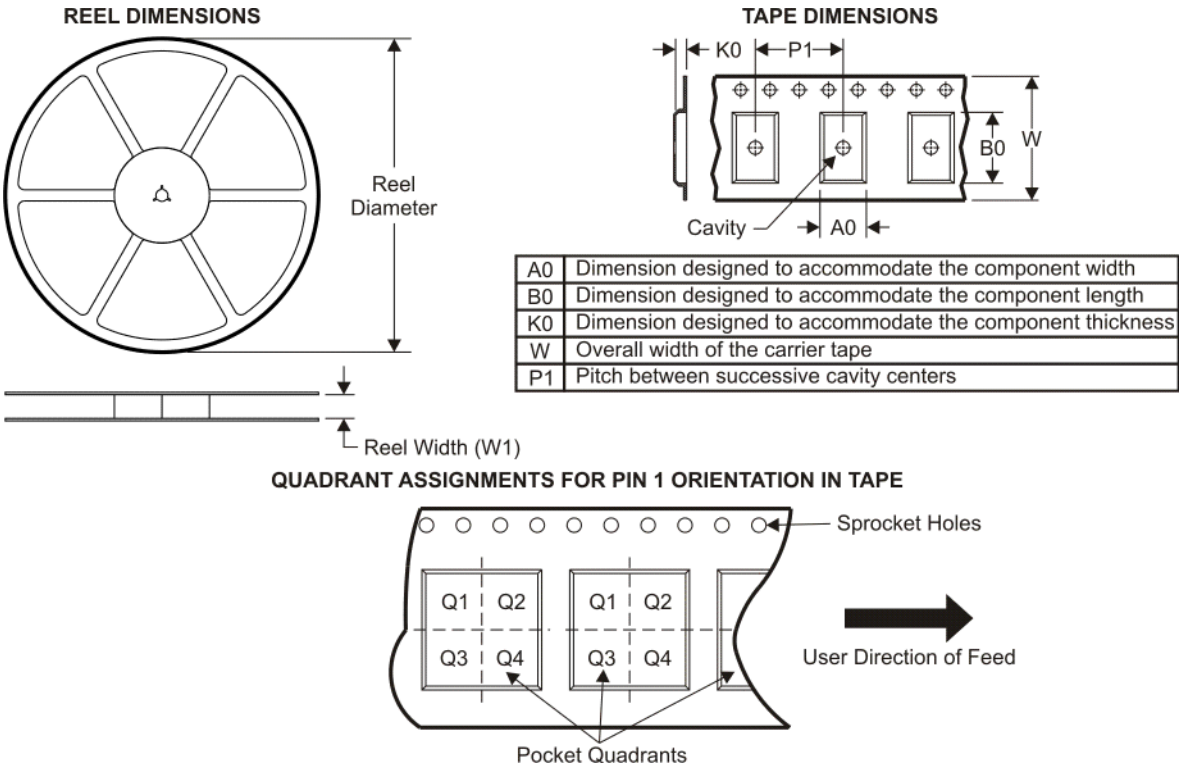
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MC3403PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3403PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

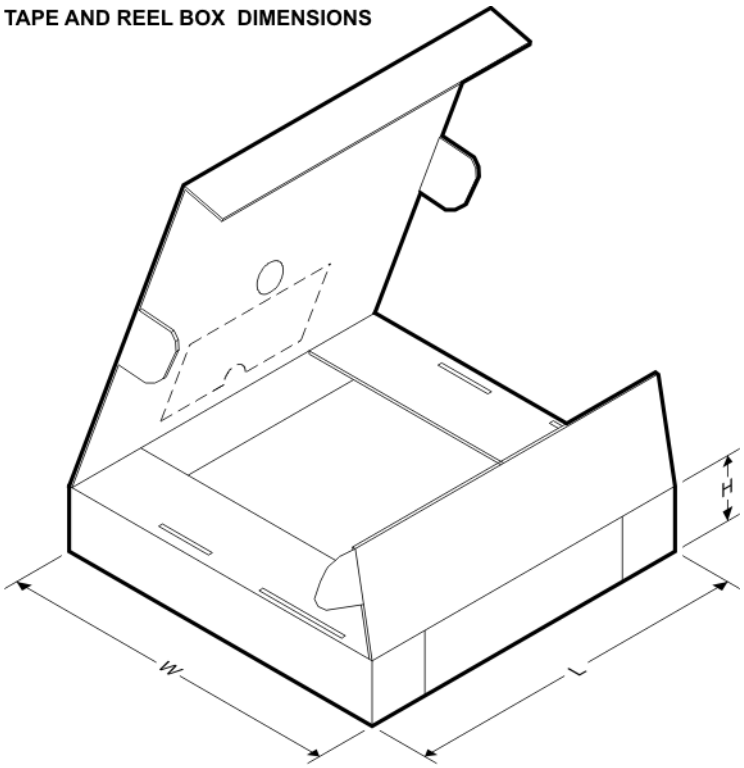


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3303DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3303PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MC3403DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3403DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3403NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MC3403PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



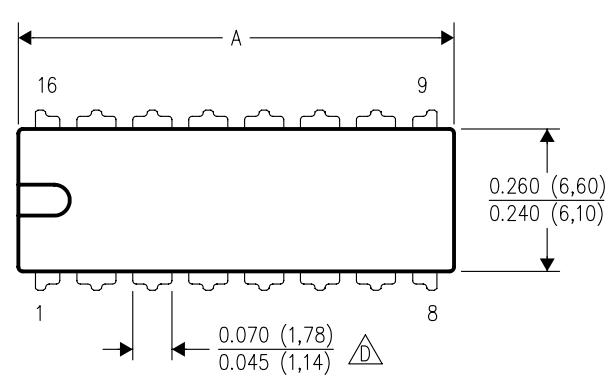
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3303DR	SOIC	D	14	2500	346.0	346.0	33.0
MC3303PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
MC3403DR	SOIC	D	14	2500	346.0	346.0	33.0
MC3403DR	SOIC	D	14	2500	333.2	345.9	28.6
MC3403NSR	SO	NS	14	2000	346.0	346.0	33.0
MC3403PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

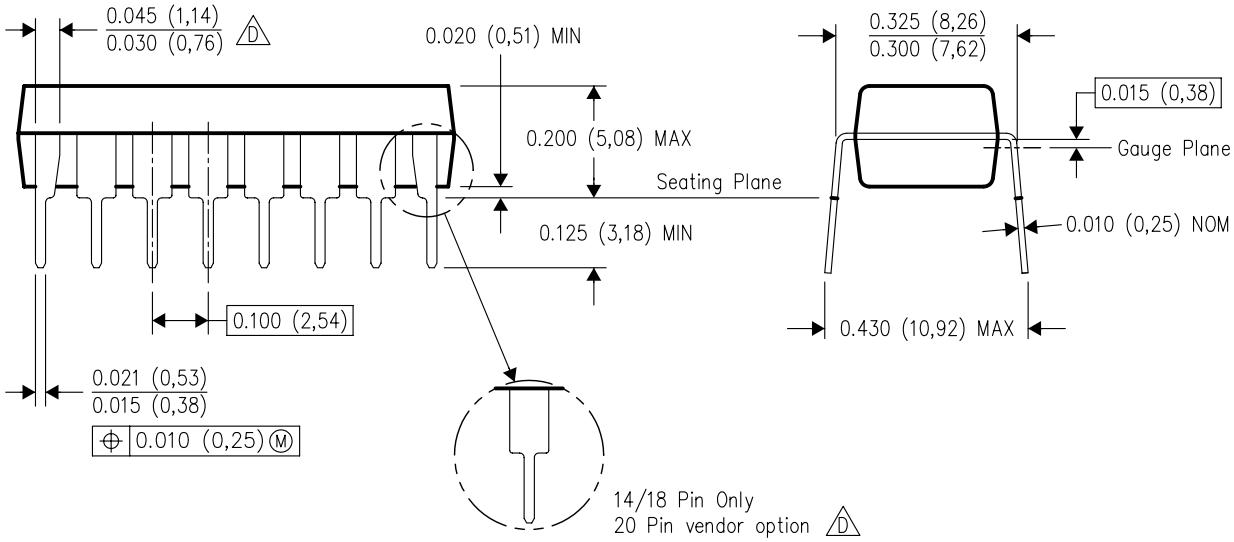
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



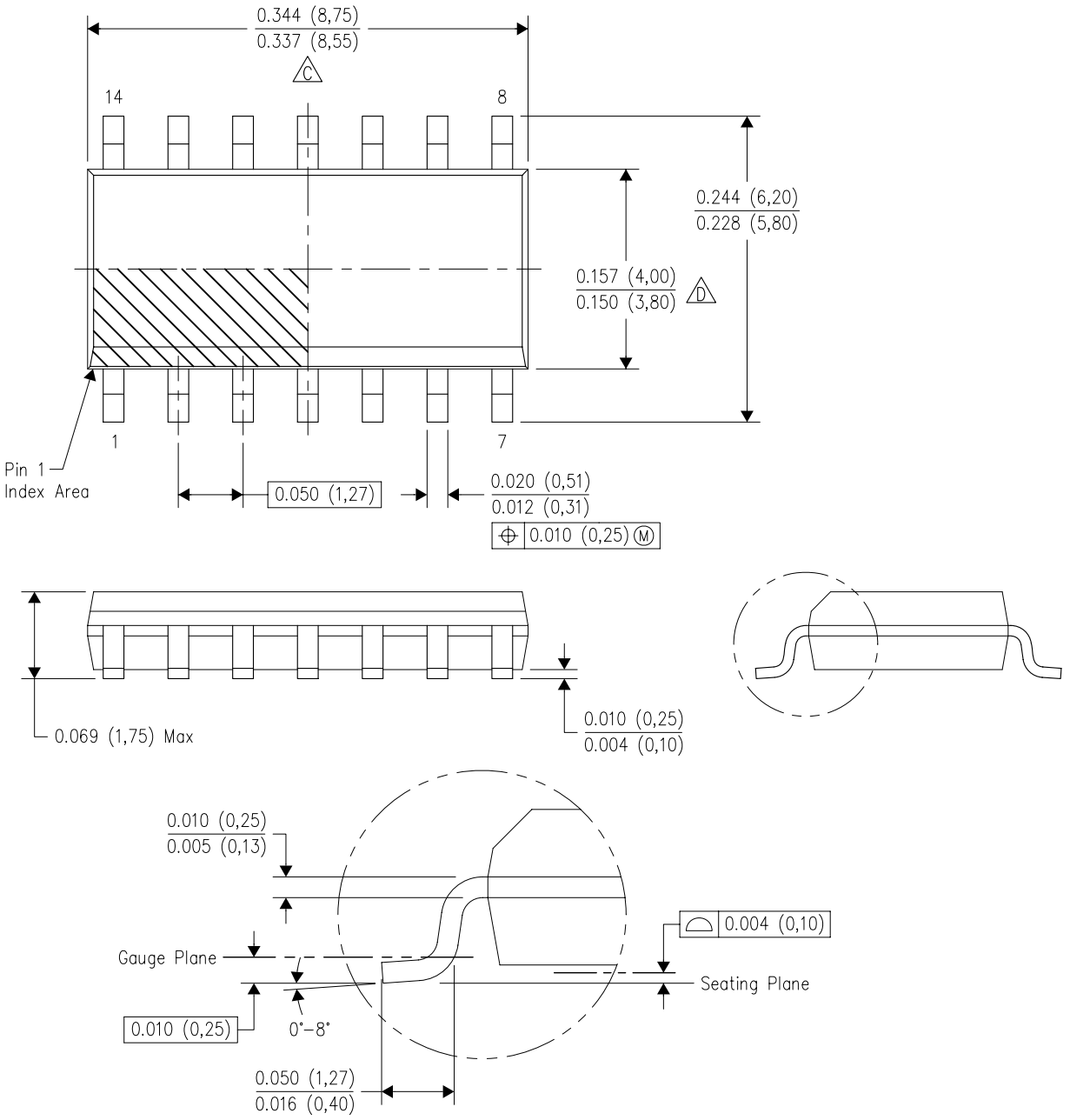
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

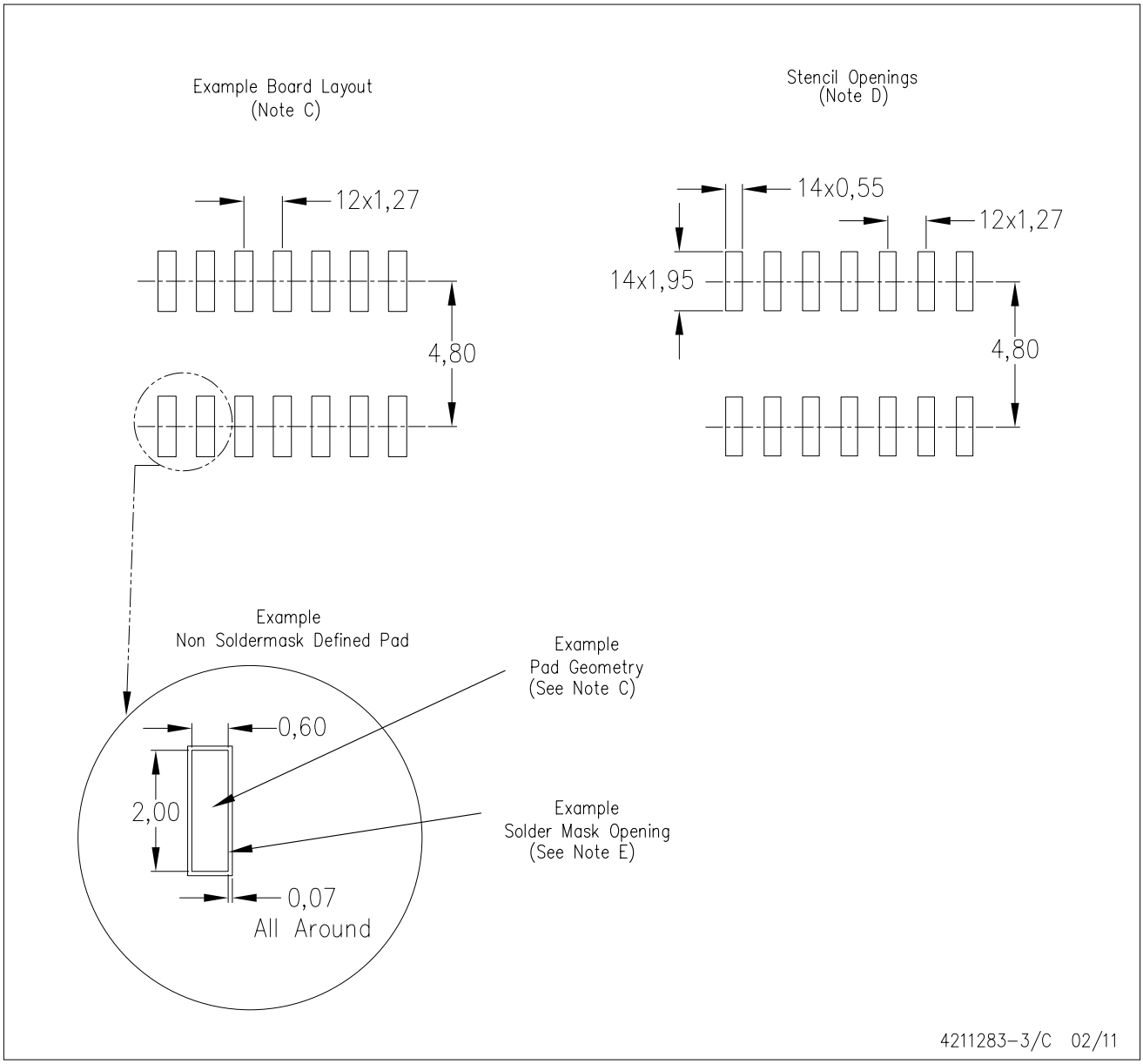
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–4/L 02/11

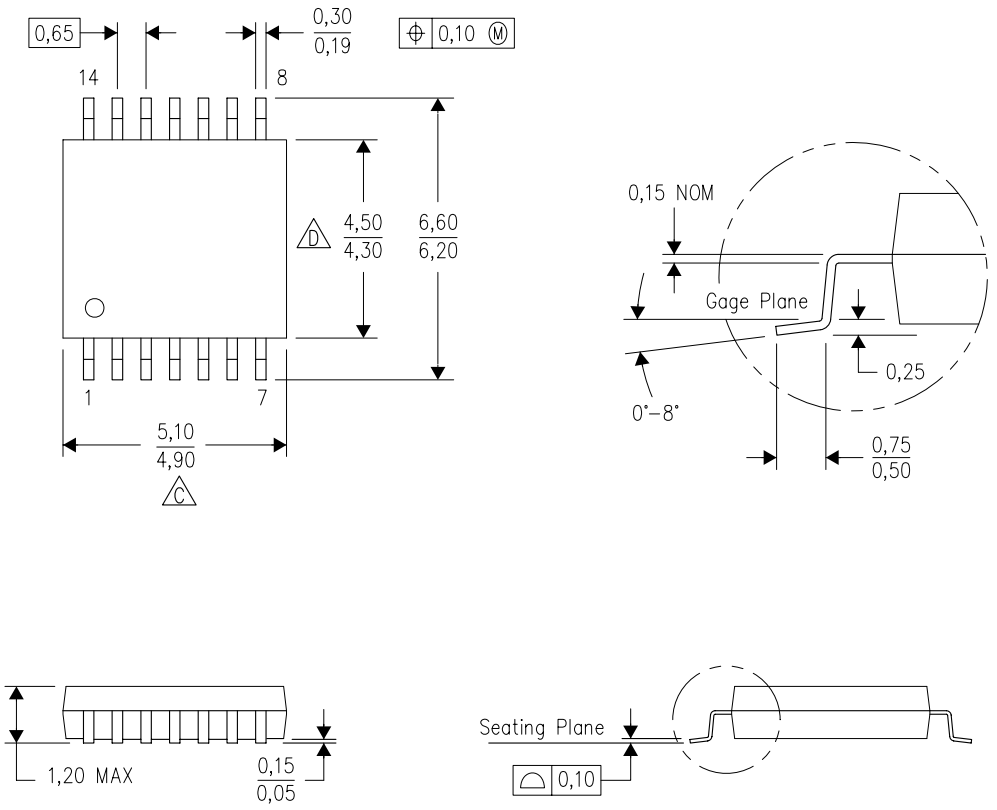
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

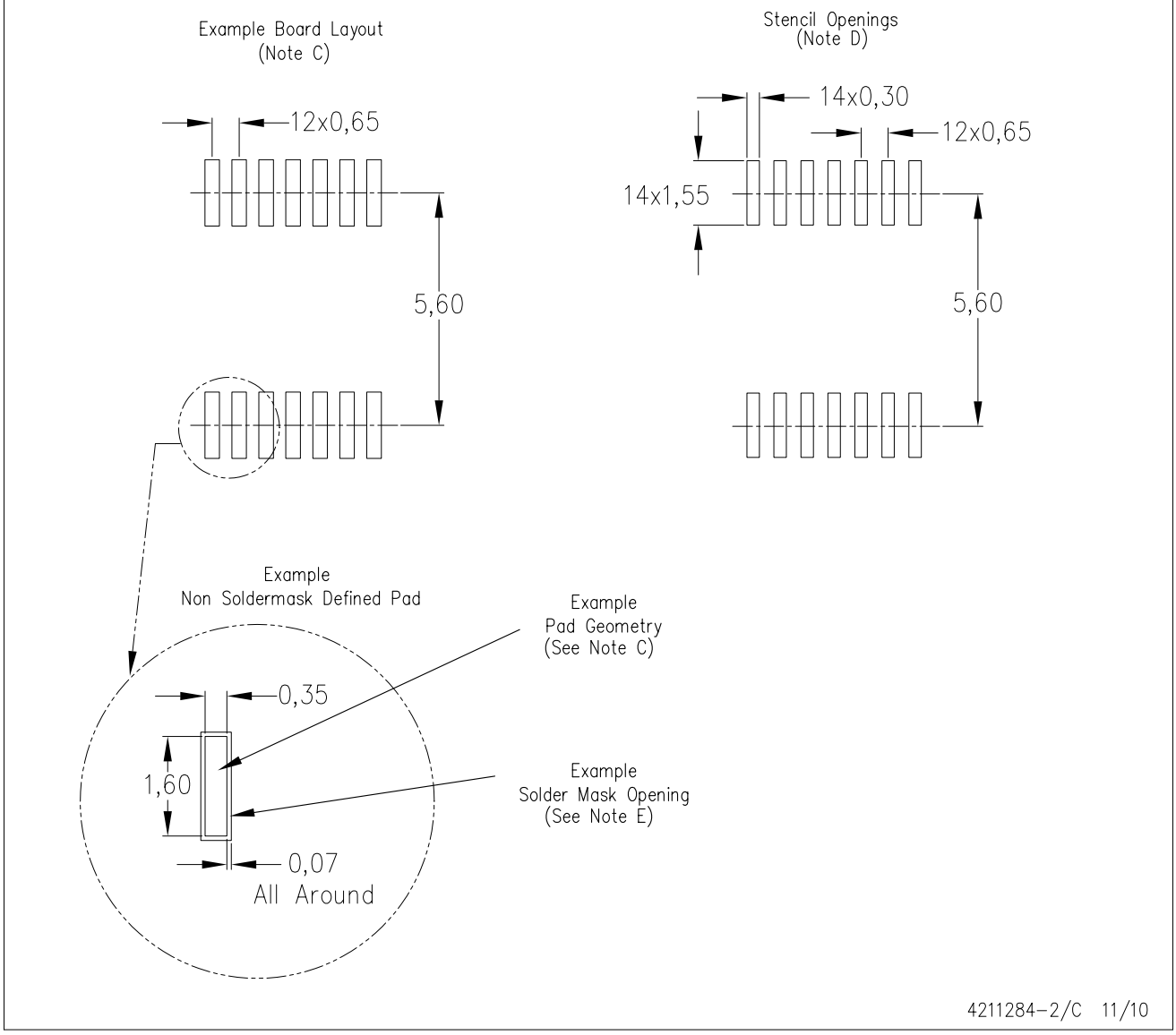
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

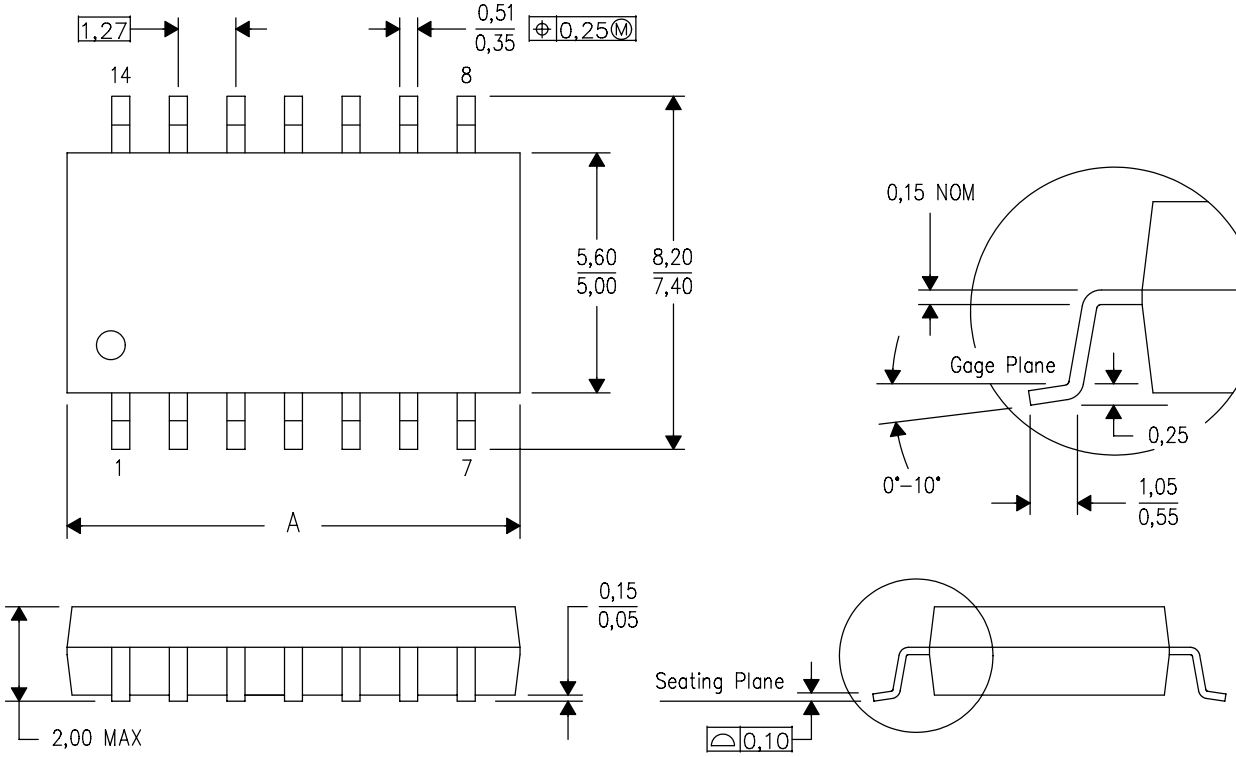


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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