User's Guide

TPS54383 Step-Down Converter Evaluation Module User's Guide

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1 Introduction

The TPS54383EVM evaluation module (EVM) is a dual non-synchronous buck converter providing fixed 5.0-V and 3.3-V output at up to 2 A each from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS54383 Dual Non-Synchronous Buck Converter with Integral High-Side FET.

1.1 Description

TPS54383EVM is designed to use a regulated 12-V (+10% / -20%) bus to produce two regulated power rails, 5.0 V and 3.3 V at up to 2 A of load current each. TPS54383EVM is designed to demonstrate the TPS54383 in a typical 12-V bus system while providing a number of test points to evaluate the performance of the TPS54383 in a given application. The EVM can be modified to other input or output voltages by changing some of the components.

1.2 Applications

- Non-Isolated Low Current Point of Load and Voltage bus converters
- Consumer Electronics
- LCD TV
- Computer Peripherals
- Digital Set Top Box

1.3 Features

- 12-V (+10% / -20%) Input Range
- 5.0-V and 3.3-V Fixed Output Voltage, Adjustable with Resistor Change
- 2-A_{DC} Steady State Output Current (3 A Peak)
- 300-kHz Switching Frequency (fixed by TPS54383)
- Internal Switching MOSFET and External Rectifier Diode
- Double Sided 2 Active Layer PCB (all components on top side, test point signals routed on internal layers)
- Active Converter Area (less than 2.5 square inch < 1.15” x 2.15”)
- Convenient Test Points (used for probing switching waveforms and non-invasive loop response testing)

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2 TPS54383EVM Electrical Performance Specifications

Table 2-1. Electrical Performance Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Characterstics						
V_{IN}	Input coltage		9.6	12	13.2	V
I_{IN}	Input current	V_{IN} = nom, I_{OUT} = max	-	1.6	2.0	A
	No load input current	V_{IN} = nom, I_{OUT} = 0 A	-	12	20	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = min to max	4.0	4.2	4.4	V
Output Characterstics						
V_{OUT1}	Output voltage 1	V_{IN} = nom, I_{OUT} = nom	4.85	5.0	5.15	V
V_{OUT2}	Output voltage 2	V_{IN} = nom, I_{OUT} = nom	3.20	3.3	3.40	
	Line regulation	V_{IN} = min to max	-	-	1%	
	Load regulation	IOUT = min to max	-	-	1%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = nom, I_{OUT} = max	-	-	50	mV_{pp}
I_{OUT1}	Output current 1(1)	V_{IN} = min to max	0		2.0	A
I_{OUT2}	Output current 2(1)	V_{IN} = min to max	0		2.0	
I_{OCP1}	Output over current Channel 1	V_{IN} = nom, V_{OUT} = V_{OUT1} - 5%	3.1	3.7	4.5	
I_{OCP2}	Output over current Channel 2	V_{IN} = nom, V_{OUT} = V_{OUT2} - 5%	3.1	3.7	4.5	
Systems Characterstics						
F_{SW}	Switching frequency		255	310	375	kHz
ηpk	Peak efficiency	V_{IN} = nom	-	90%	-	
η	Full load efficiency	V_{IN} = nom, I_{OUT} = max	-	85%	-	
Top	Operating temperature range	V_{IN} = min to max, I_{OUT} = min to max	0	25	60	°C

(1) Recommended Load Current limited to 2 A to prevent rectifier diodes surface temperature from exceeding 65°C.

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3 Schematic

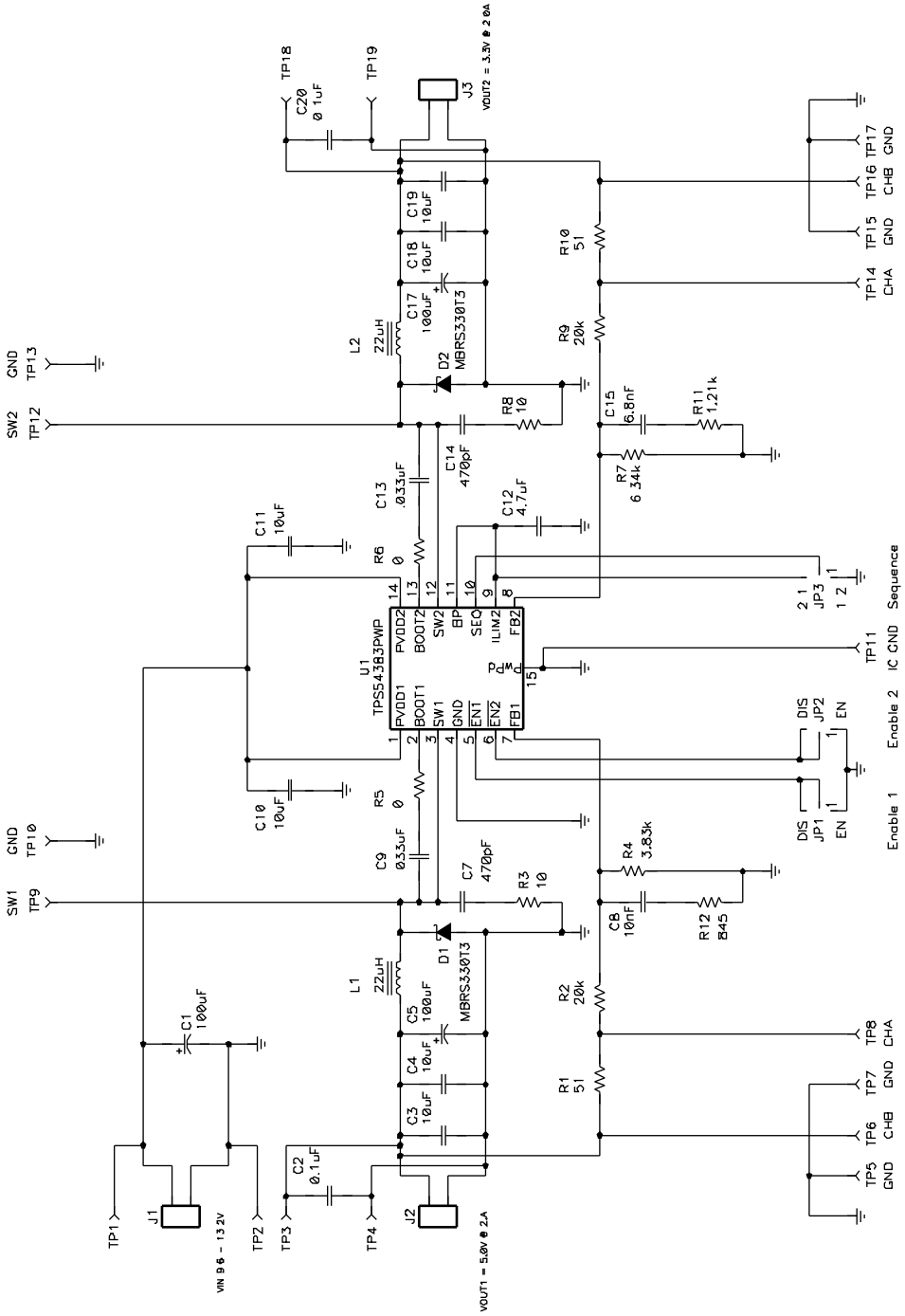

Figure 3-1. TPS54383EVM Schematic

Note

For reference only, see Table 7-1, List of Materials for specific values.

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3.1 Sequencing Jump (JP3)

The TPS54383EVM provides a 3-pin, 100-mil header and shunt for programming the TPS54383's sequencing function. Placing the JP3 shunt in the left position connects the sequence pin to BP and sets the TPS54383 controller to sequence Channel 2 prior to Channel 1 when Enable 2 is activated. Placing the JP3 shunt in the right position connects the sequence pin to GND and sets the TPS54383 converter to sequence Channel 1 prior to Channel 1 when Enable 1 is activated. Removing the JP3 shunt disables sequencing and allows Channel 1 and Channel 2 to be enabled independently.

3.2 Enable Jumpers (JP1 and JP2)

TPS54383EVM provides separate 3-pin, 100-mil headers and shunts for exercising the TPS54383 Enable functions. When JP3 is removed placing the JP1 shunt in the left position connects EN1 to ground and turns on Output 1 and placing the JP2 shunt in the left position connects EN2 to ground and turns on Output 2.

When the JP3 shunt is in the LEFT position, placing the JP2 shunt in the left position connects EN2 to ground and turns on first Output 2 and then Output 1.

When the JP3 shunt is in the RIGHT position, placing the JP1 shunt in the left position connects EN1 to ground and turns on first Output 1 and then Output 2.

3.3 Test Point Descriptions

Table 3-1. Test Point Descriptions

Test Point	Lable	Use	Section
TP1	VIN	Monitor input voltage	Section 3.3.1
TP2	GND	Ground for input voltage	Section 3.3.1
TP3	VOUT1	Monitor VOUT1 Voltage	Section 3.3.2
TP4	GND	Ground for VOUT1 voltage	Section 3.3.2
TP5	GND	Ground for Channel B loop monitoring	Section 3.3.3
TP6	CHB	Channel B for loop monitoring	Section 3.3.3
TP7	GND	Ground for Channel A loop monitoring	Section 3.3.3
TP8	CHA	Channel A for loop monitoring	Section 3.3.3
TP9	SW1	Monitor switching node of Channel 1	Section 3.3.4
TP10	GND	Ground for switch node of Channel 1	Section 3.3.4
TP11	IC_GND	Monitor device ground	Section 3.3.5
TP12	SW2	Monitor switching node of Channel 2	Section 3.3.6
TP13	GND	Ground for switch node of Channel 2	Section 3.3.6
TP14	CHA	Channel A for loop monitoring	Section 3.3.7
TP15	GND	Ground for Channel A loop monitoring	Section 3.3.7
TP16	CHB	Channel B for loop monitoring	Section 3.3.7
TP17	GND	Ground for Channel B loop monitoring	Section 3.3.7
TP18	VOUT2	Monitor VOUT2 voltage	Section 3.3.8
TP19	GND	Ground for VOUT2 voltage	Section 3.3.8

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3.3.1 Input Voltage Monitoring (TP1 and TP2)

TPS54383EVM provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

3.3.2 Channel 1 Output Voltage Monitoring (TP3 and TP4)

TPS54383EVM provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connectors. All output voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive terminal to TP3 and negative terminal to TP4. For Output ripple measurements, TP3 and TP4 allow a user to limit the ground loop area by using the Tip and Barrel measurement technique shown in Figure 4-2. All output ripple measurements should be made using the Tip and Barrel measurement.

3.3.3 Channel 1 Loop Analysis (TP5, TP6, TP7 and TP8)

TPS54383EVM contains a 51-Ω series resistor (R1) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30 mV or less) signal across R1 through TP6 and TP8. By monitoring the ac injection level at TP8 and the returned ac level at TP6, the power supply loop response can be determined.

3.3.4 Channel 1 Switching Waveforms (TP9 and TP10)

TPS54383EVM provides a test point and a local ground connection (TP10) for the monitoring of the Channel 1 power stage switching waveform. Connect an oscilloscope probe to TP9 to monitor the switch node voltage for Channel 1.

3.3.5 TPS54383 Device Ground (TP11)

TPS54383EVM provides a test point for the device ground. To measure the device pin voltages, connect the ground of the oscilloscope probe to TP11.

3.3.6 Channel 2 Switching Waveforms (TP12 and TP13)

TPS54383EVM provides a test point and a local ground connection (TP13) for the monitoring of the Channel 1 power stage switching waveform. Connect an oscilloscope probe to TP12 to monitor the switch node voltage for Channel 1.

3.3.7 Channel 2 Loop Analysis (TP14, TP15, TP16 and TP17)

TPS54383EVM contains a 51-Ω series resistor (R10) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30 mV or less) signal across R10 through TP14 and TP16. By monitoring the ac injection level at TP14 and the returned ac level at TP16, the power supply loop response can be determined.

3.3.8 Output Voltage Monitoring (TP18 and TP19)

TPS54383EVM provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connector losses. All output voltage measurements should be made between TP18 and TP19. To use TP18 and TP19, connect a voltmeter positive terminal to TP18 and negative terminal to TP19. For output ripple measurements, TP18 and TP19 allow a user to limit the ground loop area by using the Tip and Barrel measurement technique shown in Figure 4-2. All output ripple measurements should be made using the Tip and Barrel measurement.

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4 Test Set Up

4.1 Equipment

4.1.1 Voltage Source

VIN: The input voltage source (VIN) should be a 0-15 V variable dc source capable of 5 A_{DC}. Connect VIN to J1 as shown in Figure 4-2.

4.1.2 Meters

- A1: 0-3 A_{DC}, ammeter
- V1: VIN, 0-15 V voltmeter
- V2: VOUT1 0-6 V voltmeter
- V3: VOUT2 0-4 V voltmeter

4.1.3 Loads

LOAD1: The Output1 Load (LOAD1) should be an electronic constant current mode load capable of 0-2 A_{DC} at 5.0 V

LOAD2: The Output2 Load (LOAD2) should be an electronic constant current mode load capable of 0-2 A_{DC} at 3.3 V

4.1.4 Oscilloscope

Oscilloscope: A digital or analog oscilloscope can be used to measure the ripple voltage on VOUT. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP3 and TP4 or TP18 and TP19 can be used to measure the output ripple voltages by placing the oscilloscope probe tip through TP3 or TP18 and holding the ground barrel to TP4 or TP19 as shown in Figure 4-2. For a hands free approach, the loop in TP4 or TP19 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

VIN to J1: The connection between the source voltage, VIN and J1 of HPA241 can carry as much as 5 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD1: The power connection between J2 of HPA241 and LOAD1 can carry as much as 2 A_{DC}. The minimum recommended wire size is AWG #18, with the total length of wire less than 2 feet (1 foot output, 1 foot return).

J3 to LOAD2: The power connection between J3 of HPA241 and LOAD2 can carry as much as 2 A_{DC}. The minimum recommended wire size is AWG #18, with the total length of wire less than 2 feet (1 foot output, 1 foot return).

4.1.6 Other

Fan: This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is recommended to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

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4.2 Equipment Setup

Shown in Figure 4-1 is the basic test set up recommended to evaluate the TPS54383EVM. Please note that although the return for J1, J2 and JP3 are the same system ground, the connections should remain separate as shown in Figure 4-1

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, VIN, it is advisable to limit the source current from VIN to 5.0 A maximum. Make sure VIN is initially set to 0 V and connected as shown in Figure 4-1.
3. Connect the ammeter A1 (0-5 A range) between VIN and J1 as shown in Figure 4-1.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 4-1.
5. Connect LOAD1 to J2 as shown in Figure 4-1. Set LOAD1 to constant current mode to sink 0 A_{DC} before VIN is applied.
6. Connect voltmeter, V2 across TP3 and TP4 as shown in Figure 4-1.
7. Connect LOAD2 to J3 as shown in Figure 4-1. Set LOAD2 to constant current mode to sink 0 A_{DC} before VIN is applied.
8. Connect voltmeter, V3 across TP18 and TP19 as shown in Figure 4-1.
9. Place fan as shown in Figure 4-1 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

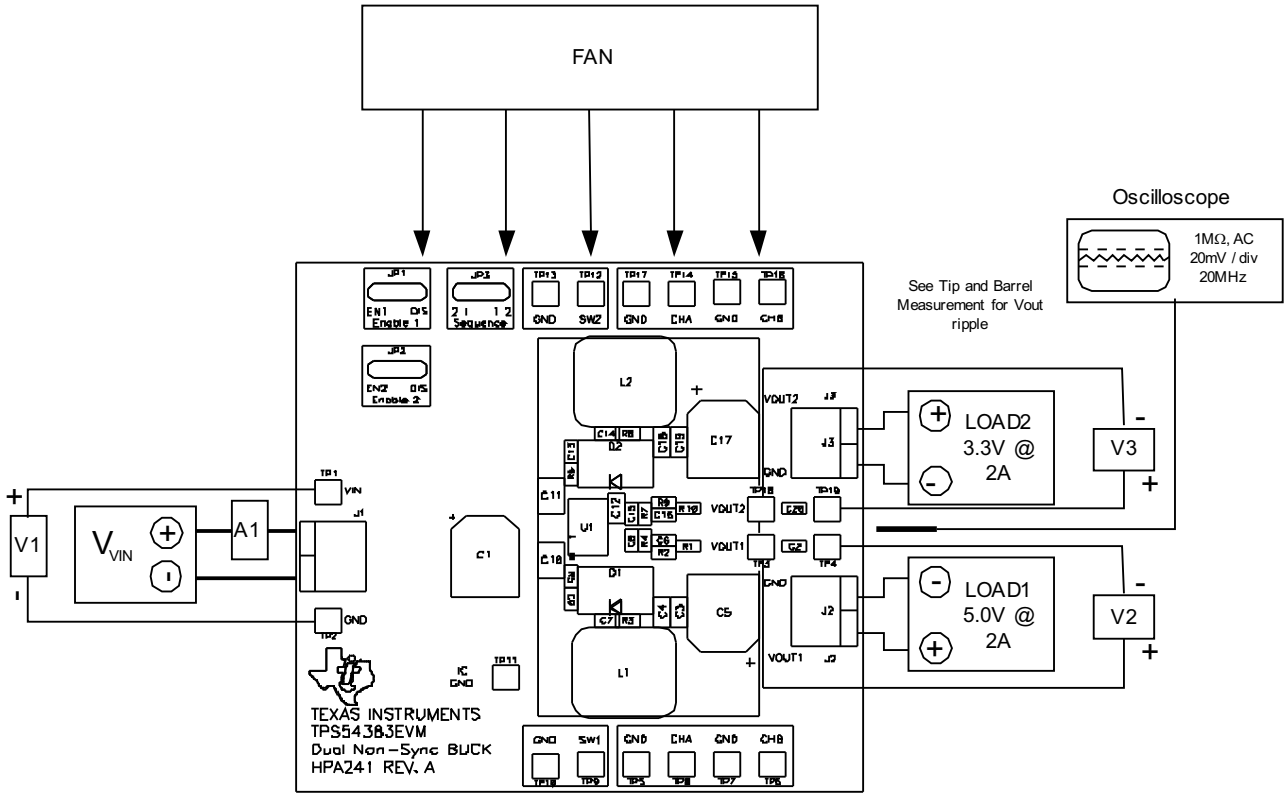

Figure 4-1. TPS54383EVM Recommended Test Set-Up

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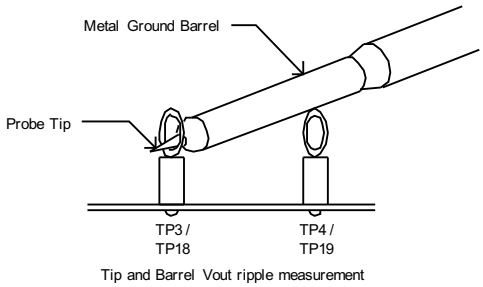

Figure 4-2. Tip and Barrel Measurement Technique (output ripple measurement using TP3 and TP4 or TP18 and TP19)

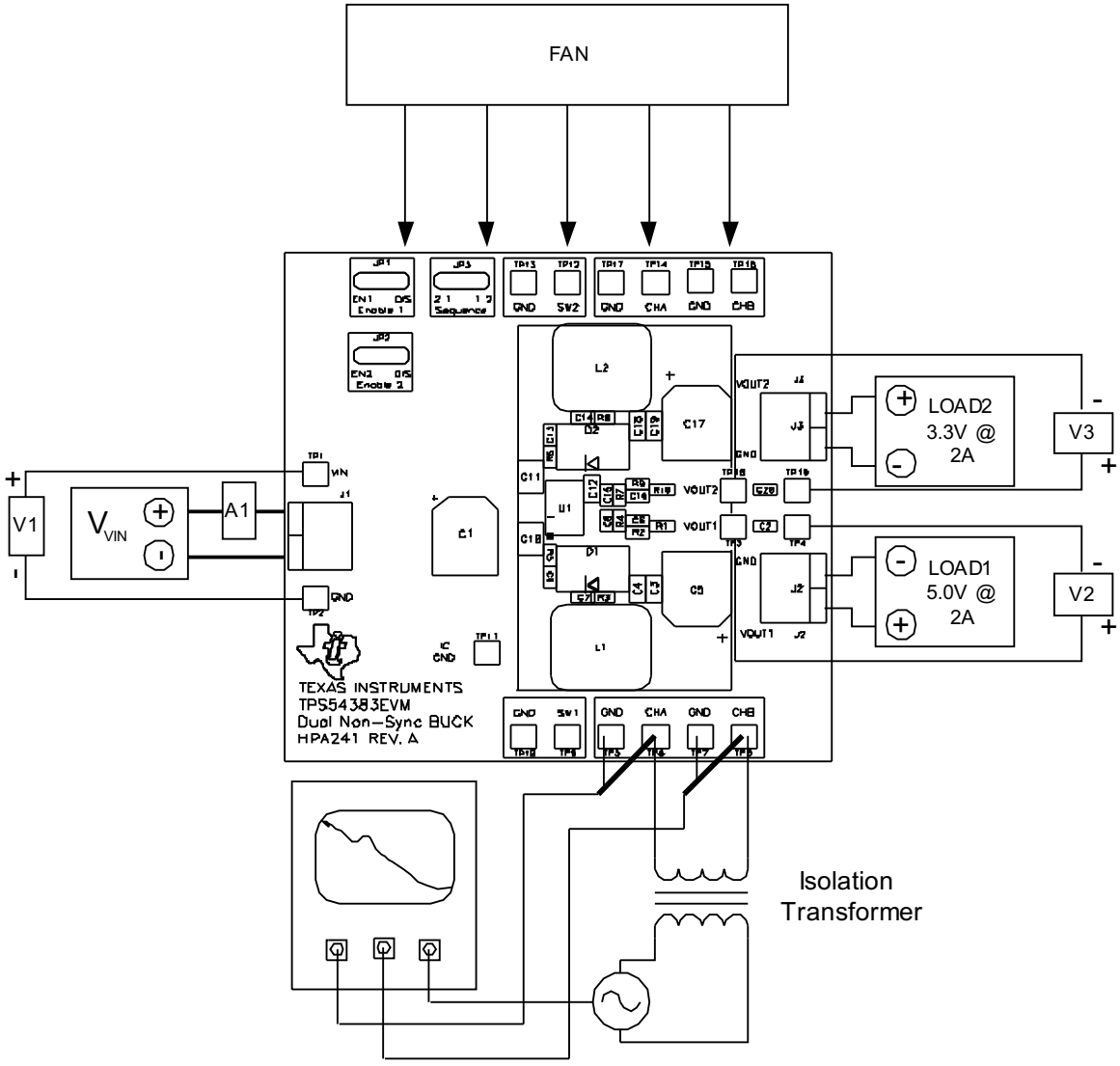

Figure 4-3. Control Loop Measurement Setup

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4.3 Start Up / Shut Down Procedure

1. Increase VIN from 0 V to 12 V_{DC}.
2. Vary LOAD1 from 0 – 2 A_{DC}
3. Vary LOAD2 from 0 – 2 A_{DC}
4. Vary VIN from 9.6 V_{DC} to 13.2 V_{DC}
5. Decrease VIN to 0 V_{DC}
6. Decrease LOAD1 to 0 A.

4.4 Output Ripple Voltage Measurement Procedure

1. Increase VIN from 0 V to 12 V_{DC}.
2. Adjust LOAD1 to desired load between 0 A_{DC} and 2 A_{DC}.
3. Adjust VIN to desired load between 9.6 V_{DC} and 13.2 V_{DC}.
4. Connect oscilloscope probe to TP3 and TP4 or TP18 and TP19 as shown in Figure 4-2.
5. Measure output ripple.
6. Decrease VIN to 0 V_{DC}.
7. Decrease LOAD1 to 0 A.

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1 kHz to 1 MHz isolation transformer to TP6 and TP8 as show in Figure 4-3.
2. Connect input signal amplitude measurement probe (Channel A) to TP8 as shown in Figure 4-3.
3. Connect output signal amplitude measurement probe (Channel B) to TP6 as shown in Figure 4-3.
4. Connect ground lead of Channel A and Channel B to TP5 & TP7 as shown in Figure 4-3.
5. Inject 30 mV or less signal across R1 through isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz with 10 Hz or lower post filter.
7. Control loop gain can be measured by:

$$20 \times LOG\left(\frac{ChannelB}{ChannelA}\right)$$

8. Control loop phase is measured by the phase difference between Channel A and Channel B.
9. Control loop for Channel 2 can be measured by making the following substitutions.
   a. Change TP6 to TP16
   b. Change TP8 to TP14
   c. Change TP5 to TP17
   d. Change TP7 to TP15
10. Disconnect isolation transformer before making any other measurements (signal injection into feedback may interfere with accuracy of other measurements).

4.6 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down VIN
3. Shut down LOAD1
4. Shut down fan

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5 TPS54383EVM Typical Performance Data and Characteristic Curves

Figure 5-1 through Figure 5-5 present typical performance curves for the TPS54383EVM. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

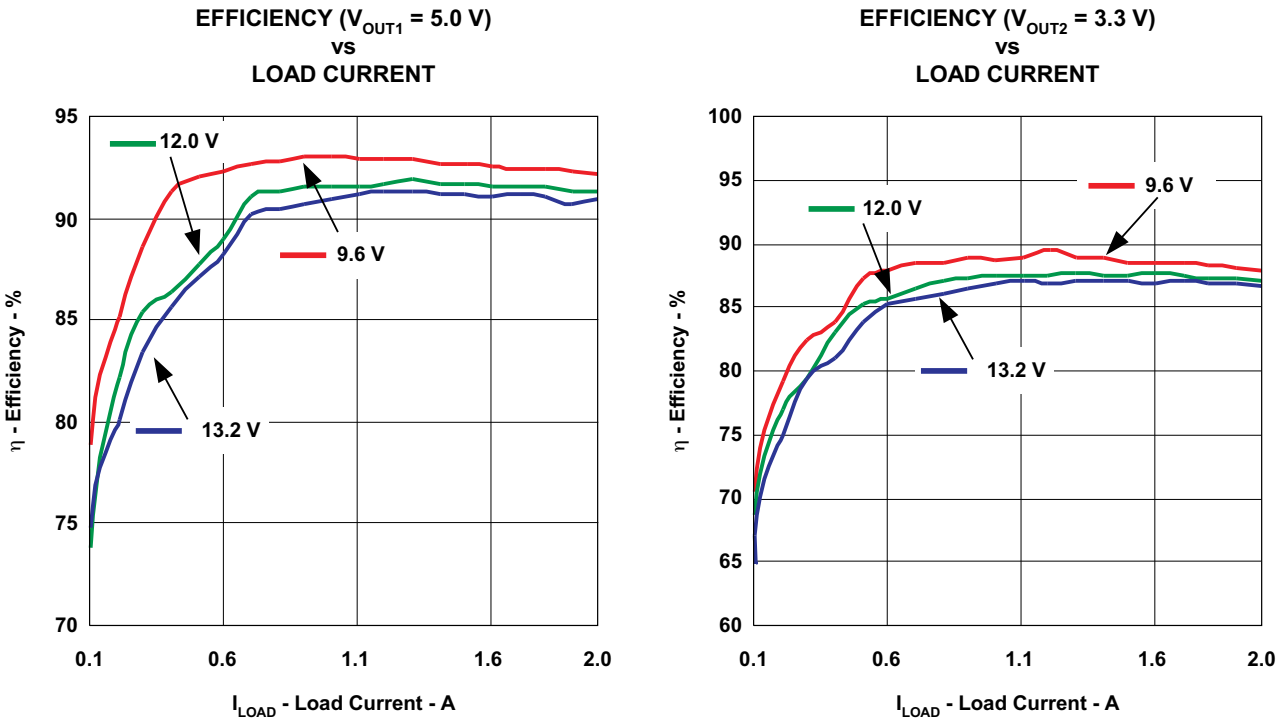

Figure 5-1. TPS54383EVM Efficiency verse Load Current V_{IN} =9.6-13.2 V, V_{OUT1} = 5.0 V I_{OUT1} = 0-2 A, V_{OUT2} = 3.3 V I_{OUT2} = 0-2 A

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5.2 Line and Load Regulation

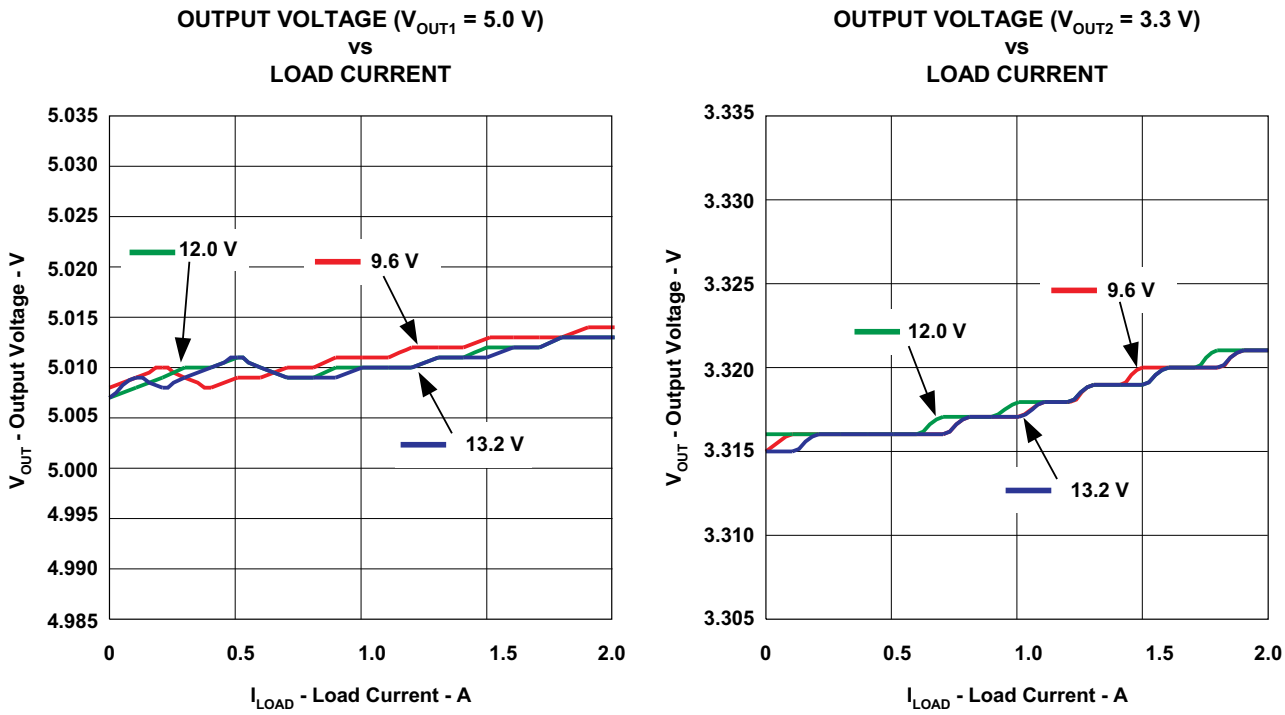

Figure 5-2. TPS54383EVM Output Voltage verse Load Current V_{IN} =9.6-13.2 V, V_{OUT1} = 5.0 V I_{OUT1} = 0-2 A, V_{OUT2} = 3.3 V I_{OUT2} = 0-2 A

5.3 Output Voltage Ripple

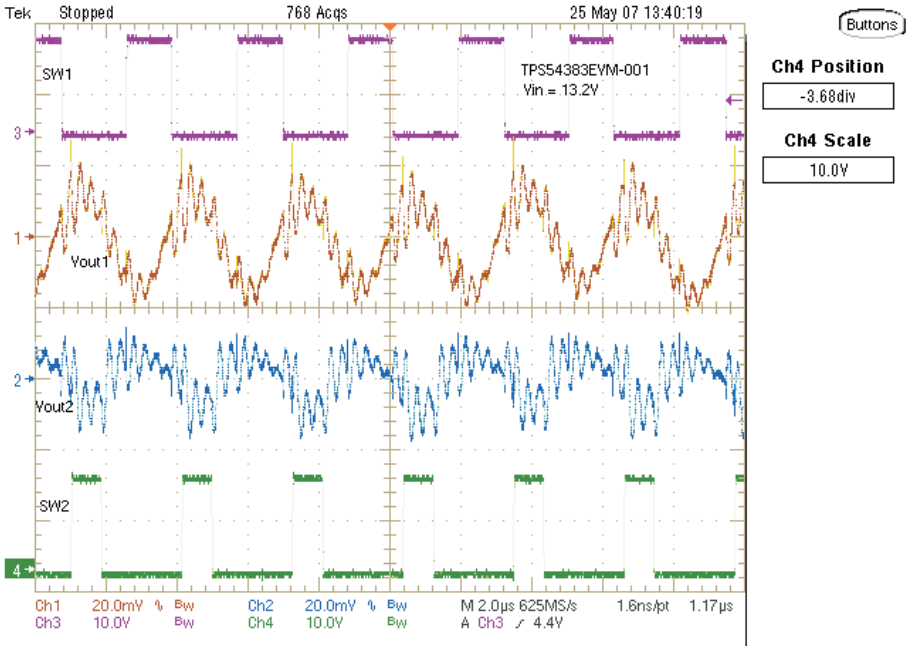

Figure 5-3. TPS54383EVM Output Voltage Ripple (V_{IN} = 13.2 V, I_{OUT1} = I_{OUT2} = 2 A)

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5.4 Switch Node

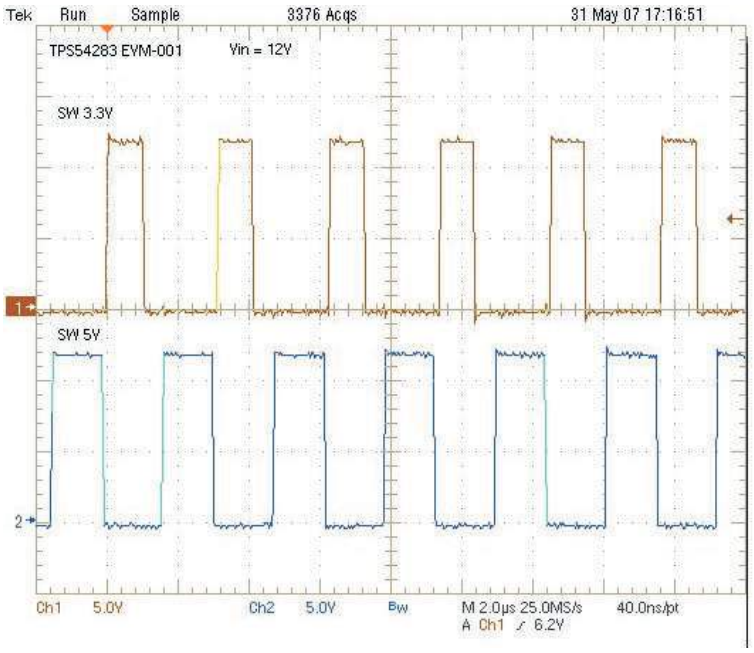

Figure 5-4. TPS54383EVM Switching Waveforms V_{IN} = 12 V, I_{OUT} = 2 A Ch1: TP9 (SW1), Ch2: TP12 (SW2)

5.5 Control Loop Bode Plot (low line, V_{IN} = 8 V)

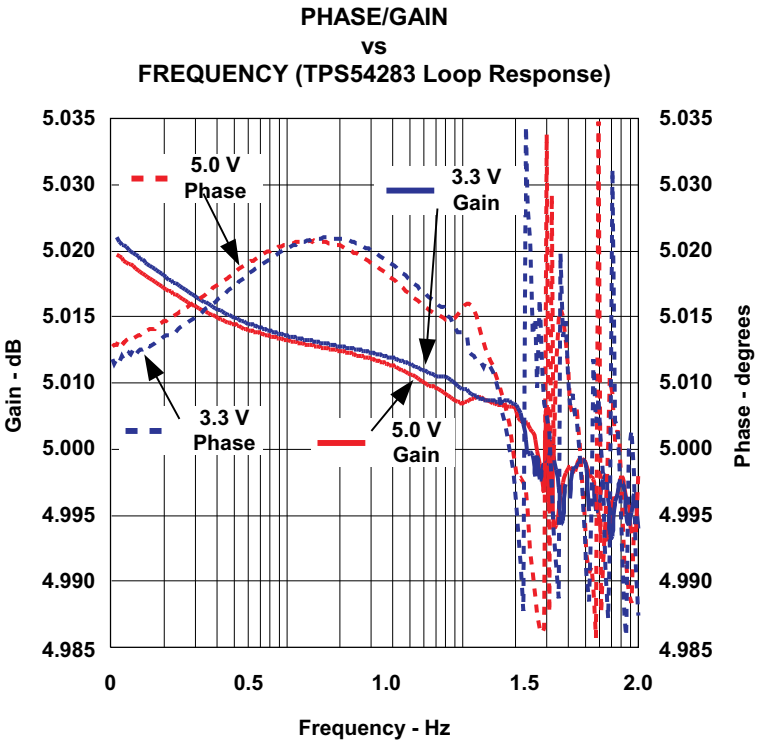

Figure 5-5. TPS54383EVM Gain and Phase vs Frequency

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5.6 Light Load Operation (revision A PCB only)

Under light load operation the TPS54383 controller can enter a pulse skipping mode when the inductor current falls below 800 mA. Under this mode of operation the output ripple voltage will increase. Table 5-1 shows the typical output ripple over the range of light load currents.

Table 5-1. Output Voltage Ripple verse Load Current at Light Load

LOAD CURRENT (A)	V_{OUT1} RIPPLE (mV)	V_{OUT2} RIPPLE (mV)	PULSE SKIPPING (Yes/No)
0.0	105	61	Yes
0.1	94	72	Yes
0.2	120	75	Yes
0.3	136	92	Yes
0.4	117	94	Yes
0.5	34	20	No
0.6	26	18	No
0.7	28	19	No
0.8	28	21	No
0.9	29	22	No
1.0	29	22	No

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6 EVM Assembly Drawings and Layout

The following figures (Figure 6-1 through Figure 6-6) show the design of the TPS54383EVM printed circuit board. The EVM has been designed using a 4-Layer, 2-oz copper-clad circuit board 3.0” x 3.0” with all components in a 1.15” x 2.15” active area on the top side and all active traces to the top and bottom layers to allow the user to easily view, probe and evaluate the TPS54383 control device in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

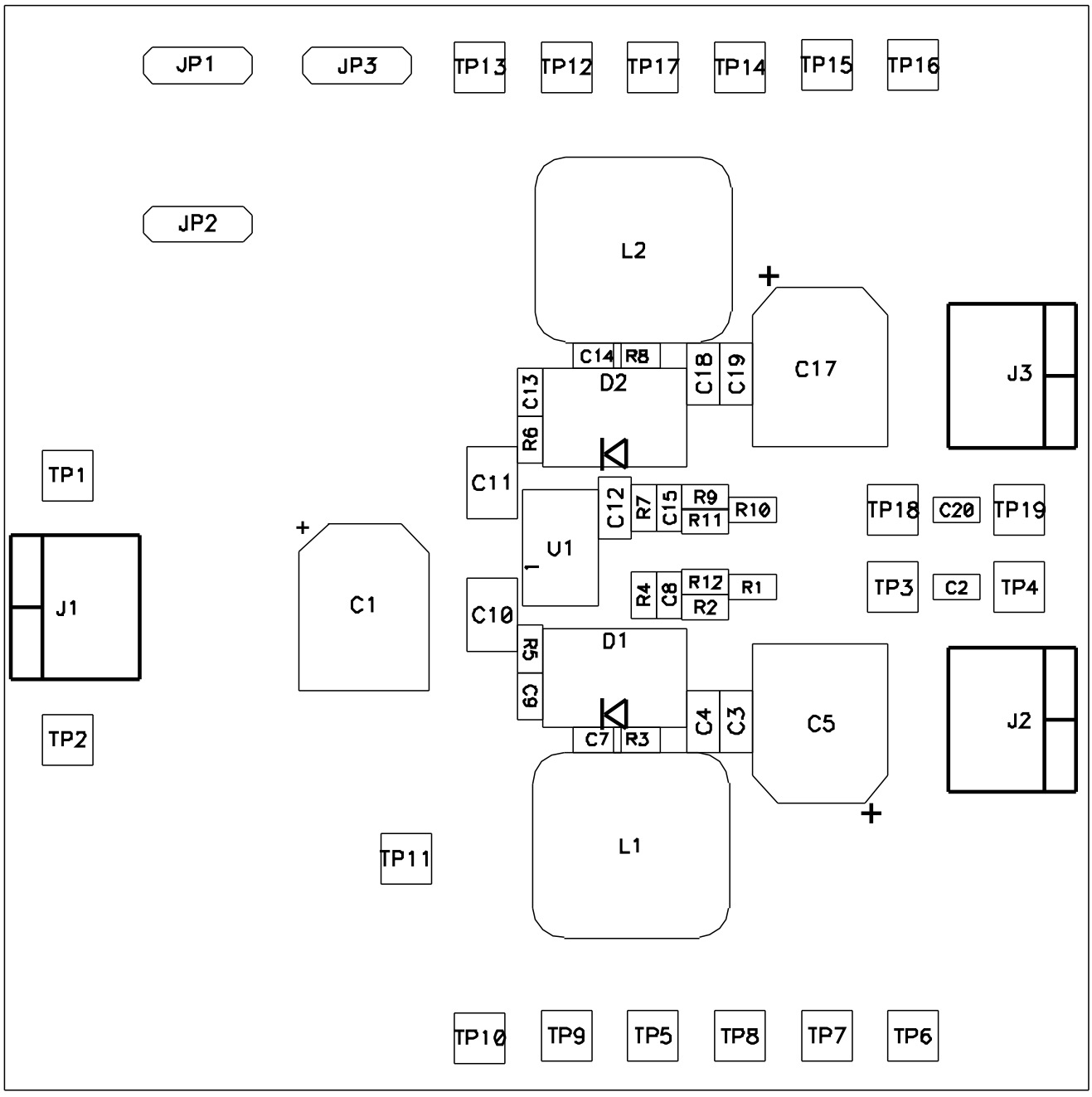

Figure 6-1. TPS54383EVM Component Placement (viewed from top)

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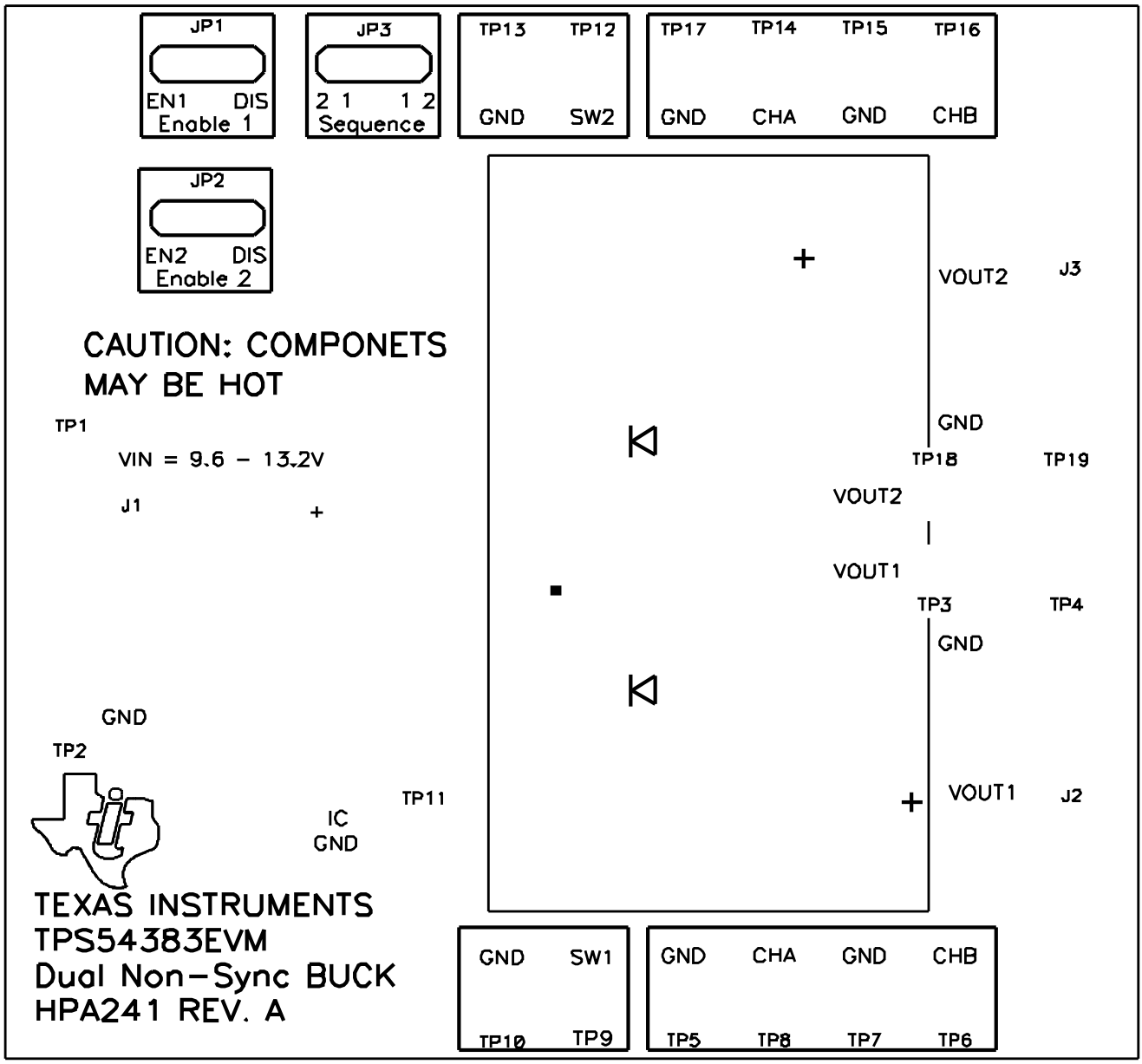

Figure 6-2. TPS54383EVM Silkscreen (viewed from top)

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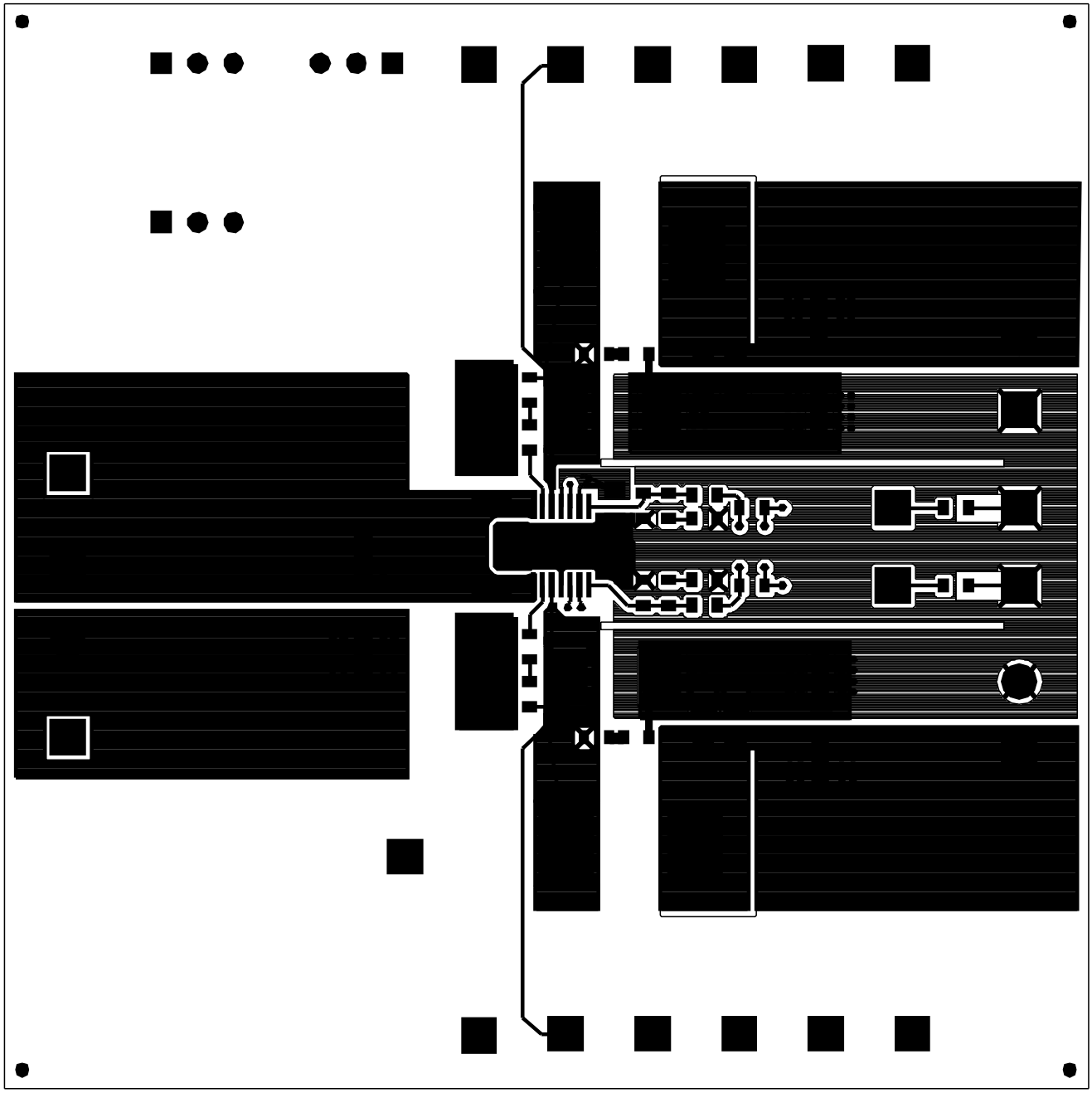

Figure 6-3. TPS54383EVM Top Copper (viewed from top)

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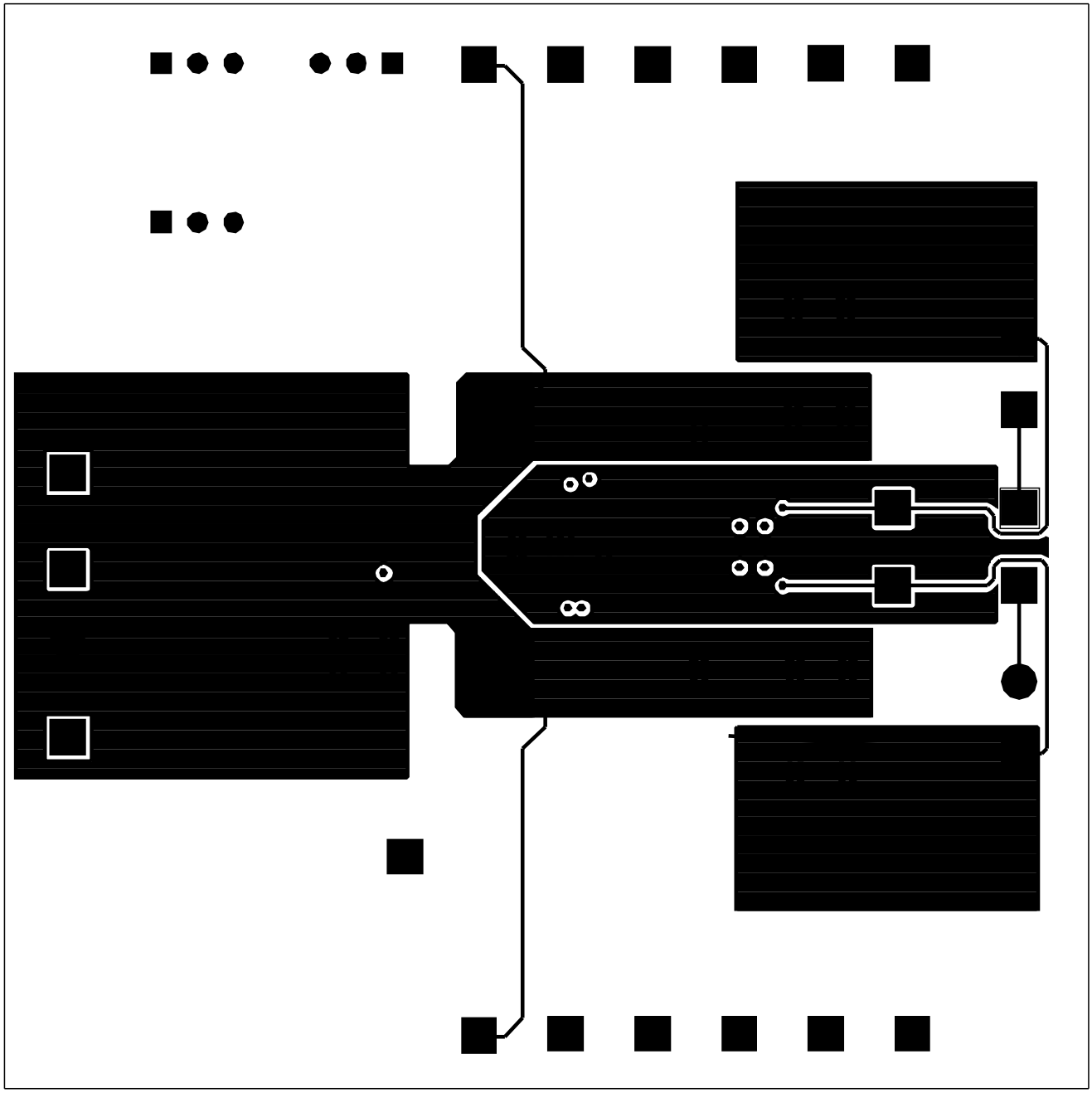

Figure 6-4. TPS54383EVM Bottom Copper (x-ray view from top)

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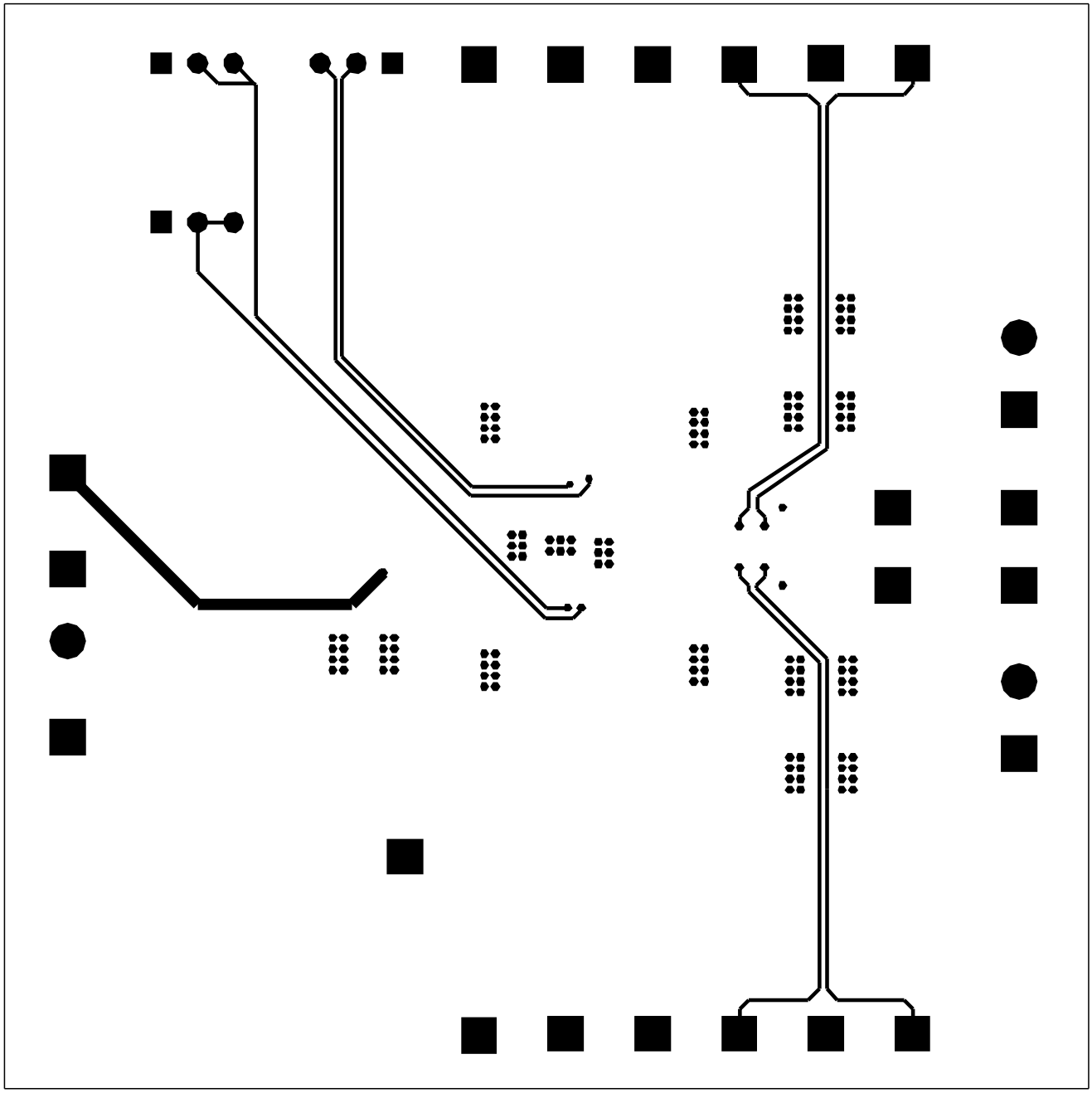

Figure 6-5. TPS54383EVM Internal 1 (x-ray view from top)

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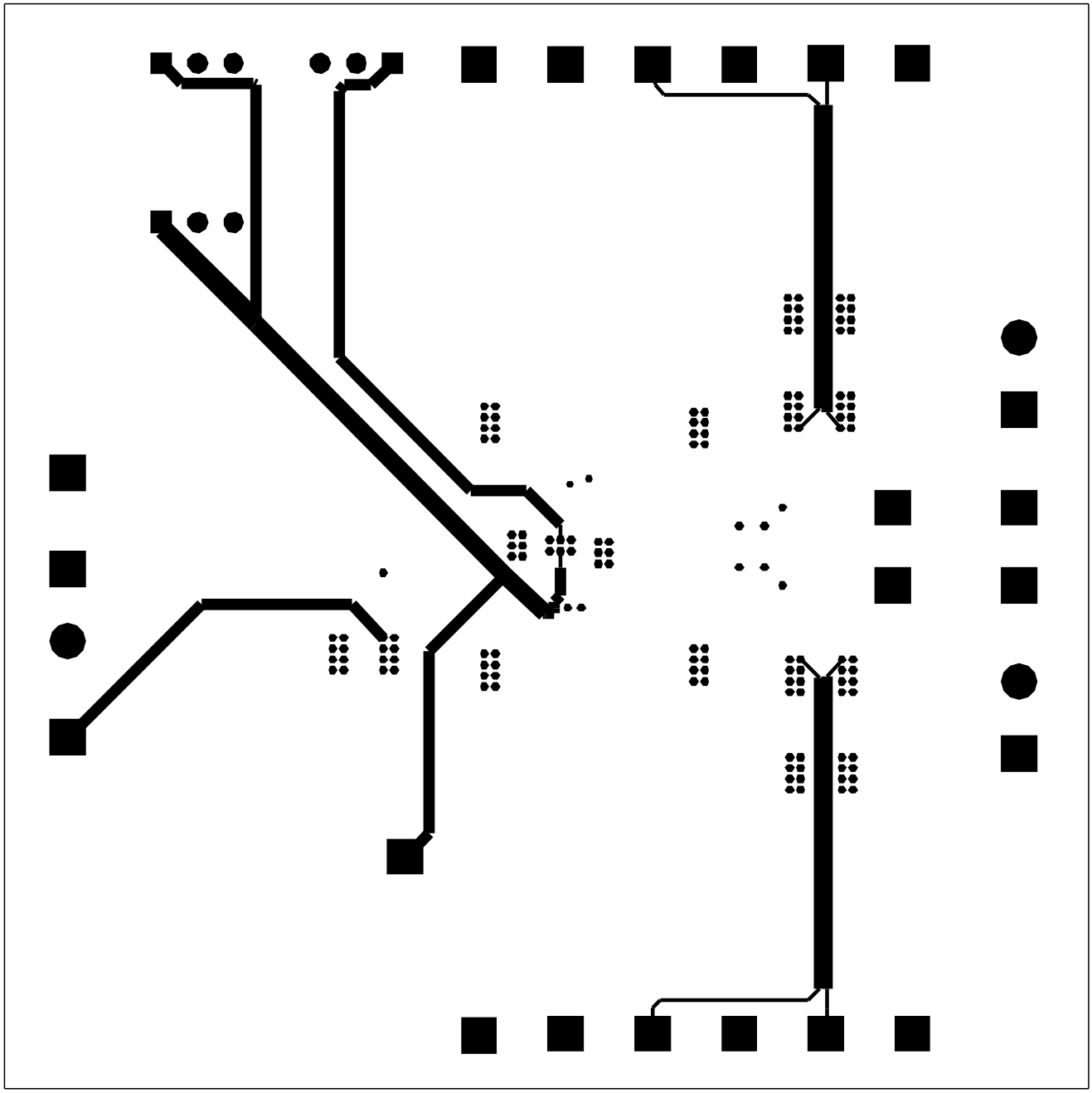

Figure 6-6. TPS54383EVM Internal 2 (x-ray view from top)

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7 List of Materials

Table 7-1. TPS54383EVM List of Materials

QTY	REF DES	DESCRIPTION	MFR	PART NUMBER
1	C1	Capacitor, aluminum, 25 V, ±20%, 100 µF, 0.328 x 0.390 inch	Panasonic	EEEFC1E101P
2	C10, C11	Capacitor, ceramic, 25 V, X5R, 20%, 10 µF, 1210	TDK	C3216X5R1E106M
1	C12	Capacitor, ceramic, 10 V, X5R, 20%, 4.7 µF, 0805	Std	Std
1	C15	Capacitor, ceramic, 25 V, X7R, 20%, 6.8 nF, 0603	Std	Std
2	C2, C20	Capacitor, ceramic, 10 V, X7R, 20%, 0.1 µF, 0603	Std	Std
4	C3, C4, C18, C19	Capacitor, ceramic, 6.3 V, X5R, 20%, 10 µF, 0805	TDK	C2012X5R0J106M
2	C5, C17	Capacitor, aluminum, 10 V, 20%, FC series, 100 µF, 0.335 x 0.374	Panasonic	EEEFC1A101P
2	C7, C14	Capacitor, ceramic, 25 V, X7R, 20%, 470 pF, 0603	Std	Std
1	C8	Capacitor, ceramic, 25 V, X7R, 20%, 10 nF, 0603	Std	Std
2	C9, C13	Capacitor, ceramic, 25 V, X7R, 20%, .033 µF, 0603	Std	Std
2	D1, D2	Diode, Schottky, 3 A, 30 V,SMC	On Semi	MBRS330T3
3	J1, J2, J3	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35 inch	OST	ED1609
3	JP1, JP2, JP3	Header, 3 pin, 100-mil spacing, (36-pin strip), 0.100 inch x 3	Sullins	PTC36SAAN
2	L1, L2	Inductor, Power, 6.8 A, 0.038 Ω, 22 µH, 0.484 x 0.484 inch	Coilcraft	MSS1278-223ML
2	R1, R10	Resistor, chip, 1/16 W, 5%, 51 Ω, 0603	Std	Std
1	R11	Resistor, chip, 1/16 W, 1%, 1.21 kΩ, 0603	Std	Std
1	R12	Resistor, chip, 1/16 W, 1%, 845 Ω, 0603	Std	Std
2	R2, R9	Resistor, chip, 1/16 W, 1%, 20 kΩ, 0603	Std	Std
2	R3, R8	Resistor, chip, 1/16 W, 5%, 10 Ω, 0603	Std	Std
1	R4	Resistor, chip, 1/16 W, 1%, 3.83 kΩ, 0603	Std	Std
2	R5, R6	Resistor, chip, 1/16 W, 5%, 0 Ω, 0603	Std	Std
1	R7	Resistor, chip, 1/16 W, 1%, 6.34 kΩ, 0603	Std	Std
3	TP1, TP3, TP18	Test point, red, thru hole, 5010, 0.125 x 0.125 inch	Keystone	5010
9	TP2, TP4, TP5, TP7, TP10, TP13, TP15, TP17, TP19	Test point, black, thru hole, 5011, 0.125 x 0.125 inch	Keystone	5011
7	TP6, TP8, TP9, TP11, TP12, TP14, TP16	Test point, white, thru hole, 5012, 0.125 x 0.125 inch	Keystone	5012
1	U1**	IC, 300-kHz Dual Non-Sync Buck with Integrated FETs, HTSSOP-14	TI	TPS54383PWP

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2008) to Revision D (October 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 3
- Updated the user's guide title..... 3

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