SY56572XR

Low Voltage 1.2V/1.8V/2.5V CML 4:1 MUX with 1:2 FANOUT 6.4Gbps with EQUALIZATION

General Description

The SY56572XR is a fully differential, low voltage 1.2V/1.8V/2.5V CML 4:1 Mux, with input equalization, and integrated 1:2 Fanout Buffer. The SY56572XR can process clock signals as fast as 4.5GHz or data patterns up to 6.4Gbps.

The differential input includes Micrel's unique 3-pin input termination architecture that interfaces to DC-coupled 2.5V/3.3V LVPECL, 1.2V/1.8V/2.5V CML or LVDS differential signals. For AC-coupled input applications, an internal voltage reference is provided for input bias. Input voltages as small as 200mV (400mV$_{pp}$) are applied before the 9, 18 or 27-inch FR4 transmission line.

The SY56572XR operates from a 2.5V ±5% core supply and a 1.2V, 1.8V or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range

(–40°C to +85°C). The SY56572XR is part of Micrel's high-speed, Precision Edge® product line.

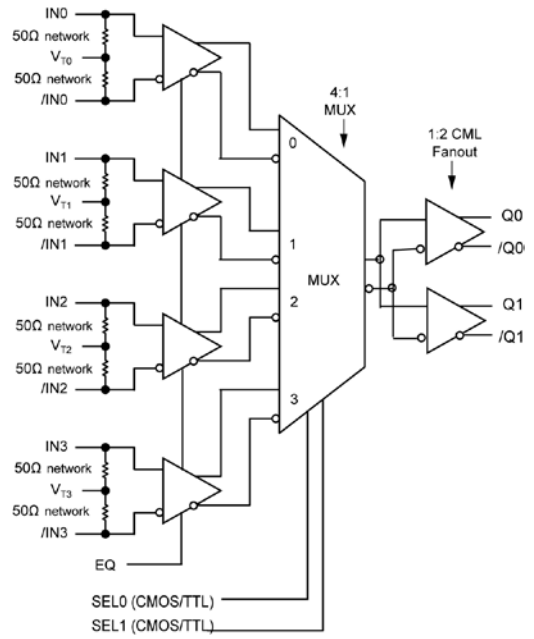
Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

- 1.2V/1.8V/2.5V CML 4:2 MUX with input equalization.
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 6.4Gbps throughput
  - <360ps propagation delay (IN-to-Q)
  - <15ps within-device skew
- Ultra-low jitter design
  - <0.8ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
- 2.5V ±5% , 1.8/1.2V ±5% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 32-pin (5mm x 5mm) QFN package

Functional Block Diagram



Applications

- Data Distribution
- SONET clock and data distribution
- Fiber Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

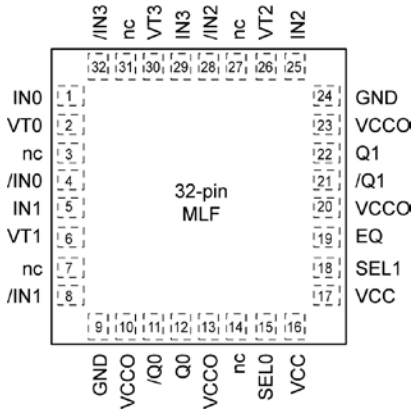
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY56572XRMG	QFN-32	Industrial	SY56572X with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY56572XRMGTR[2]	QFN-32	Industrial	SY56572X with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1,4 5,8 25,28 29,32	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3	Differential Inputs: Accepts differential signals as small as 200mV (400mV$_{PP}$) applied to the input of a 9, 18 or 27 inch 6mil FR4 stripline transmission line. See "Input and Output Stage" section for details of this input.
2 6 26 30	VT0 VT1 VT2 VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC coupling. For AC coupling, bypass VT with 0.1µF low ESR capacitor to VCC. See "Input Interface Applications" subsection and Figure 2a.
19	EQ	Three level input for equalization control.
15 18	SEL0 SEL1	Single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. Input logic threshold is VCC/2. See "Truth Table" for select control.
16,17	VCC	Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pin as possible. Supplies the input and core circuitry.
10,13,20,23	VCCO	Output Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CCO} pin as possible. Supplies the output buffers.
9,24	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
12,11 22,21	Q0, /Q0 Q1, /Q1	CML Differential Output Pair: Differential buffered copy of the input signal. The output swing is typically 390mV. See "Functional Description" subsection for termination information.

Truth Table

EQ Input	Equalization FR4 6mil Stripline
LOW	9 "
FLOAT	18"
HIGH	27"

SEL1	SEL0	
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
1	1	IN3 Input Selected

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +3.0V
Supply Voltage (V_{CCO}) ..... –0.5V to +3.0V
V_{CC} -V_{CCO} ..... <1.8V
V_{CCO} -V_{CC} ..... <0.5 V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}+0.4V
CML Output Voltage (V_{OUT}) ..... 0.6V to 3V
Current (V_T)
Source or sink on VT pin ..... ±100mA
Input Current
Source or sink Current on (IN, /IN) ..... ±50mA
Maximum operating Junction Temperature ..... 125°C
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{cc}) ..... 2.375V to 2.625V
(V_{cco}) ..... 1.14V to 2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN
Still-air (θ_{JA}) ..... 50°C/W
Junction-to-board (ψ_{JB}) ..... 20°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range	V_{CC}	2.375	2.5	2.625	V
		V_{CCO}	1.14	1.2	1.26	V
		V_{CCO}	1.7	1.8	1.9	V
		V_{CCO}	2.375	2.5	2.625	V
I_{CC}	Power Supply Current	Max. V_{CC}		110	140	mA
I_{CCO}	Power Supply Current	No Load. V_{CCO}		32	42	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.2		V_{CC}+0.4	V
V_{IL}	Input LOW Voltage (IN, /IN)	IN, /IN	0		V_{IH}–0.2	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 3a, Note 5, applied to input of transmission line.	0.2		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	See Figure 3b, Note 5, applied to input of transmission line.	0.4		2.0	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IN} (max) is specified when V_T is floating.

CML Outputs DC Electrical Characteristics[6]

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO}.
V_{CCO} = 1.7V to 1.9V, 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs.
V_{CC} = 2.375V to 2.625V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CCO}	V_{CC}-0.020	V_{CC}-0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing	See Figure 3a	300	390	475	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	600	780	950	mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = 2.375V to 2.625V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Three Level EQ Input DC Electrical Characteristics[6]

V_{CC} = 2.375V to 2.625V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}-0.3		V_{CC}	V
V_{IL}	Input LOW Voltage		0		V_{EE}+0.3	V
I_{IH}	Input HIGH Current	V_{IH} = V_{CC}			400	µA
I_{IL}	Input LOW Current	V_{IL} = GND	-480			µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO}.

V_{CCO} = 1.7V to 1.9V, 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs.

V_{CC} = 2.375V to 2.625V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	6.4			Gbps
		V_{OUT} > 200mV (Clock)	4.5			GHz
t_{PD}	Propagation Delay (IN-to-Q) (SEL-to-Q)	Note 7, Figure 1a	210	280	360	ps
		Figure 1b			1	ns
t_{Skew}	Output-to-Output Skew	Note 8		3	15	ps
	Part-to-Part Skew	Note 9			100	ps
t_{Jitter}	Data Random Jitter	Note 10			0.8	ps_{RMS}
	Data Deterministic Jitter	Note 11			10	ps_{PP}
t_R t_F	Output Rise/Fall Time (20% to 80%)	At full output swing.	30	55	85	ps
	Duty Cycle	Differential I/O	45		55	%

Notes:

7. Propagation delay is measured with no attenuating transmission line connected to the input.
8. Output-to-Output skew is the difference in time between both outputs under identical input transition, temperature and power supply
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Random jitter is additive jitter.
11. Deterministic jitter is measured with 2^{23}–1 PRBS pattern.

Functional Description

CML Output Termination with Vcco 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ωto 1.2V, not 100Ω differentially across the outputs. If AC coupling is used, Figure 5d, terminate into 50Ω to 1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage. Any unused output pair with VCCO at 1.2V needs to be terminated, do not leave floating.

CML Output Termination with VCCO 1.8V, 2.5V

For VCCO of 1.8V or 2.5V, Figure 5a/b, terminate with either 50Ω to 1.8V or 100Ω differentially across the outputs. AC-or DC-coupling is fine. For best signal integrity, terminate any unused output pairs.

Timing Diagrams

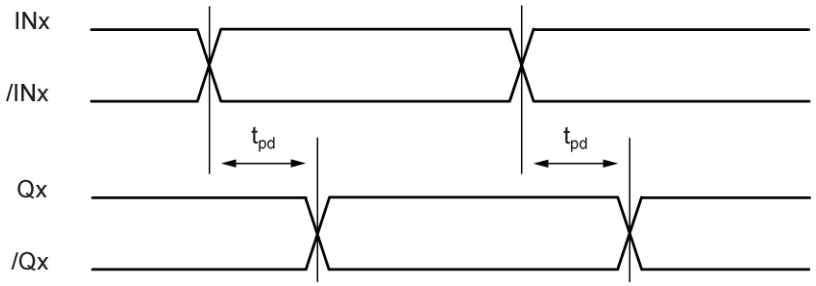


Figure 1a. IN-to-Q Timing Diagram

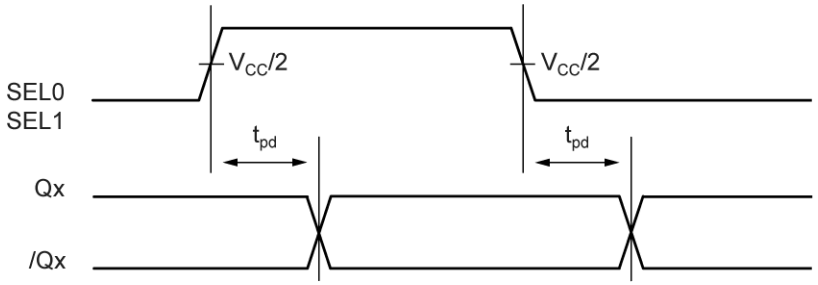


Figure 1b. SEL-to-Q Timing Diagram
(Qx state can be high or low depending on input data)

Input and Output Stage

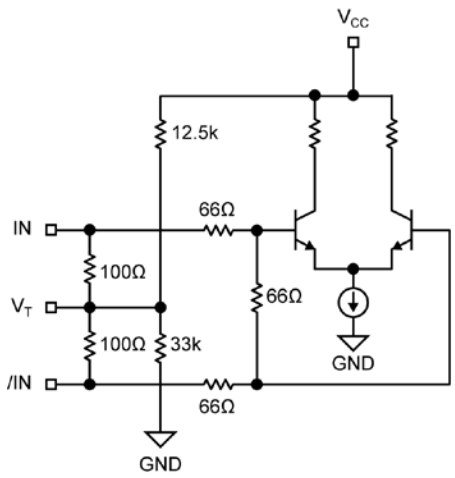


Figure 2a. Simplified Differential Input Buffer

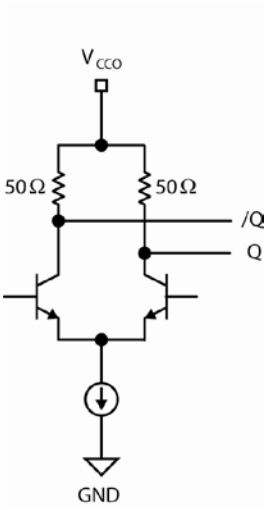


Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings

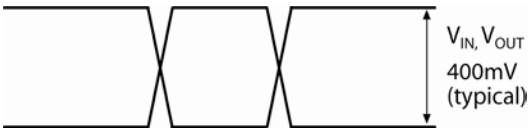


Figure 3a. Single-Ended Swing

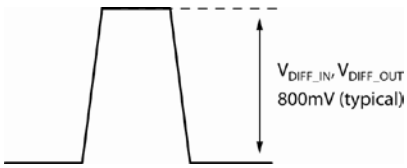


Figure 3b. Differential Swing

Input Interface Applications

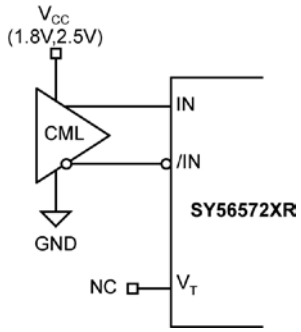


Figure 4a. CML Interface
100 Ω Differential
(DC-Coupled, 1.8V, 2.5V)

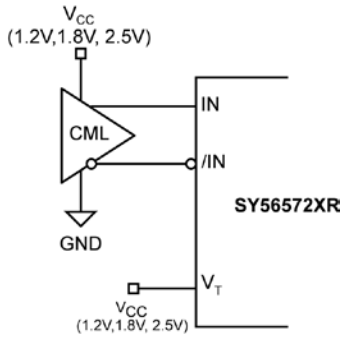


Figure 4b. CML Interface
50Ω-to-Vcc
(DC-Coupled, 1.2V,1.8V,2.5V)

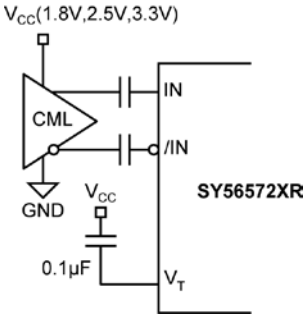


Figure 4c. CML Interface
(AC-Coupled)

***See note in Functional Description for 1.2V CML driver with AC-Coupling.**

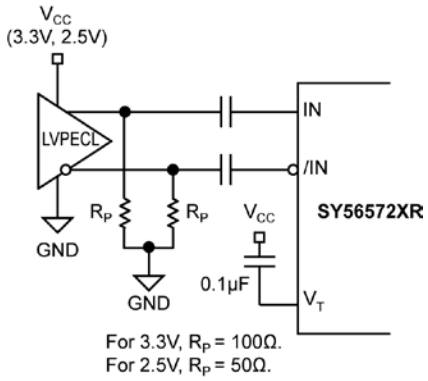


Figure 4d. LVPECL Interface
(AC-Coupled)

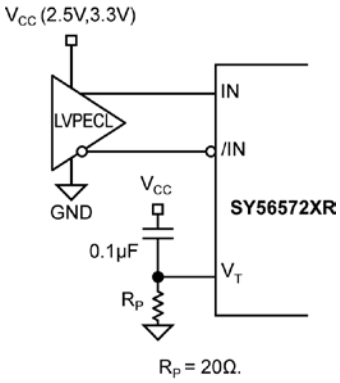


Figure 4e. LVPECL Interface
(DC-Coupled 2.5V and 3.3V)

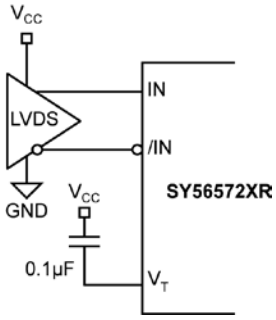


Figure 4f. LVDS Interface

CML Output Termination

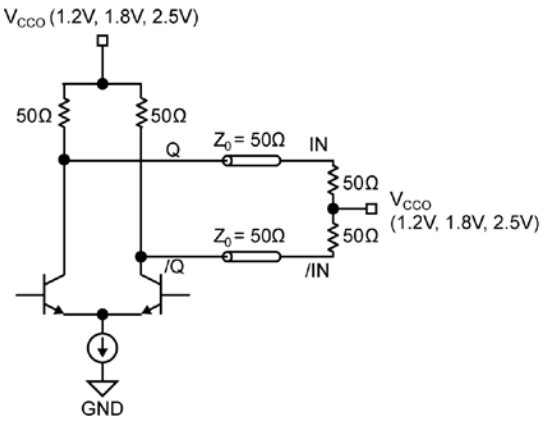


Figure 5a. 1.2V, 1.8V, 2.5V CML DC-Coupled Termination

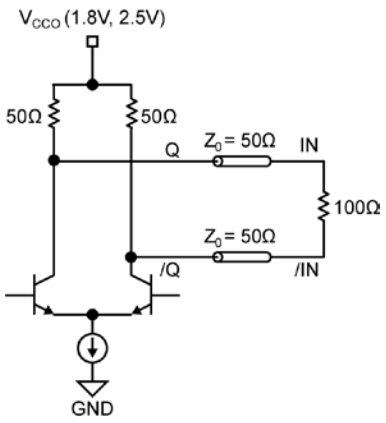


Figure 5b. 1.8V, 2.5V CML DC-Coupled Termination

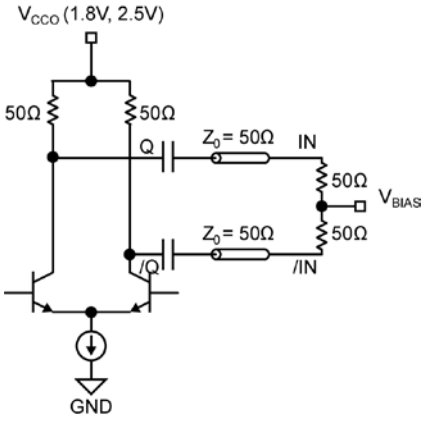


Figure 5c. CML AC-Coupled Termination.
VCCO 1.8V, 2.5V only.

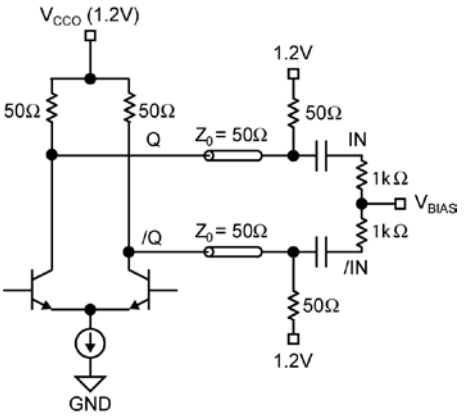
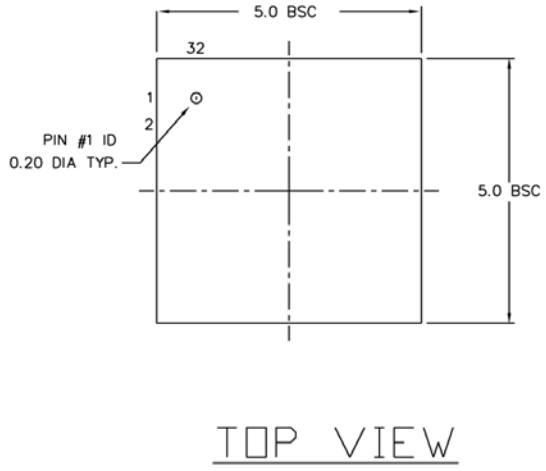
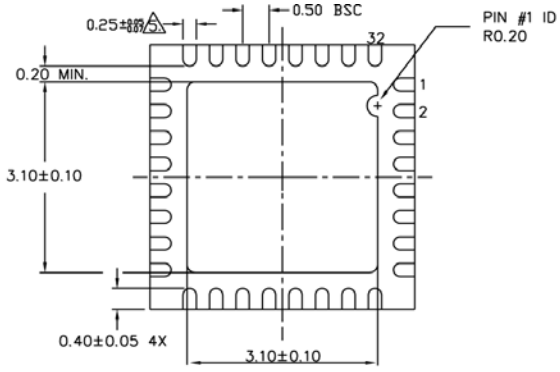


Figure 5d. CML AC-Coupled Termination.
VCCO 1.2V only.

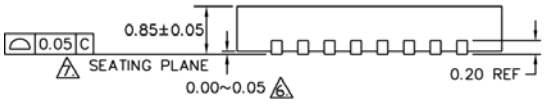
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin QFN

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