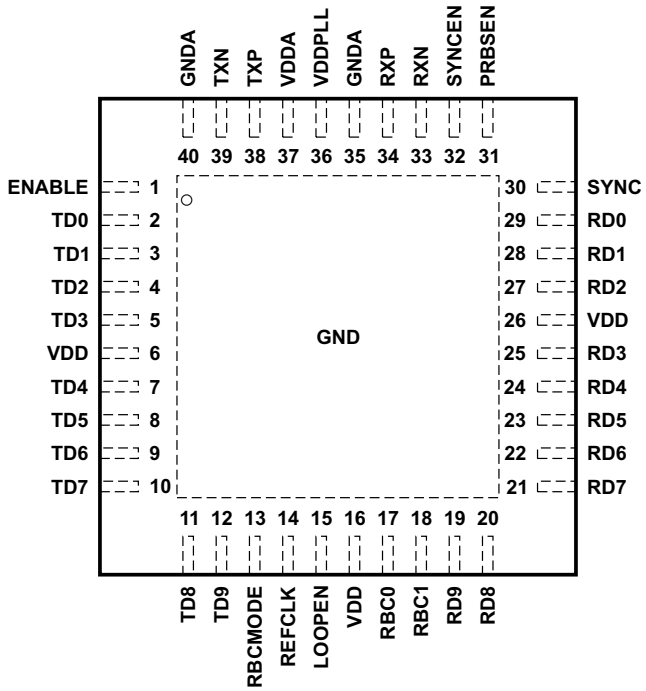
ETHERNET TRANSCEIVER

Check for Samples: TLK1221

FEATURES

- **0.6- to 1.3-Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Low Power Consumption 250 mW (typ) at 1.25 Gbps**
- **LVPECL-Compatible Differential I/O on High-Speed Interface**
- **Single Monolithic PLL Design**
- **Support For 10-Bit Interface**
- **Fast Relock Times Less Than 256 ns (typ) Suitable for EPON/GEPON Applications such as OLT and ONU Systems**
- **Receiver Differential-Input Thresholds, 200-mV Minimum**
- **Industrial Temperature Range From –40°C to 85°C**
- **IEEE 802.3 Gigabit Ethernet Compliant**
- **Designed in 0.25 µm CMOS Technology**
- **No External Filter Capacitors Required**
- **Comprehensive Suite of Built-In Testability**
- **2.5-V Supply Voltage for Lowest-Power Operation**
- **3.3-V Tolerant on LVTTL Inputs**
- **Hot Plug Protection**
- **40-Pin 6-mm × 6-mm QFN PowerPAD™ Package**

RHA Package
(Top View)



DESCRIPTION

The TLK1221 gigabit Ethernet transceiver provides for high-speed full-duplex point-to-point data transmissions. These devices are based on the timing requirements of the 10-bit interface specification by the IEEE 802.3 Gigabit Ethernet specification. The TLK1221 supports data rates from 0.6 Gbps through 1.3 Gbps.

The primary application of these devices is to provide building blocks for point-to-point baseband data transmission over controlled-impedance media of 50 Ω. The transmission media can be printed-circuit board traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The TLK1221 performs the data serialization, deserialization, and clock extraction functions for a physical layer interface device. The transceiver operates at 1.25 Gbps (typical), providing up to 1 Gbps of data bandwidth over a copper or optical media interface.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

This device supports the defined 10-bit interface (TBI). In the TBI mode, the serializer/deserializer (SERDES) accepts 10-bit wide 8b/10b parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially at PECL-compatible voltage levels. The SERDES extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte.

A comprehensive series of built-in tests is provided for self-test purposes, including loopback and pseudorandom binary sequence (PRBS) generation and verification.

The TLK1221 is housed in a high-performance, thermally enhanced, 40-pin QFN package. Use of this package does not require any special considerations except to note that the pad, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is required that the TLK1221 pad be soldered to the thermal land on the board as it serves as the main ground connection for the device.

The TLK1221 is characterized for operation from –40°C to 85°C.

This device uses a 2.5-V supply. The I/O section is 3.3-V compatible. With the 2.5-V supply, the chipset is very power-efficient, dissipating less than 200 mW typical power when operating at 1.25 Gbps.

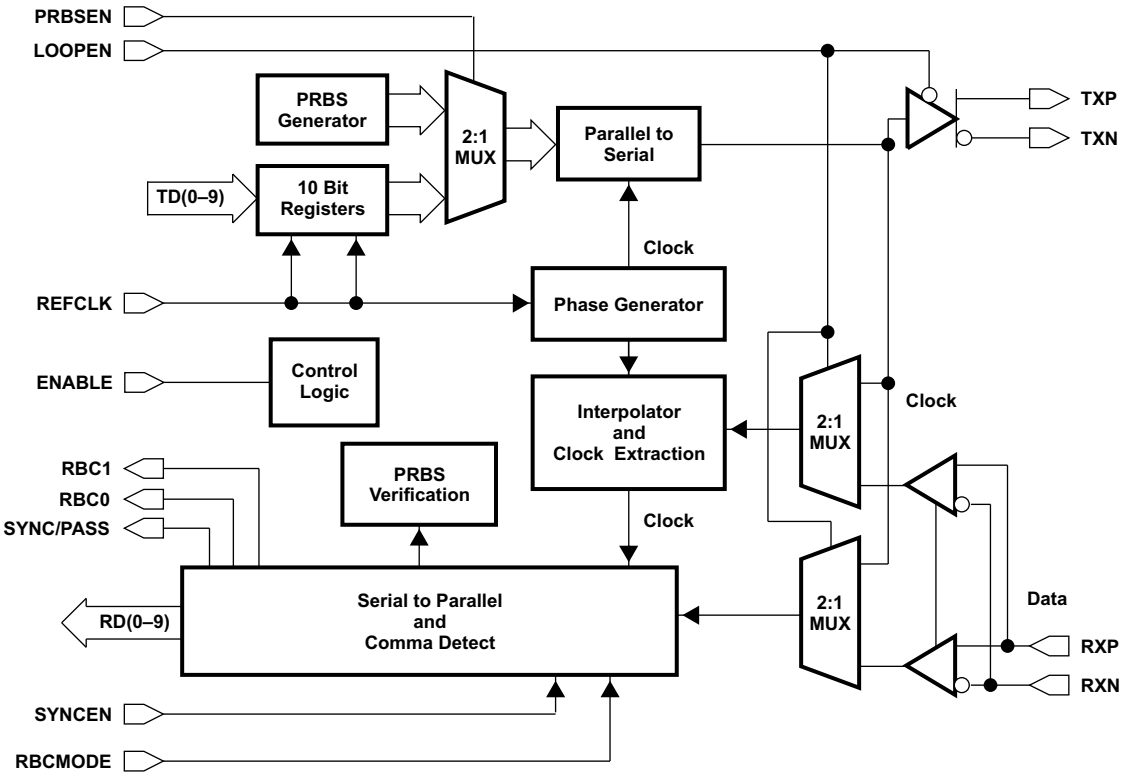
The TLK1221 is designed to be hot-plug capable. A power-on reset causes RBC0, RBC1, the parallel output signal terminals, TXP, and TXN to be held in the high-impedance state.

Differences Between TLK2201B, TLK2201BI, TLK1221, and TNETE2201

The TLK1221 is the functional equivalent of the TNETE2201. There are several differences between the devices as noted below. See Figure 12 in the application information section for an example of a typical application circuit.

- V_{CC} is 2.5 V for the TLK2201B, TLK2201BI, TLK1221, and TLK1201A vs 3.3 V for TNETE2201.
- The PLL filter capacitors on pins 16, 17, 48, and 49 of the TNETE2201 are no longer required. The TLK2201B, TLK2201BI, TLK1221, and TLK1201A use these pins to provide added test capabilities. The capacitors, if present, do not affect the operation of the device.
- No pulldown resistors are required on the TXP/TXN outputs.
- The TLK1221 is a QFN version of the TLK1211 optimized for TBI-mode operation with no JTAG functionality.
- TLK1221 also has a faster relock time than TLK1201A or TLK2201B.

FUNCTIONAL BLOCK DIAGRAM



Detailed Description

In the TBI mode, the transmitter portion registers incoming 10-bit-wide data words (8b/10b encoded data, TD0–TD9) on the rising edge of REFCLK. REFCLK is also used by the serializer, which multiplies the clock by a factor of 10, providing a signal that is fed to the shift register. The 8b/10b encoded data is transmitted sequentially, bits 0 through 9, over the differential high-speed I/O channel.

Transmission Latency

Data transmission latency is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The minimum latency in TBI mode is 20 bit times. The maximum latency in TBI mode is 22 bit times.

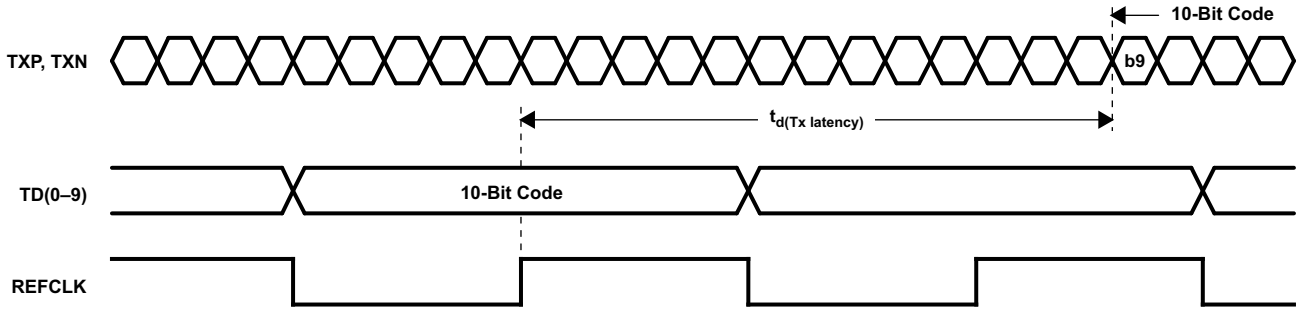


Figure 1. Transmitter Latency, Full-Rate Mode

Data Reception

The receiver section deserializes the differential serial data. The serial data is retimed based on an interpolated clock generated from the reference clock. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with the receive byte clocks (RBC0, RBC1).

Receiver Clock Select Mode

The TLK1221 only supports TBI-mode operation with half-rate and full-rate clocks on RBC0 and RBC1. In TBI mode, there are two user-selectable clock modes that are controlled by the RBCMODE terminal: 1) full-rate clock on RBC0 and 2) half-rate clocks on RBC0 and RBC1.

Table 1. Mode Selection

RBCMODE	MODE	RECEIVE BYTE CLOCK
		TLK1221
0	TBI half-rate	30–65 MHz
1	TBI full-rate	60–130 MHz

In the half-rate mode, two receive byte clocks (RBC0 and RBC1) are 180 degrees out of phase and operate at one-half the data rate. The clocks are generated by dividing down the recovered clock. The received data is output with respect to the two receive byte clocks (RBC0, RBC1), allowing a protocol device to clock the parallel bytes using the RBC0 and RBC1 rising edges. For the outputs to the protocol device, byte 0 of the received data is valid on the rising edge of RBC1. Refer to the timing diagram shown in Figure 2.

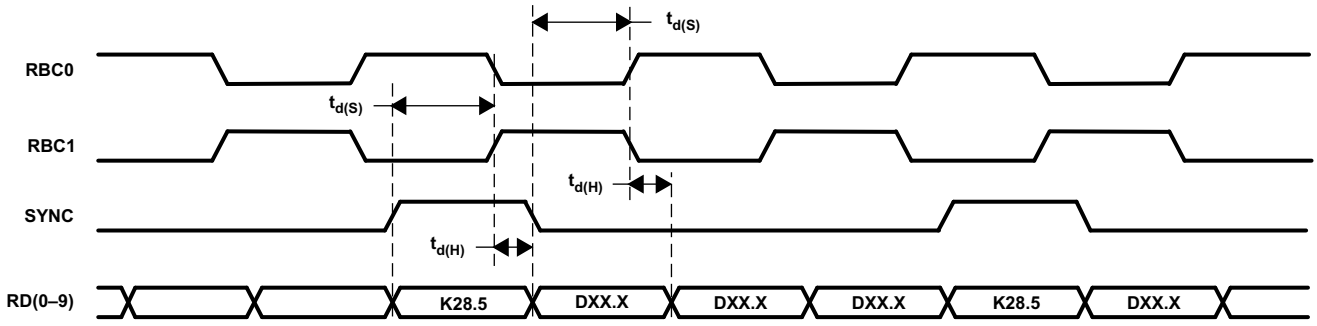


Figure 2. Synchronous Timing Characteristic Waveforms (TBI Half-Rate Mode)

The receiver clock interpolator can lock to the incoming data without the need for a lock-to-reference preset. The received serial data rate (RXP and RXN) is at the same baud rate as the transmitted data stream, ±0.02% (200 PPM) for proper operation.

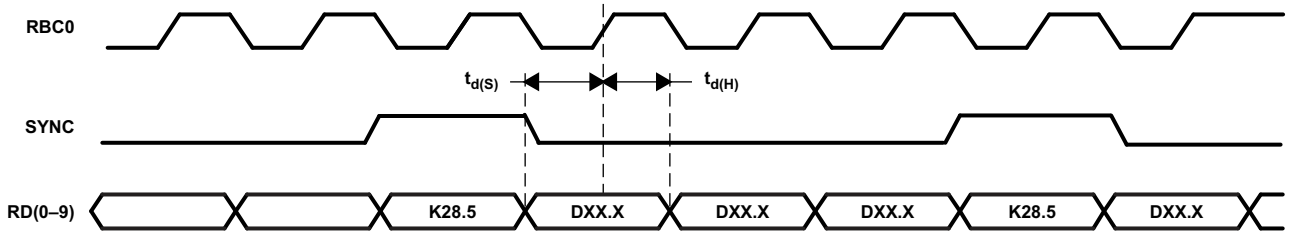


Figure 3. Synchronous Timing Characteristic Waveforms (TBI Full-Rate Mode)

Receiver Word Alignment

These devices use the IEEE 802.3 Gigabit Ethernet defined 10-bit K28.5 character, which contains the 7-bit comma-pattern word alignment scheme. The following sections explain how this scheme works and how it realigns to the proper byte boundary of the data.

Comma Character on Expected Boundary

These devices provide 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing the SYNCEN terminal high. This enables the function that examines and compares serial input data to the 7-bit synchronization pattern. The K28.5 character is defined by the 8b/10b coding scheme as a pattern consisting of 0011 1110 10 (a negative number beginning with disparity), with the 7 MSBs (0011 111) referred to as the comma character. The K28.5 character was implemented specifically for aligning data words. As long as the K28.5 character falls within the expected 10-bit boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 2 shows the timing characteristics of RBC0, RBC1, SYNC and RD0–RD9 while synchronized. (Note: the K28.5 character is valid on the rising edge of RBC1).

Comma Character Not on Expected Boundary

If synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 4. The RBC0 and RBC1 pulse widths are stretched or stalled in their current state during realignment. With this design, the maximum stretch that occurs is 20 bit times. This occurs during a worst-case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. Figure 4 shows the timing characteristics of the data realignment.

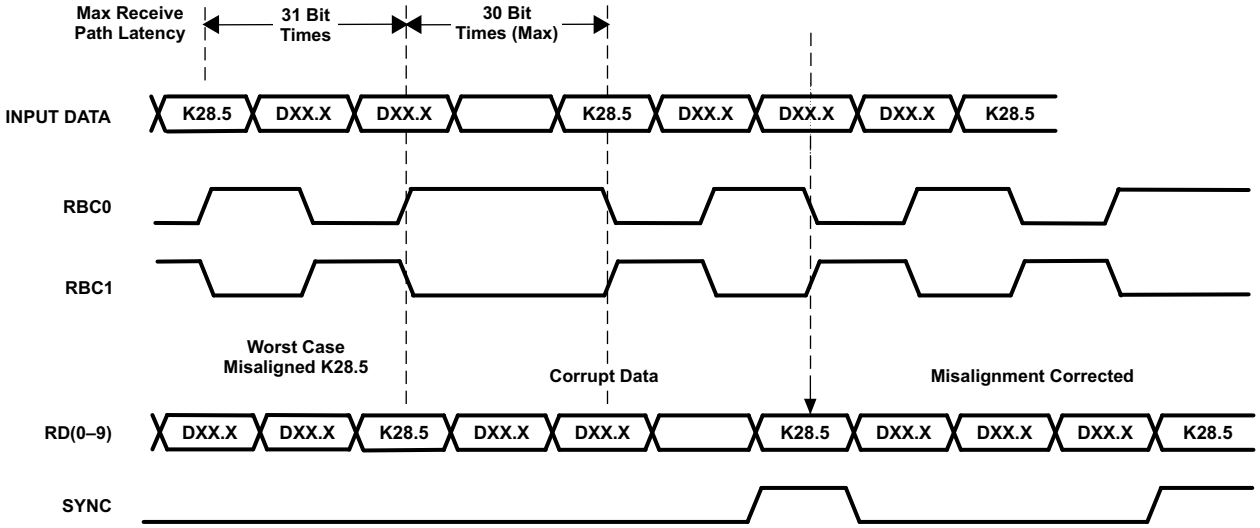


Figure 4. Word Realignment Timing Characteristic Waveforms

Systems that do not require framed data may disable byte alignment by tying SYNCEN low.

When a SYNC character is detected, the SYNC signal is brought high and is aligned with the K28.5 character. The duration of the SYNC pulse is equal to the duration of the data.

Data Reception Latency

The serial-to-parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as the first bit. The minimum latency in TBI mode is 18 bit times and the maximum latency is 24 bit times.

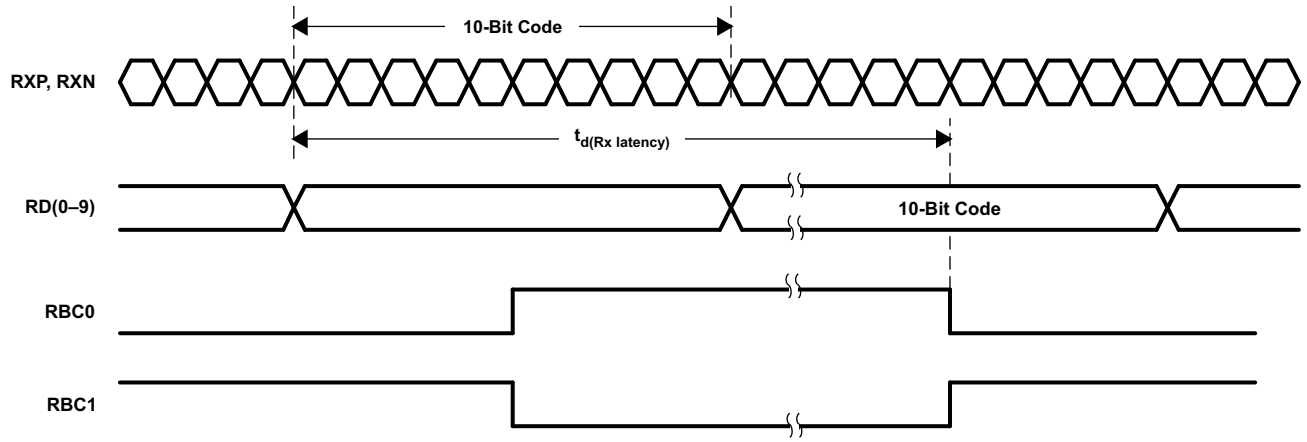


Figure 5. Receiver Latency, TBI Half-Rate Mode Shown

Testability

The loopback function provides for at-speed testing of the transmit/receive section of the circuitry. The enable function allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function also allows for built-in self-test (BIST).

Loopback Testing

The transceiver can provide a self-test function by enabling (LOOPEN to high level) the internal loopback path. Enabling this function causes serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

ENABLE Function

When held low, ENABLE disables all quiescent power in both analog and digital circuitry. This allows an ultralow-power idle state when the link is not active.

PRBS Function

These devices have a built-in $2^7 – 1$ PRBS function. When the PRBSEN control bit is set high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel transmitter input bus. Data from the normal parallel input source is ignored during PRBS test mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT) or to the receiver of another TLK1221. Because the PRBS is not really random and is really a predetermined sequence of ones and zeros, the data can be captured and checked for errors by a BERT. These devices also have a built-in BERT function on the receiver side that is enabled by PRBSEN. It can receive a PRBS pattern and check for errors, and then report the errors by forcing the SYNC/PASS terminal low. The PRBS testing supports two modes (normal and latched), which are controlled by the SYNCEN input. When SYNCEN is low, the result of the PRBS bit-error-rate test is passed to the SYNC/PASS terminal. When SYNCEN is high, the result of the PRBS verification is latched on the SYNC/PASS output (i.e., a single failure forces SYNC/PASS to remain low).

Table 2. PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
SIGNAL			
TXP TXN	38 39	PECL O	Differential output transmit. TXP and TXN are differential serial outputs that interface to a copper or an optical I/F module. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low.

Table 2. PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RXP RXN	34 33	PECL I	Differential input receive. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
REFCLK	14	I	Reference clock. REFCLK is an external input clock that synchronizes the receiver and transmitter interface (60 MHz to 130 MHz). The transmitter uses this clock to register the input data (TD0–TD9) for serialization. In the TBI mode that data is registered on the rising edge of REFCLK.
TD0–TD9	2–5, 7–12	I	Transmit data. These inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.
RD0–RD9	29–27, 25–19	O	Receive data. These outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1. RD0 is the first bit received.
RBC0 RBC1	17 18	O	Receive byte clock. RBC0 and RBC1 are recovered clocks used for synchronizing the 10-bit output data on RD0–RD9. In the half-rate mode, the 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data. In normal-rate mode, only RBC0 is valid and operates at 1/10th the serial data rate. Data is aligned to the rising edge.
RBCMODE	13	I P/D(1)	Receive clock mode select. When RBCMODE is low, half-rate clocks are output on RBC0 and RBC1. When RBCMODE is high, a full baud-rate clock is output on RBC0, and RBC1 is held low.
SYNCEN	32	I P/U (2)	Synchronous function enable. When SYNCEN is high, the internal synchronization function is activated. When this function is activated, the transceiver detects the comma pattern (0011 111 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0–RD9.
SYNC/PASS	30	O	Synchronous detect. The SYNC output is asserted high upon detection of the comma pattern in the serial data path. SYNC pulses are output only when SYNCEN is activated (asserted high). In PRBS test mode (PRBSEN = high), SYNC/PASS outputs the status of the PRBS test results (high = pass).
TEST			
LOOPEN	15	I P/D(3)	Loop enable. When LOOPEN is high (active), the internal loopback path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loopback test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRBSEN	31	I P/D(3)	PRBS enable. When PRBSEN is high, the PRBS generation circuitry is enabled. The PRBS verification circuit in the receive side is also enabled. A PRBS signal can be fed to the receive inputs and checked for errors, which are reported by the SYNC/PASS terminal indicating low.
ENABLE	1	I P/U(2)	When this terminal is low, the device is disabled for Iddq testing. RD0–RD9, RBCn, TXP and TXN are high-impedance. The pullup and pulldown resistors on any input are disabled. When ENABLE is high, the device operates normally.
POWER			
VDD	6, 16, 26	Supply	Digital logic power. Provides power for all digital circuitry and digital I/O buffers
VDDA	37	Supply	Analog power. VDDA provides power for the high-speed analog circuits, receiver, and transmitter.
VDDPLL	36	Supply	PLL power. Provides power for the PLL circuitry. This terminal requires additional filtering.
GROUND			
GNDA	35, 40	Ground	Analog ground. GNDA provides a ground for the high-speed analog circuits, RX and TX.
GNDQFN	PAD	Ground	Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers

(1) P/D = Internal pulldown resistor
(2) P/U = Internal pullup resistor
(3) P/D = Internal pulldown resistor

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE (1)	UNIT
V_{DD}	Supply voltage (2)	–0.3 to 3	V
V_I	Input voltage range at TTL terminals	–0.5 to 4	V
V_I	Input voltage range at other terminals	–0.3 to V_{DD} + 0.3	V
ESD	Electrostatic discharge	CDM: 1, HBM: 2	kV
T_{stg}	Storage temperature	–65 to 150	°C
T_A	Characterized free-air temperature range	–40 to 85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RHA (1) (2)	2.85 W	28 mW/°C	1.57 W	1.4 W

(1) The thermal resistance junction to ambient of the RHA package is 35°C/W measured on a high-K board.
(2) The thermal resistance junction-to-case (exposed pad) of the RHA package is 5°C/W.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}, V_{DDA}, V_{DDPLL}	Supply voltage		2.3	2.5	2.7	V
I_{DD}, I_{DDA}, I_{DDPLL}	Total supply current	Frequency = 1.25 Gbps, PRBS pattern; ENABLE = 1, V_{DD} , V_{DDPLL} and V_{DDA} = 2.7 V			113	mA
P_D	Total power dissipation	Frequency = 1.25 Gbps, PRBS pattern		235	305	mW
I_{DDQ}	Total shutdown current (I_{DD}+I_{DDA} + I_{DDPLL})	Enable = 0; V_{DD} , V_{DDPLL} and V_{DDA} = 2.7 V			1000	µA
PLL	Startup lock time	V_{DD}, V_{DDA} = 2.5 V			500	µs
T_A	Operating free-air temperature		–40		85	°C

REFERENCE CLOCK (REFCLK) TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency	Minimum data rate	TYP – 0.01%	60	TYP + 0.01%	MHz
		Maximum data rate	TYP – 0.01%	130	TYP + 0.01%	
	Accuracy		–100		100	ppm
DC	Duty cycle		40%	50%	60%	
	Jitter	Random plus deterministic			40	ps

TTL ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –400 µA	V_{DD} – 0.2	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND	0.25	0.5	V
V_{IH}	High-level input voltage		1.7		3.6	V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	V_{DD} = 2.3 V, V_{IN} = 2 V			40	µA
I_{IL}	Low-level input current	V_{DD} = 2.3 V, V_{IN} = 0.4 V	–40			µA
C_{IN}	Input capacitance				4	pF

TRANSMITTER/RECEIVER CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VOD = |TxD – TxN|	Rt = 50 Ω	600	850	1100	mV
$V_{(CM)}$	Transmit common mode voltage range	Rt = 50 Ω	1000	1250	1400	mV
	Receiver input voltage requirement, VID = |RxP – RxN|		200		1600	mV
	Receiver common mode voltage range, (RxP + RxN)/2		1000	1250	2250	mV
C_I	Receiver input capacitance				2	pF
$t_{(TJ)}$	Serial data total jitter (peak-to-peak)	Differential output jitter, random + deterministic, PRBS pattern, R_ω = 125 MHz			0.24	UI
$t_{(DJ)}$	Serial data deterministic jitter (peak-to-peak)	Differential output jitter, PRBS pattern, R_ω = 125 MHz			0.12	UI
t_r, t_f	Differential signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, see Figure 6 and Figure 8	100		250	ps
	Serial data jitter tolerance minimum required eye opening, (per IEEE-802.3 specification)	Differential input jitter, random + deterministic, R_ω = 125 MHz	0.25			UI
	Receiver data acquisition lock time from power up				500	µs
	Data relock time from application of valid input data stream	0.75 UI jitter closure with random data ata 1.25 Gbps			256	ns
		0.20 UI jitter closure with 01010.. data at 1.25 Gbps			128	
$t_{d(Tx\ latency)}$	Tx latency	See Figure 1	20		22	UI
$t_{d(Rx\ latency)}$	Rx latency	See Figure 5 and Figure 7	18		24	UI

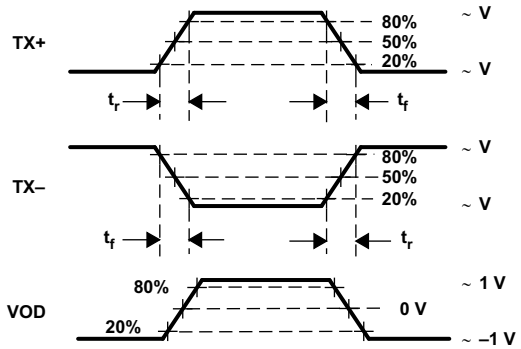


Figure 6. Differential and Common-Mode Output Voltage Definitions

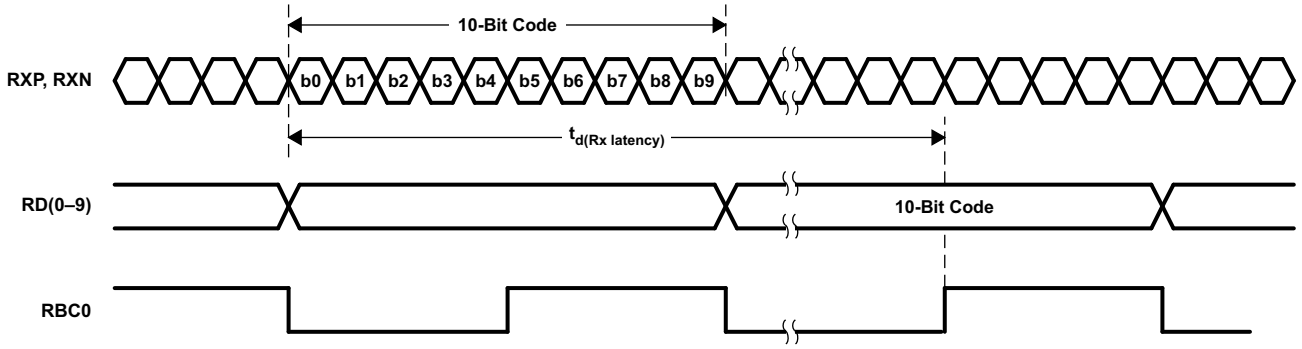


Figure 7. Receiver Latency, TBI Normal Mode Shown

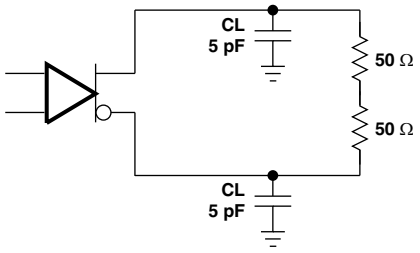


Figure 8. Transmitter Test Setup

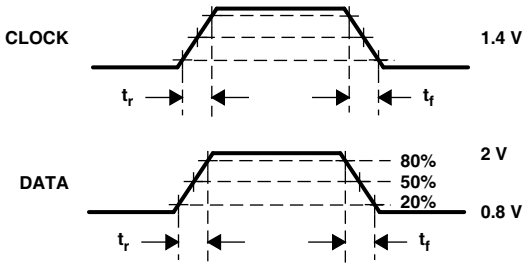


Figure 9. TTL Data I/O Valid Levels for AC Measurement

LVTTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(RBC)}$	Clock rise time	80% to 20% output voltage, C = 5 pF (see Figure 9)	0.3		1.5	ns
$t_{f(RBC)}$	Clock fall time		0.3		1.5	ns
t_r	Data rise time		0.3		1.5	ns
t_f	Data fall time		0.3		1.5	ns
$t_{su(d1)}$	Data setup time (RD0–RD9)	TBI normal mode (see Figure 3), R_ω = 125 MHz, data valid prior to RBC0 rising	2.5			ns
		TBI normal mode (see Figure 3), R_ω = 61.44 MHz, data valid prior to RBC0 rising	5			ns
$t_{h(d1)}$	Data hold time (RD0–RD9)	TBI normal mode (see Figure 3), R_ω = 125 MHz, data valid after RBC0 rising	2			ns
		TBI normal mode (see Figure 3), R_ω = 61.44 MHz, data valid after RBC0 rising	4			ns
$t_{su(d3)}$	Data setup time (RD0–RD9)	TBI half-rate mode, R_ω = 125 MHz (see Figure 2)	2.5			ns
$t_{h(d3)}$	Data hold time (RD0–RD9)	TBI half-rate mode, R_ω = 125 MHz (see Figure 2)	1.5			ns

TRANSMITTER TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(d4)}$	Data setup time (TD0–TD9)		1.6			ns
$t_{h(d4)}$	Data hold time (TD0–TD9)		0.8			ns
t_r, t_f	TD[0,9] data rise and fall time	See Figure 9			2	ns

Table 3. AVAILABLE OPTIONS

T_A	PACKAGE
	QFN PLASTIC QUAD FLAT PACK (RHA)
–40°C to 85°C	TLK1221RHA

APPLICATION INFORMATION

8b/10b Transmission Code

The PCS maps GMII signals into ten-bit code groups and vice versa, using an 8b/10b block coding scheme. The PCS uses the transmission code to improve the transmission characteristics of information to be transferred across the link. The encoding defined by the transmission code ensures that sufficient transitions are present in the PHY bit stream to make clock recovery possible in the receiver. Such encoding also greatly increases the likelihood of detecting any single- or multiple-bit errors that may occur during transmission and reception of information. The 8b/10b transmission code specified for use has a high transition density, is run length limited, and is dc-balanced. The transition density of the 8b/10b symbols ranges from 3 to 8 transitions per symbol. The definition of the 8b/10b transmission code is specified in IEEE 802.3 Gigabit Ethernet and ANSI X3.230-1994 (FC-PH), clause 11.

8b/10b transmission code uses letter notation describing the bits of an unencoded information octet. The bit notation of A, B, C, D, E, F, G, H for an unencoded information octet is used in the description of the 8b/10b transmission code-groups, where A is the LSB. Each valid code group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups and /Kx.y/ for the special control code-groups, where y is the decimal value of bits EDCBA and x is the decimal value of bits HGF (noted as K<HGF.EDCBA>). Thus, an octet value of FE representing a code-group value of K30.7 would be represented in bit notation as 111 11110.

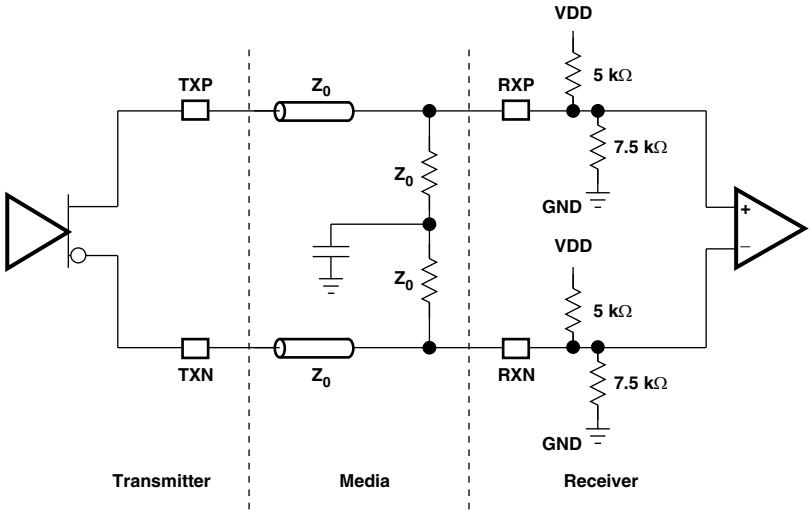


Figure 10. High-Speed I/O Directly Coupled Mode

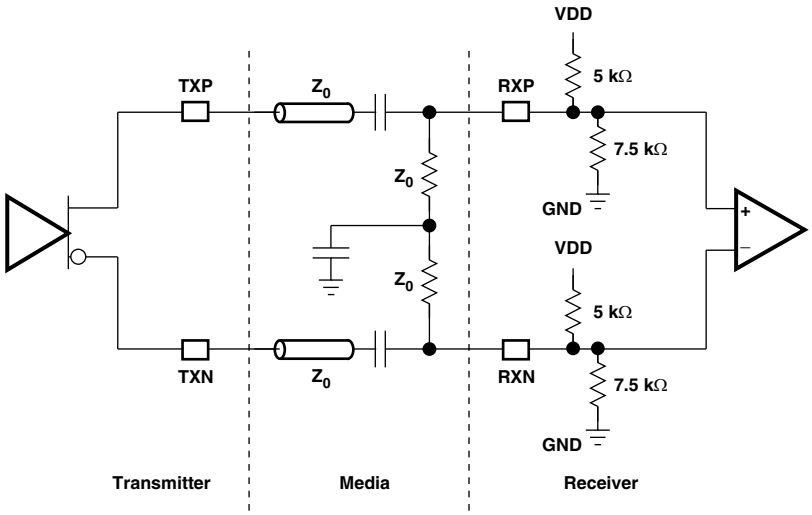


Figure 11. High-Speed I/O AC-Coupled Mode

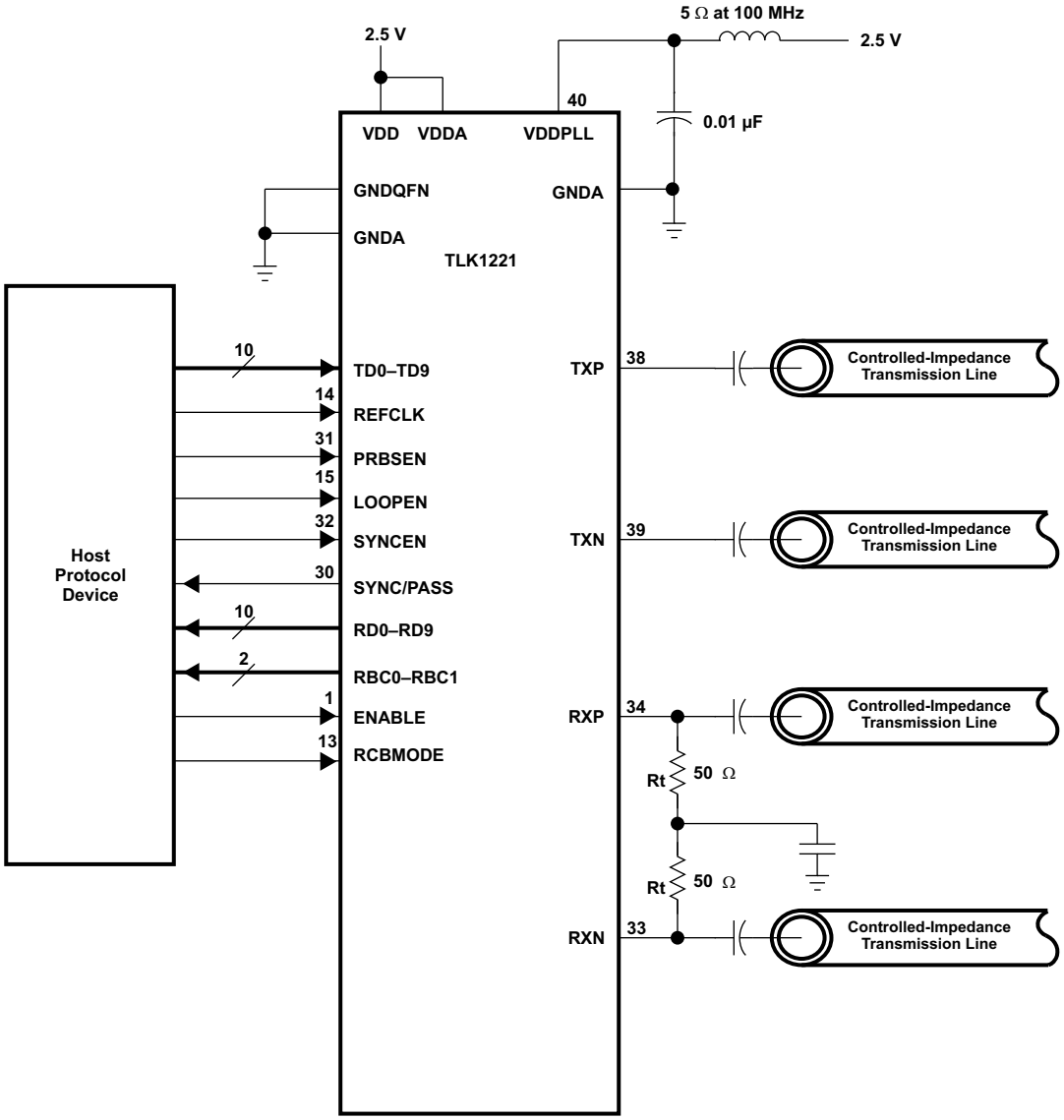


Figure 12. Typical Application Circuit (AC Mode)

REVISION HISTORY

Changes from Original (February 2007) to Revision A **Page**

- Added Fast Relock Times Less to list of Features 1
- Changed Last two items in the Differenvces list 2
- Changed Data relock time in the Transmitter Characteristics 9

Changes from Revision A (June 2007) to Revision B **Page**

- Changed From: The minimum latency in TBI mode is 19 bit times. The maximum latency in TBI mode is 20 bit times. To: The minimum latency in TBI mode is 20 bit times. The maximum latency in TBI mode is 22 bit times 3
- Changed From: The minimum latency in TBI mode is 21 bit times and the maximum latency is 31 bit times. To: The minimum latency in TBI mode is 18 bit times and the maximum latency is 24 bit times. 5

Changes from Revision B (March 2009) to Revision C **Page**

- Changed Pin Function Table - Enable Pin I/O From: P/D to P/U 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK1221RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK1221	Samples
TLK1221RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK1221	Samples
TLK1221RHATG4	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK1221	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

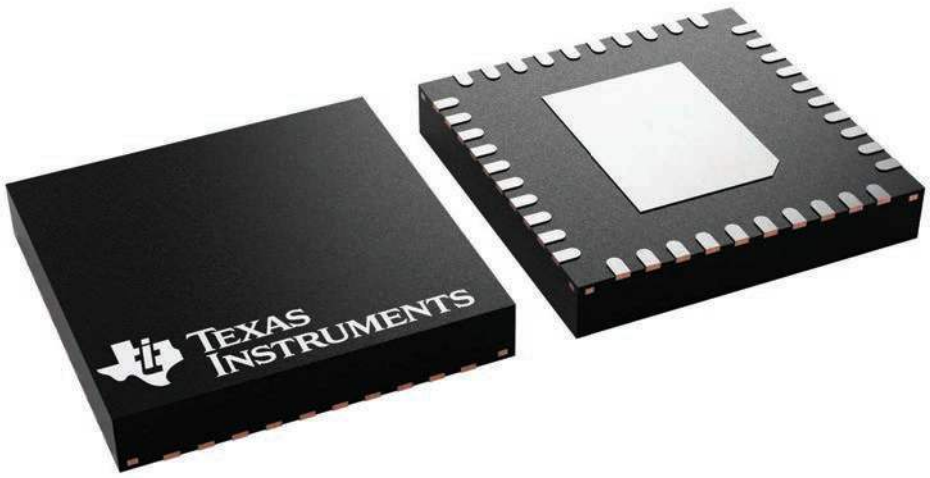
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



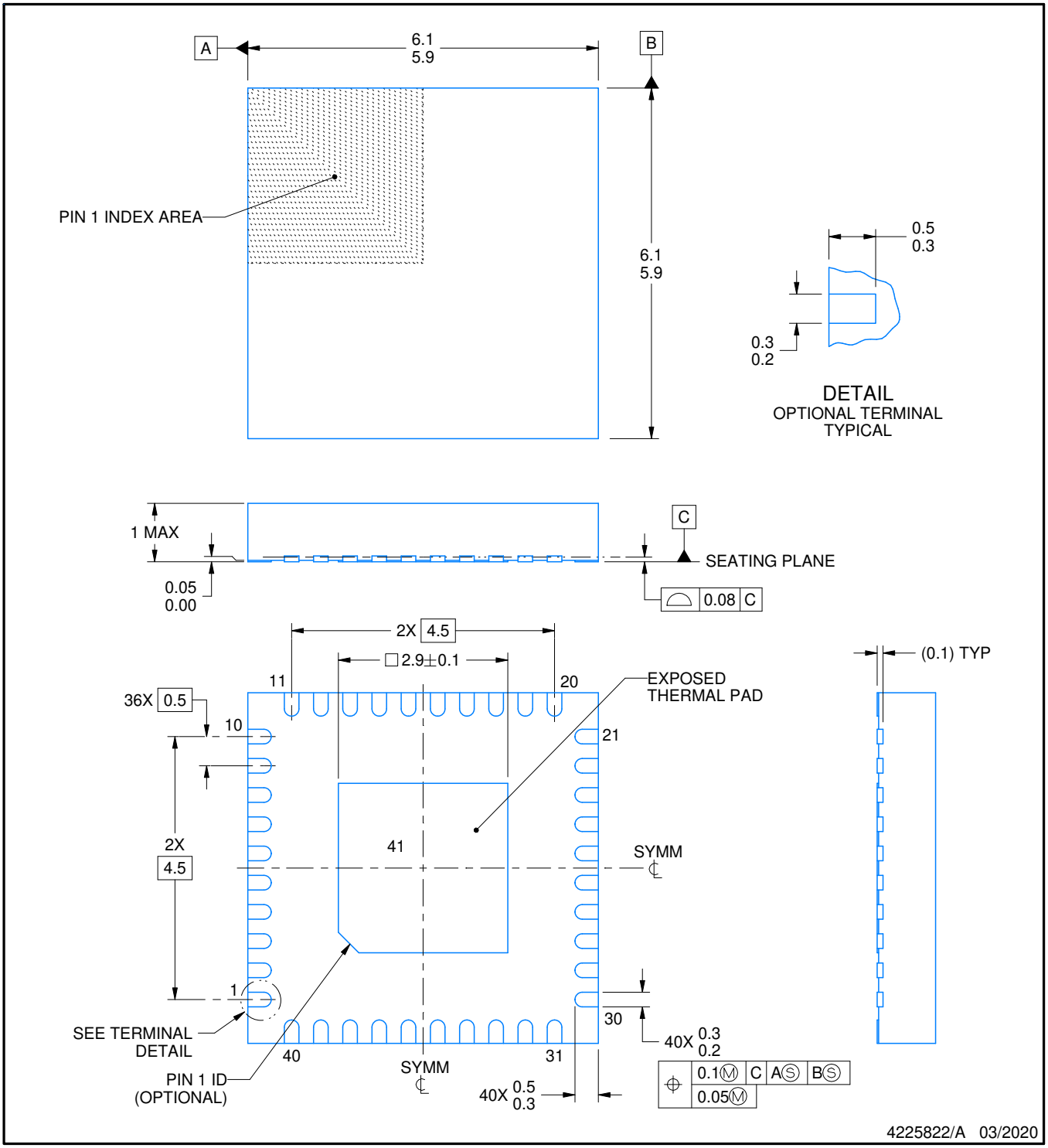
4225870/A

PACKAGE OUTLINE

RHA0040D

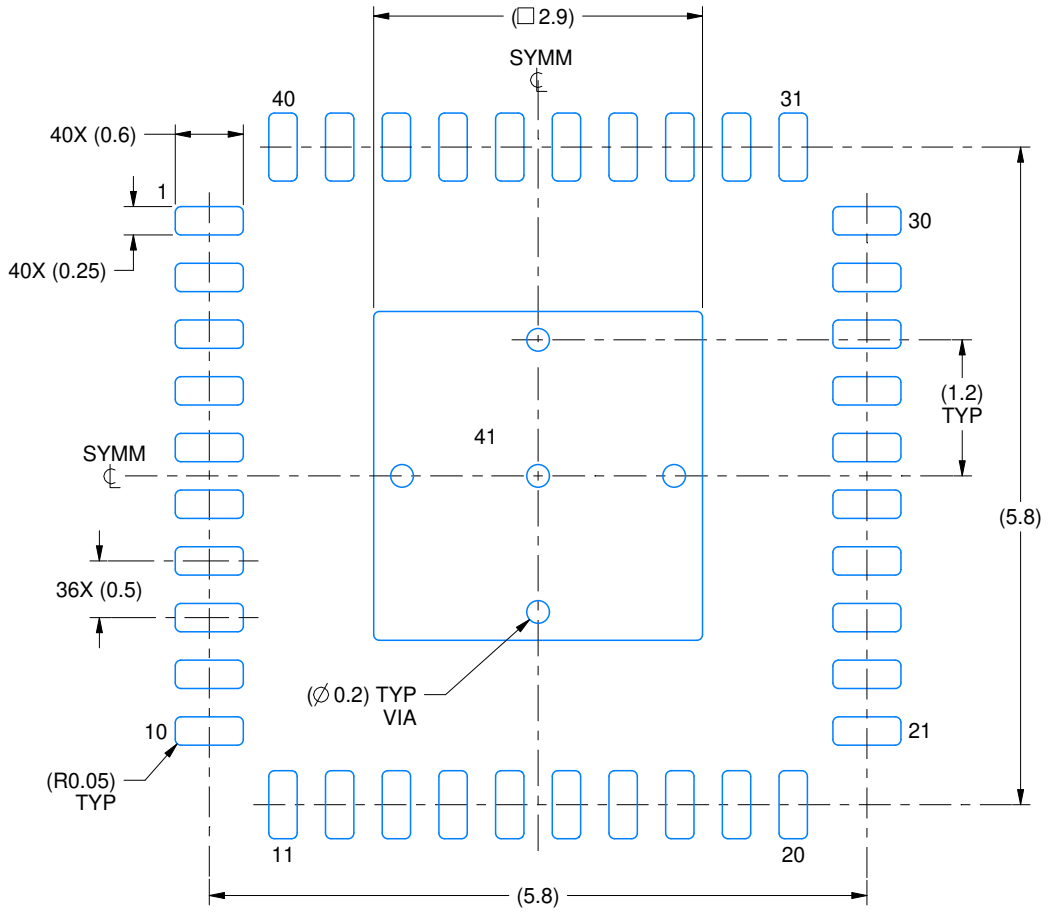
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

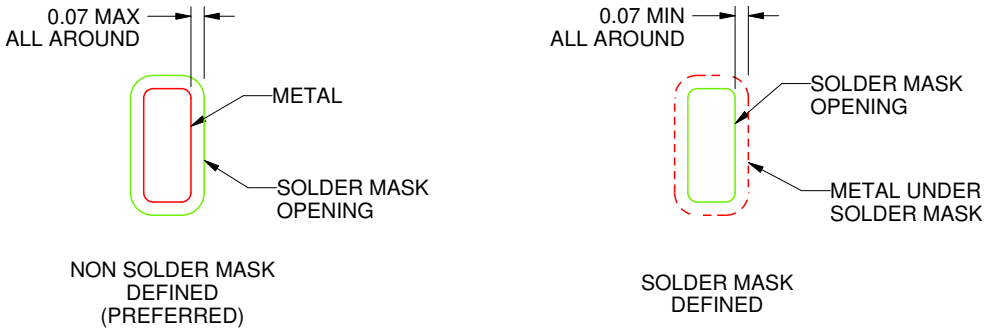


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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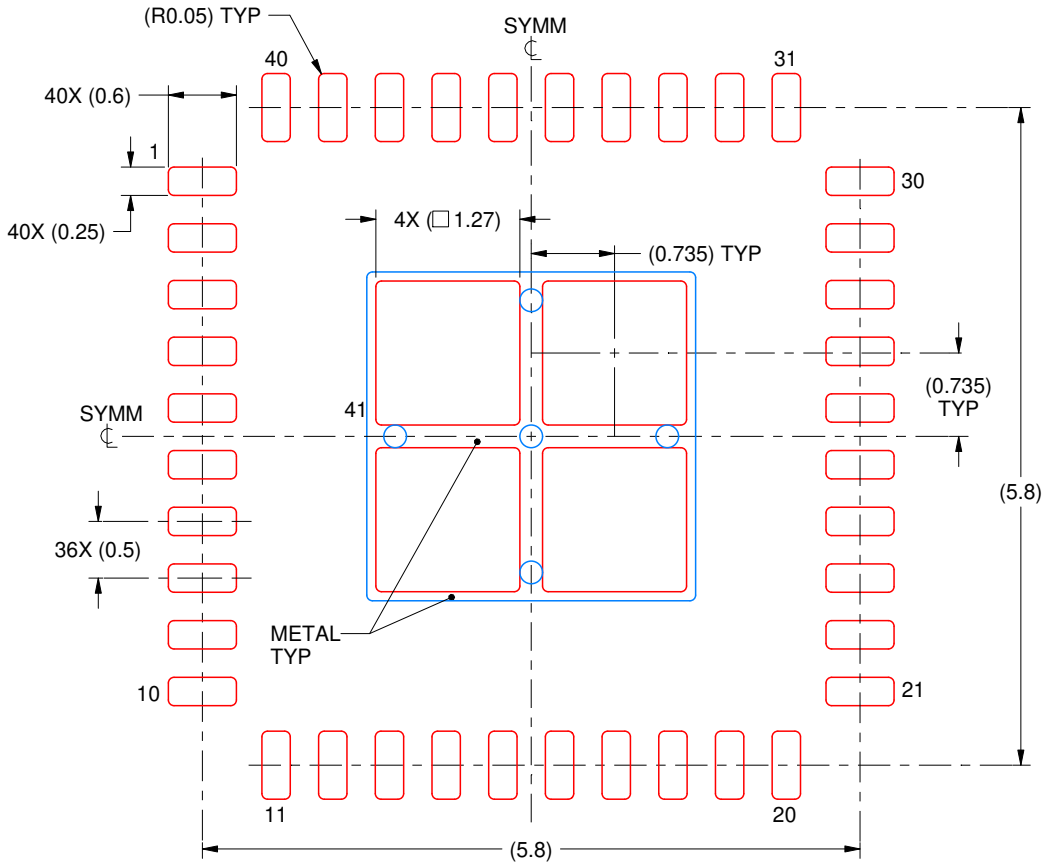
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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