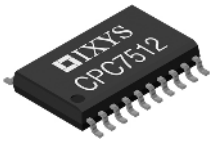
CPC7512

Dual 1-Form-A Shunt-Isolated High-Voltage High-Frequency Analog Switch



Features

- Up to ±320V Switch to Ground Potential
- Series Switches Open Contact Isolation up to ±600V
- 60dB Off Isolation at 1MHz
- Thermal Shutdown Protects Against Fault Conditions
- Guaranteed Break-Before-Make
- Low, Matched R_{ON}
- Flexible Switch Configurations
- Smart Logic for Power-Up/Hot-Plug State Control
- 5V Operation with Very Low Power Consumption
- TTL Logic-Level Inputs
- Input Latch
- Clean, Bounce-Free Switching
- Monolithic IC Reliability

Applications

- Multiplexed Ultrasonic Transducer Switching
- Battery Monitoring and Charging
- Automatic Test Equipment (ATE)
- Instrumentation
- Industrial Controls and Monitoring

Description

The CPC7512 dual 1-Form-A high-voltage, high-frequency, shunt-isolated analog switch builds upon IXYS Integrated Circuits Division's design and fabrication expertise for industrial applications. This monolithic solid state device provides the switching functionality of two normally open (1-Form-A) solid state relays for high frequency applications in one small economical package. Both switches incorporate shunt isolation by means of a T-switch compensation technique to minimize series capacitance through the open off-state switches for improved off-state isolation over frequency.

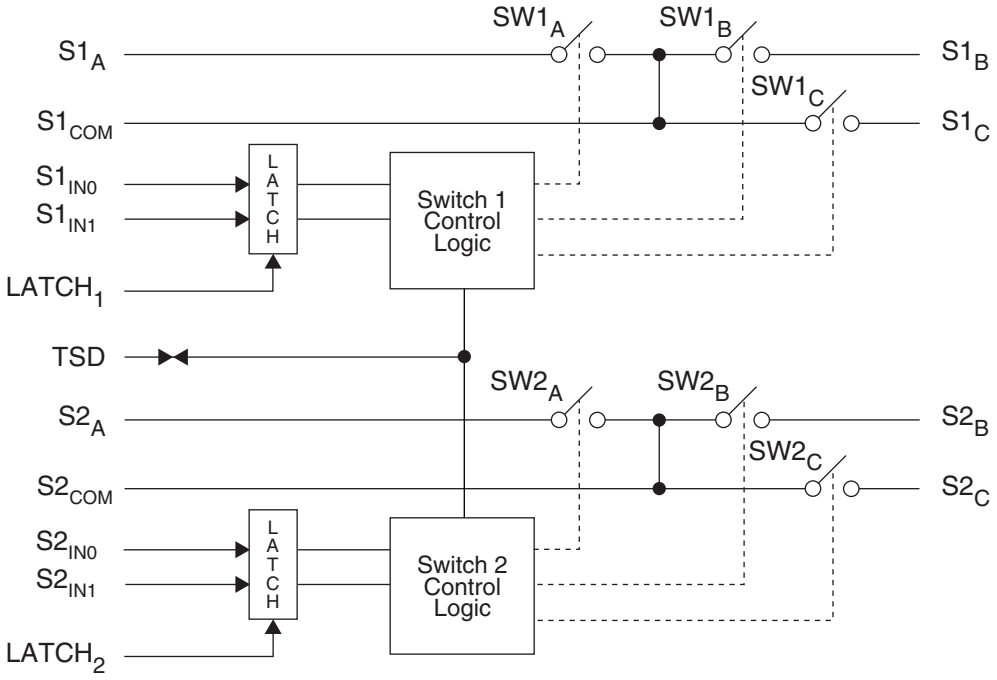
Designed to provide flexible single-ended or differential access to high voltage networks, the CPC7512 is functionally configured as two independent logical switches. The self-biasing switches do not require external high-voltage supplies for proper operation.

An integrated thermal shutdown feature provides not only enhanced protection for devices connected to high voltage networks up to ±320V, but also an external signal to indicate the device is shut down.

Ordering Information

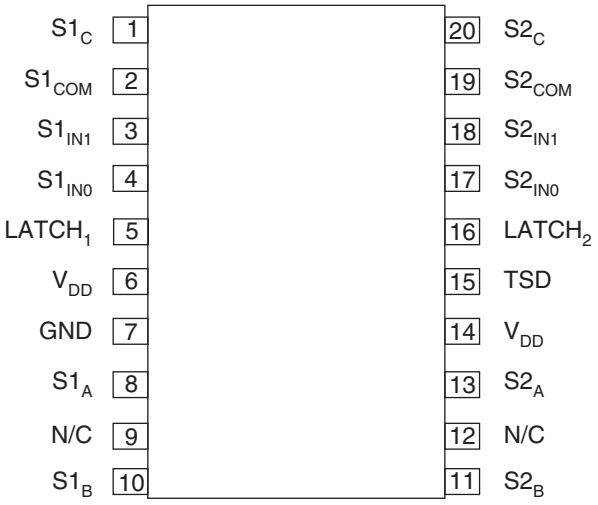
Part #	Description
CPC7512Z	20-Pin SOIC in Tubes (40/Tube)
CPC7512ZTR	20-Pin SOIC Tape & Reel (1000/Reel)

Figure 1. CPC7512 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pin Descriptions

Pin	Name	Type	Description
6,14	V_{DD}	P	Logic Supply Voltage
7	GND	P	Ground
9, 12	N/C	-	Not Connected
15	TSD	I/O	Thermal Shutdown
			Switch 1
1	$S1_C$	A	Switch 1 Port C
2	$S1_{COM}$	A	Switch 1 common node for all three switches
8	$S1_A$	A	Switch 1 Port A
10	$S1_B$	A	Switch 1 Port B
3	$S1_{IN1}$	I	Switch 1 input control bit: Bit 1
4	$S1_{IN0}$	I	Switch 1 input control bit: Bit 0
5	$LATCH_1$	I	Switch 1 configuration latch
			Switch 2
20	$S2_C$	A	Switch 2 Port C
19	$S2_{COM}$	A	Switch 2 common node for all three switches
13	$S2_A$	A	Switch 2 Port A
11	$S2_B$	A	Switch 2 Port B
17	$S2_{IN0}$	I	Switch 2 input control bit: Bit 0
18	$S2_{IN1}$	I	Switch 2 input control bit: Bit 1
16	$LATCH_2$	I	Switch 2 configuration latch

Pin Types:
P = Power
I = Digital Input
I/O = Digital Input / Output with internal pull up.
A = Analog I/O

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD} (+5V supply)	-0.3	+ 7	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Switch output to logic inputs isolation	-	320	V
Switch output to ground	-	320	V
Series switch open-contact isolation (Across any two series switches)	-	600	V
Operating relative humidity, Non-Condensing	5	95	%
Junction operating temperature	-40	+110	°C
Ambient operating temperature	-40	+85	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing or design. Typical values are characteristic of the device at 25°C, and are the result of engineering evaluations. They are provided for informational purposes only and are not guaranteed by production testing.

Unless otherwise noted the specifications cover the V_{DD} operational range and the ambient operating temperature range T_A = -40°C to +85°C. Testing is performed with the logic low input voltage V_{IL} = 0V_{DC} and the logic high input voltage V_{IH} = V_{DD}.

1.5 Switch Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW} = Sx_A to Sx_{COM}, Sx_B to Sx_{COM}, Sx_C to Sx_{COM}; Sx_{COM} = Gnd; All switches Off					
	+25°C, V_{SW} = ±320V	I_{SW}	-	±0.1	±1	µA
	+85°C, V_{SW} = ±330V			±0.3		
	-40°C, V_{SW} = ±310V			±0.1		
On Resistance: Sx_A to Sx_B	SW_{xA} = SW_{xB} = On, SW_{xC} = Off I_{SW} = ±10mA, ±40mA					
	+25°C	R_{ON}	-	29	-	Ω
	+85°C		-	-	62	
	-40°C		-	21	-	
On Resistance Matching: Sx_A to Sx_B	Per On Resistance Test Conditions	ΔR_{ON}	-	0.1	1	Ω
On Resistance: SWx_C, Sx_C to Sx_{COM}	SW_{xA} = SW_{xB} = Off, SW_{xC} = On I_{SW} = ±10mA, ±40mA					
	+25°C	R_{ON}	-	60	-	Ω
	+85°C		-	85	110	
	-40°C		-	45	-	
Off-State Voltage	Maximum Differential Voltage[1,2], Switches Off	V_{OFF}	-	-	600	V
High Frequency Dynamic Current Limit (t ≤0.5 µs)	Apply ±1 kV 10x1000 µs pulse with appropriate protection in place [2], Switches On	I_{SW}	-	1	-	A
Logic Input to Switch Output Isolation	V_S = Sx_A to Gnd, Sx_B to Gnd, Sx_C to Gnd, Sx_{COM} to Gnd; All switches Off.					
	+25°C, V_S = ±320V	I_{SW}	-	±0.1	±1	µA
	+85°C, V_S = ±330V			±0.3		
	-40°C, V_S = ±310V			±0.1		
Crosstalk	50Ω Termination, f=1MHz [3]	-	-55	-	-	dB
Off-State Isolation	50Ω Termination, f=1MHz [4]	-	50	60	-	dB
Switch to Ground Capacitance	All switches Off, Sx_A, Sx_B, Sx_C, and Sx_{COM} are open circuit					
	Sx_A to Gnd, Sx_B to Gnd	C	-	80	-	pF
	Sx_C to Gnd		-	40	-	
	Sx_{COM} to Gnd		-	115	-	
Transient Immunity	100V_{P-P} Square Wave at 100Hz	dV/dt	1500	2100	-	V/µs

[1] Across any two inactive (Off) switches.
[2] Maximum +/- 310V with respect to ground at any switch.
[3] See "Figure 1. Crosstalk Test Configuration" on page 6.
[4] See "Figure 2. Switch Off-State Isolation Test Configuration" on page 6.

NOTE: V_{SW} is the voltage across a switch or a pair of switches in series and V_S is the voltage at a switch pin with respect to ground.

Figure 1. Crosstalk Test Configuration

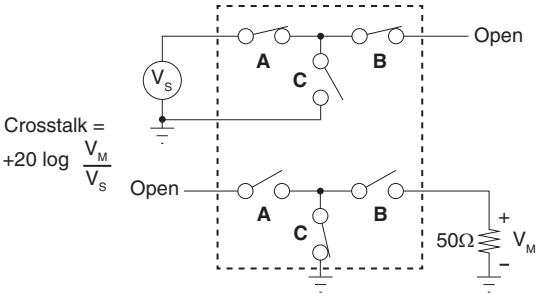
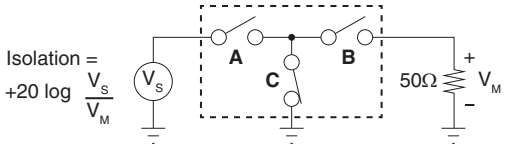


Figure 2. Switch Off-State Isolation Test Configuration



1.6 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input Voltage: (Sx_{INx}, $LATCH_x$, TSD)						
Logic High Threshold	Input voltage rising	V_{IH}	-	1.5	2.0	V
Logic Low Threshold	Input voltage falling	V_{IL}	0.8	1	-	V
Hysteresis		ΔV_{IN}		500		mV
Input Leakage Current						
Logic High:						
Sx_{INx}	V_{IH} = 2.4V	I_{IH}	-	0.1	1	µA
$LATCH_x$			-10	-19	-175	
TSD			-10	-16	-50	
Logic Low:						
Sx_{INx}	V_{IL} = 0.4V	I_{IL}	-	0.1	1	µA
$LATCH_x$			-	-47	-250	
TSD			-	-16	-50	
Output Characteristics						
Output Voltage: TSD:						
Logic High	I_{TSD} = 10µA	V_{TSD_Off}	2.4	V_{DD}	-	V
Logic Low	I_{TSD} = 1mA	V_{TSD_On}	-	0	0.4	V

1.7 Switch Timing Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Switch turn on delay	$LATCH_x$ = 0V, I_{SW_off} = 0mA, t_{on} @ I_{SW} = 9mA	t_{d_on}	-	0.25	1.0	ms
Switch turn off delay	$LATCH_x$ = 0V, I_{SW_on} = 10mA, t_{off} @ I_{SW} = 0.5mA	t_{d_off}	-	0.05	0.5	ms
No Overlap[1] (Break-before-make)	Sx_A to Sx_C, Sx_B to Sx_C, $t_{d\_off} \le t_{d\_on}$, Both directions, 4.75 ≤ V_{DD} ≤ 5.25V		TRUE			

[1] This parameter ensures the turn off time for Switches A and B is less than the turn on time of Switch C and the turn off time of Switch C is less than the turn on time of Switches A and B thereby assuring there is no conduction from either Switch A or B through Switch C when switching between complementary states.

1.8 V_{DD} Voltage Supply Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
Voltage operational range	-	V_{DD}	4.5	5	5.5	V
	No Overlap: See Note	V_{DD}	4.75	5	5.25	V
Current Specifications						
V_{DD} Current	$4.5 \le V_{DD} \le 5.5V$, All States, All logic I/O = Open	I_{DD}	0.4	1.5	2.3	mA
Under Voltage Lockout Specifications						
Thresholds	V_{DD} rising	UVLO	-	3.4	-	V
	V_{DD} falling		-	3	-	
Hysteresis			-	0.4	-	

Note: To ensure compliance of the “No Overlap” parameter given in Section 1.7 "Switch Timing Specifications” on page 6, the operational voltage range is reduced as listed above.

1.9 Protection Circuitry Thermal Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Thermal Shutdown Temperature Specifications [1]						
Thermal shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits	T_{TSD_on}	110	125	150	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C

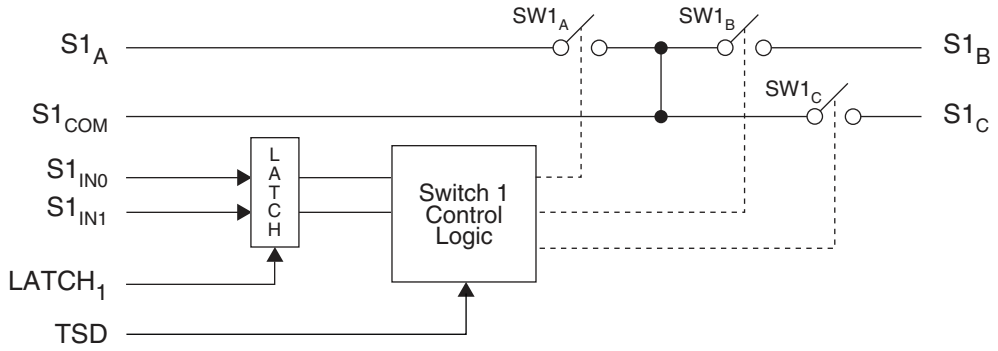
[1] *Thermal shutdown flag (TSD) will be high during normal operation and low during thermal shutdown state.*

1.10 Truth Table

The truth table and block diagram are shown for Switch 1. Operation is the same for both switches, S1 and S2. Refer to accompanying block diagram.

$LATCH_1$	$S1_{IN1}$	$S1_{IN0}$	TSD	$SW1_A$	$SW1_B$	$SW1_C$	Switch State
0	0	0	Z [2]	OFF	OFF	OFF	All-Off: All switches are open (Off) [1]
0	0	1		OFF	ON	ON	BC: $S1_B$ connected to $S1_C$
0	1	0		ON	ON	OFF	AB: $S1_A$ connected to $S1_B$
0	1	1		OFF	OFF	ON	C: $S1_C$ connected $S1_{COM}$
1	x	x		Unchanged	Unchanged	Unchanged	Latest switch state persists
x	x	x	0 [3]	OFF	OFF	OFF	Thermal shutdown active, all switches are open (Off)
x	x	x	0 [4,5]	OFF	OFF	OFF	All-Off: All switches are open (Off)

[1] *Default state following power up and after an under-voltage lock out event.*
[2] *Z = High Impedance with a weak internal pull-up. Because TSD has an internal pull-up, it should be controlled with an open-collector or open-drain type device.*
[3] *TSD outputs a logic low.*
[4] *TSD driven to a logic low by an external device. External device output should be an open-collector or an open-drain type.*
[5] *When TSD is released, the switches revert back to their previous state.*



2. Performance Data

Figure 3. On-State Insertion Loss: Sx_A to Sx_B

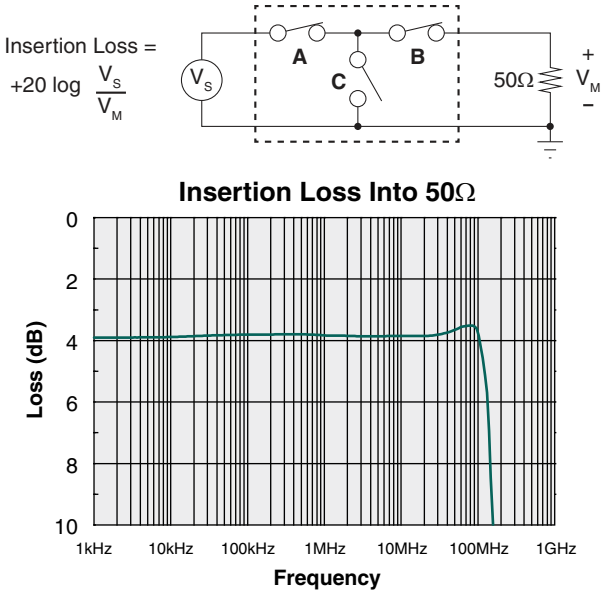


Figure 4. Off-State Switch Isolation: Sx_A to Sx_B

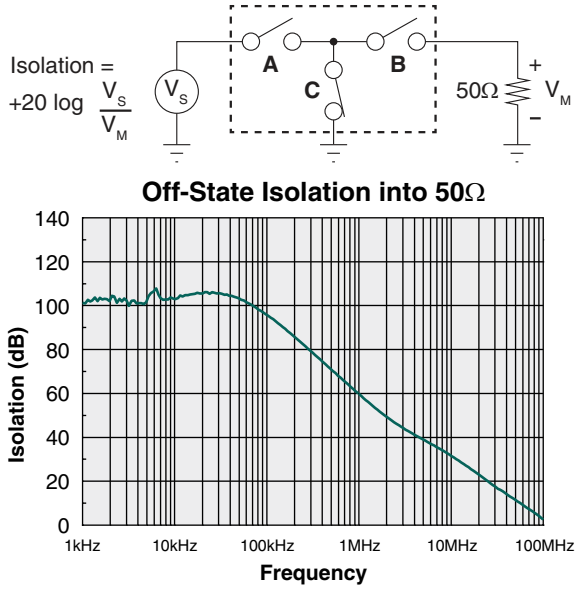
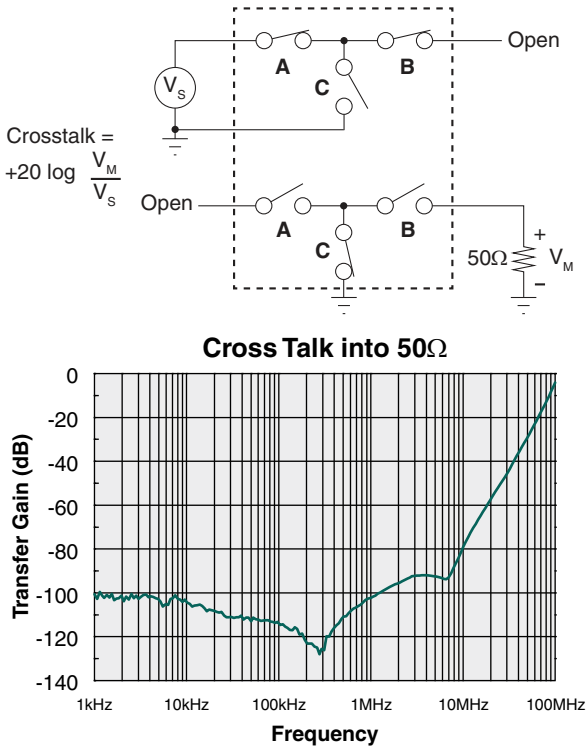


Figure 5. Switch to Switch Cross Talk



3. Functional Description

3.1 Introduction

The CPC7512 Dual, 1Form-A, Shunt-Isolated High-Voltage, High-Frequency, Analog Switch has two symmetrical switch arrays with four operating states to facilitate switching of high-frequency, high-voltage signals using the AB and C switch states and the flexibility to provide a variety of alternative switching solutions for low-frequency high-voltage signal applications. Operational states and logical behavior of the device is shown in the **"Truth Table" on page 8**. Switch organization consists of two channels, each having three switches.

Within each channel there is an independent LATCH input and a common Thermal Shutdown circuit that is shared by the two channels. Other than the shared TSD circuit, switch functionality under normal operating conditions within each channel is independent of the other channel. In designs where the switches will be required to carry high load currents or operate in higher temperature environments, the thermal specifications should be reviewed because the TSD circuit is shared by both channels. An excess thermal condition in one channel resulting in an active TSD event will cause an interruption in the other channel as well when the TSD protection circuit activates.

Solid-state switch construction of the CPC7512 offers clean, bounce-free switching with simple TTL logic level input control to provide access to high voltage interfaces without the impulse noise generated by traditional electromechanical switching techniques. TTL logic level input control eliminates the additional driver circuitry required by traditional techniques.

The low on-resistance (R_{ON}) symmetrical linear switches utilized in the AB switch state are configured as matched pairs, $SW1_A/SW1_B$ and $SW2_A/SW2_B$, for improved performance when differential access is required. Their symmetrical construction provides an additional degree of design flexibility allowing either side of the switch to be connected to the high voltage network.

Integrated into the CPC7512 switches are high frequency dynamic current limiting and thermal shutdown mechanisms to provide protection for the electronics being connected to a high voltage network during a fault condition. High frequency positive and negative transient currents such as lightning are reduced by the dynamic current limiting function while protection from prolonged low frequency power-cross and DC currents is provided by the thermal shutdown circuitry.

To protect against a high voltage fault in excess of the CPC7512's maximum voltage rating, use of an over-voltage protector is required. The protector must limit the voltage seen at the switch terminals to a level less than the switches' breakdown voltage. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type protector is highly recommended. With proper selection of the protector, telecom applications using the CPC7512 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

Operating from a single +5V supply the CPC7512 has extremely low power consumption.

3.2 Under-Voltage Switch Lock-Out Circuitry

Smart logic in the CPC7512 provides for switch state control during both power up and power loss transients to prevent undesired connections to high voltage networks. This is done by setting the switches' logic to the All-Off state. An internal detector evaluates the V_{DD} supply against internally set thresholds to determine when to de-assert the under-voltage switch lock-out circuitry with a rising V_{DD}, and when to assert the under-voltage switch lock-out circuitry with a falling V_{DD}. Any time unsatisfactory low V_{DD} conditions exist, the lock-out circuit overrides user switch control by blocking the external information applied to the input pins, output by the internal latch, and conditioning the internal switch commands to the All-Off state. Upon restoration of V_{DD}, the switches will remain off until the $LATCH_x$ input is pulled low at which time proper conditioning of the Sx_{IN0} and Sx_{IN1} inputs must be made.

The rising V_{DD} lock-out release threshold ensures all internal logic is properly biased and functional before accepting external switch commands from the inputs. For a falling V_{DD} event, the lock-out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

3.3 Switch Logic

The CPC7512 under-voltage switch lock-out circuitry monitors the V_{DD} supply to ensure proper and safe switch behavior whenever the supply voltage is inadequate.

Under normal V_{DD} supply conditions data applied to the Sx_{IN0} and Sx_{IN1} inputs is controlled by the LATCH. The LATCH, depending on the logic level applied to it's control input $LATCH_x$, will either block the input data or pass the input data to the switch control logic. Once the input data is passed to the switch control logic, the value from the inputs will be locked by the LATCH when the $LATCH_x$ control is asserted to a logic HIGH.

3.3.1 Data Latch

The CPC7512 has two integrated transparent data latches, one for each channel. The latch-enable operation is controlled by TTL input logic levels at the $LATCH_x$ pins. Inputs to the data latch are via the Sx_{IN0} and Sx_{IN1} input pins while the data latch outputs are internal nodes used for state control. When $LATCH_x$, the latch enable control pin, is at a logic 0 the data latch is transparent and the input control signals flow directly through the data latch to the state control circuitry. A change in input will be reflected by a change in the switch state.

Whenever the latch enable control pin is at logic 1, the data latch is active and the control data is locked. Subsequent changes to the Sx_{IN} input control pins will not result in a change to the control logic or affect the existing switch states.

The switches will remain in the state they were in when the $LATCH_x$ changes from logic 0 to logic 1, and will not respond to subsequent changes in input as long as the $LATCH_x$ is at logic 1. TSD however is not constrained by the latch function. Since internal thermal shutdown control is not affected by the state of the latch enable input, TSD will override state control.

3.3.2 TSD Pin Description

The TSD pin is a bidirectional I/O structure with an internal pull-up resistor sourced from V_{DD}. As an output, this pin indicates the status of the thermal shutdown circuitry of the CPC7512. During normal operation this pin will typically be pulled up to V_{DD} but under fault conditions that create excess thermal loading, the entire device will enter thermal shutdown and a logic low will be output at TSD.

As an input, the TSD pin can be used to place the device into the All-Off state by simply pulling the input low. This is a convenient way to temporarily place the device's switches into the off state without the need to cycle the inputs and LATCH controls through an off and then an on sequence. When TSD is released, the device will revert back to it's previous state.

When using TSD as an input, IXYS Integrated Circuits Division recommends the use of an open-collector or an open-drain type output to apply the logic LOW.

Forcing TSD to a logic 1 or tying it to V_{DD} does not affect the CPC7512 thermal shutdown functionality. The device ignores this input level and still enters the thermal shutdown state at high temperature. In other words, the thermal shutdown feature can not be overridden by an external pull-up on the TSD control.

3.4 Power Supplies

Only a +5V logic supply and ground are required by the CPC7512. Switch state control is powered exclusively by the +5V supply. As a result, the CPC7512 exhibits extremely low power consumption during active and idle states.

3.5 Protection

The CPC7512 provides protection for both the low voltage side circuitry it connects to high voltage networks and itself. Two separate layers of protection are interleaved within the device to protect against high-energy high-frequency transients and high-power, low-frequency fault conditions.

3.5.1 Dynamic High Frequency Current Limit

While in a closed switch state, high-frequency high-energy current is restricted by the CPC7512. For the telecom GR-1089-CORE specified ±1000V 10x1000µs lightning pulse with a generator source impedance of 10Ω applied to the high voltage network though a properly clamped external protector, the current seen at the CPC7512 low voltage side interface will be a pulse with a typical magnitude of 1A and a duration less than 0.5µs.

3.5.2 Thermal Shutdown

The thermal-shutdown mechanism activates when the device's die temperature reaches a minimum of 110°C, placing the device into the All-Off state regardless of logic input. During thermal shutdown events the TSD pin will output a logic low with a nominal 0V level. A logic high is output from the TSD pin during normal operation with a typical output level equal to V_{DD}.

If presented with a short-duration transient, such as a lightning event, the thermal-shutdown feature will typically not activate. But, in an extended power-cross event the device temperature will rise and the thermal shutdown mechanism will activate, forcing the device's switches to the All-Off state. At this point the current into the active switch will drop to zero. Once the device enters thermal shutdown, it will remain in the All-Off state until the internal temperature of the device drops below the de-activation level of the thermal-shutdown circuit. This permits the circuit to autonomously return to normal operation. If the fault has not passed, current will again flow and heating will resume, causing the thermal-shutdown mechanism to reactivate. This cycle of entering and exiting the thermal-shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, with an external over-voltage protector present, the external protector will activate shunting the fault current to ground.

3.6 External Protection Elements

The CPC7512 requires only over-voltage protection on the high-voltage side of the switch. Additional external protection may be required on the low-voltage side of the switch if the threshold of the high-voltage side protector exceeds the safe operation of the low-voltage side components. Because the fault current seen by the low-voltage side protector is limited by the switch's high frequency dynamic current limit, the low-voltage side protector need not be as capable as that of the high-voltage side protector. The high-voltage side protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7512. A foldback or crowbar type protector on the high-voltage side is recommended to minimize stresses on the CPC7512.

3.7 Thermal Design Assessment

A successful design utilizing the CPC7512 High-Voltage Analog Switch Array is dependent on careful consideration of the application's environment and the device's thermal constraints. For matters regarding the electrical design, this is simply a case of following the parameters provided in the preceding tables and for many this will be sufficient. However, those designers wishing to push the operational limits envelope with higher switch current and/or higher ambient operating temperatures will need to consider the thermal performance.

Being a real physical device the CPC7512 has a finite thermal capability that when properly considered will ensure appropriate behavior and performance. Determination of the thermal constraint is easily accomplished using the following power equations:

$$P_{TOTAL} = P_{V_{DD}} + \Sigma P_{SW}$$

and

$$P_{TOTAL} = \frac{\Delta T}{\Theta_{JA}}$$

Where $P_{V_{DD}}$ is the dissipated power drawn from the V_{DD} supply and ΣP_{SW} is the total power dissipated by all active switches. The V_{DD} power can be calculated from the "VDD Voltage Supply Specifications" on page 7 while the power dissipated by the switches is the sum of the concurrently active switches. Total switch power is the sum of: the squared maximum current through each active switch times the On-Resistance of the switch (I_{SWx}^2 x R_{ON}).

The second equation is used to calculate the maximum ambient temperature the device can be operated in based on the calculated total power of the previous equation. P_{TOTAL}, the value obtained in the first equation; ΔT, the junction temperature rise of the CPC7512 from ambient; and Θ_{JA}, the thermal impedance of the device package are used to determine the maximum operating ambient temperature.

Using the junction temperature rise equation $\Delta T = T_J - T_A$; the thermal impedance $\Theta_{JA} = 65.8°C/W$; and a maximum junction temperature $T_{J(max)} = 110°C$, the equation reduces to:

$$T_{A(max)} = T_{J(max)} - (P_{TOTAL} \times \Theta_{JA})$$

To avoid entering thermal shutdown, the value for the maximum junction temperature was set to 110°C as specified in the Absolute Maximum Ratings table.

Conversely, it is possible to rework the equations to determine the maximum switch current for a maximum ambient current.

When using the individual switches of the CPC7512 within their allowable operating region, no restrictions are placed on any other switch.

4. Design Example

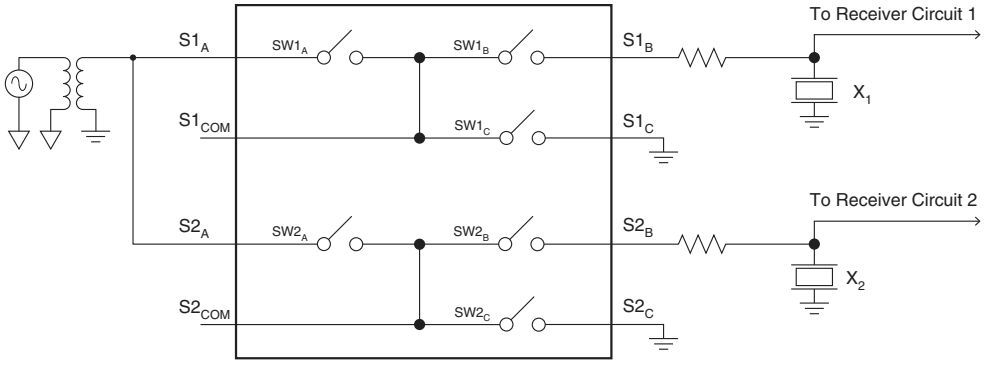
The CPC7512 can be used to provide a multiplexer function in ultrasonic transducer applications allowing the expense and the PCB real estate consumption of a transducer drive circuitry to be spread across multiple transducers. The steps to implement this concept are shown in the minimal two channel example below.

To maximize isolation between the drive circuit and non-driven transducer receiver circuits, the Sx_C terminal must be connected to ground.

4.1 Startup State Following Power Up

To facilitate a stable and safe power up transition or recovery from a supply voltage droop, all of the switches in the CPC7512 are preconditioned to the All-Off state upon power up. As can be seen in the figure below, all of the switches are open.

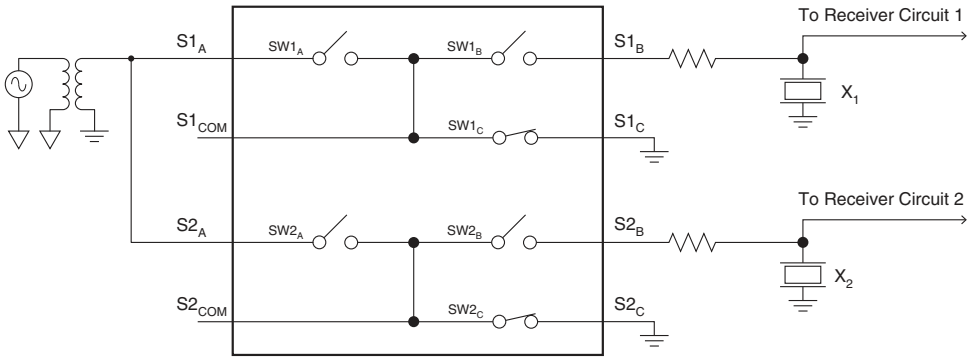
Figure 6: Power Up Default State



4.2 Initial Configuration State

Following power up, the switches should be placed in the high impedance shunt isolation state. To provide maximum shunt isolation, switches $SW1_C$ and $SW2_C$ must be terminated to ground and the switches enabled (Closed). This state minimizes signal transfer through the open A and B switches.

Figure 7: Switches A and B Open With Shunt Isolation Enabled

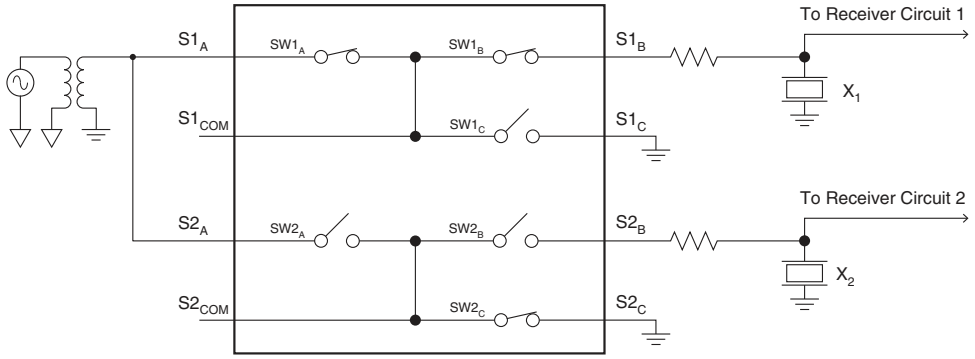


4.3 Driving Channel 1 Ultrasonic Transducer X1

To drive X1, the first transducer, switches $SW1_A$ and $SW1_B$ are closed and switch $SW1_C$ is opened. The closed switches pass the high voltage 40-50kHz signal output by the drive circuitry through the series resistor to the transducer.

In Channel 2, the portion of the high-voltage, high-frequency signal output by the drive circuitry that passes through the open $SW2_A$ switch is shunted to ground through the closed $SW2_C$ switch.

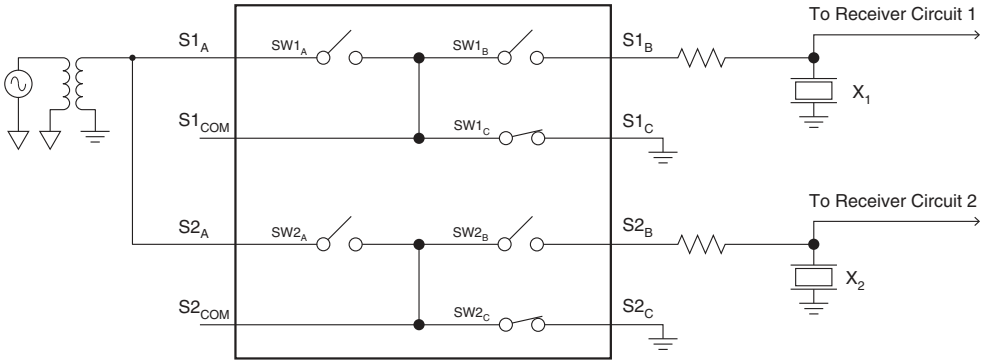
Figure 8: Driving Ultrasonic Transducer X1



4.4 Ultrasonic Transducer X1 Drive Complete

Once the transducer is energized it is separated from the generator by opening Switches $SW1_A$ and $SW1_B$. This prevents the large stimulus source voltage from overwhelming the transducer's much smaller output voltage created from the energy of the reflected ultrasonic pulse. To assist in minimizing corruption of the X1 transducer's output signal, $SW1_C$ is closed. This enhances switch isolation. The X1 transducer's output voltage is picked up by Receiver Circuit 1 and sent on to the microcontroller.

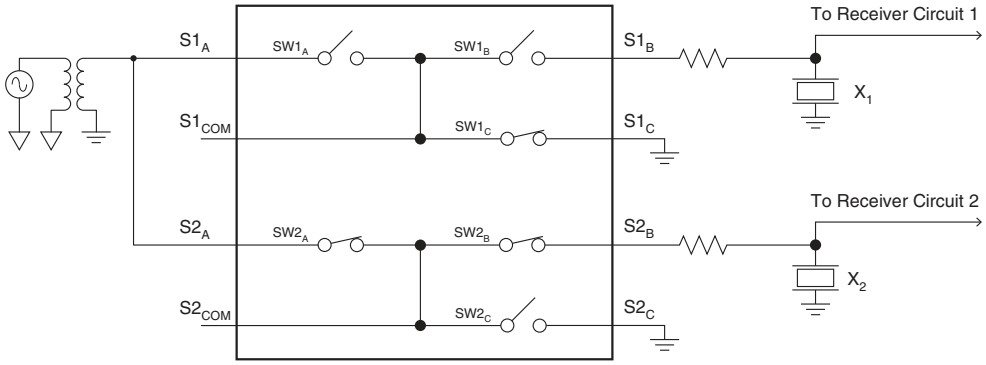
Figure 9: Separating Drive Circuitry From Transducer X1



4.5 Driving Channel 2 Ultrasonic Transducer X2

Following the driving of transducer X1, the second transducer can be stimulated. The procedure for Channel 2 is the same as that of Channel 1.

Figure 10: Driving Ultrasonic Transducer X2



For larger systems additional CPC7512's can be used allowing expansion of the single drive circuitry to as many transducers as needed.

5. Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC7512Z	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

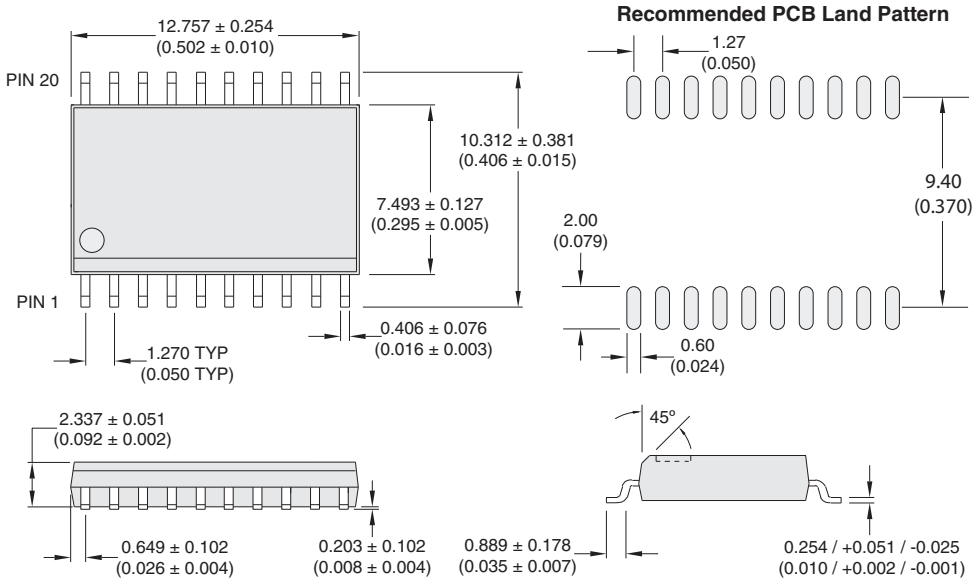
Device	Maximum Temperature x Time	Maximum Reflow Cycles
CPC7512Z	260°C for 30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

5.5 Mechanical Dimensions

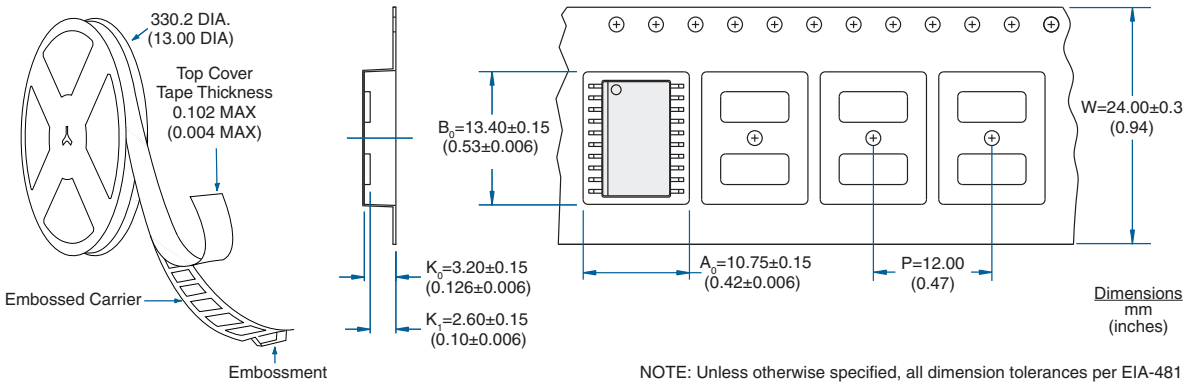
5.5.1 CPC7512Z Package Dimensions



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).

DIMENSIONS
mm
(inches)

5.5.2 CPC7512ZTR Tape & Reel Specification



Dimensions
mm
(inches)

NOTE: Unless otherwise specified, all dimension tolerances per EIA-481

For additional information please visit www.ixysic.com

Specifications: DS-CPC7512-R01

2/27/2015