TPS65182x PMIC For E Ink® Vizplex™-Enabled Electronic Paper Display

1 Features

- Single Chip Power Management Solution for E Ink® Vizplex™ Electronic Paper Displays
- Generates Positive and Negative Gate and Source Driver Voltages and Back-Plane Bias from a Single, Low-Voltage Input Supply
- 3-V to 6-V Input Voltage Range
- Boost Converter for Positive Rail Base
- Inverting Buck-Boost Converter for Negative Rail Base
- Two Adjustable LDOs for Source Driver Supply
  - LDO1: 15 V, 120 mA (VPOS)
  - LDO2: –15 V, 120 mA (VNEG)
- Accurate Output Voltage Tracking
  - VPOS - VNEG = ±50 mV
- Two Charge Pumps for Gate Driver Supply
  - CP1: 22 V, 10 mA (VDDH)
  - CP2: –20 V, 12 mA, (VEE)
- Adjustable VCOM Driver for Accurate Panel-Backplane Biasing
  - –0.3 V to –2.5 V
  - Adjustable Through External Potentiometer
  - 15-mA Max Integrated Switch
- Thermistor Monitoring
  - –10°C to 85°C Temperature Range
  - ±1°C Accuracy from 0°C to 50°C
- I^2C Serial Interface
  - Slave Address 0x48h (1001000)
- Flexible Power-Up Sequencing
- Sleep Mode Support
- Thermally Enhanced Package for Efficient Heat Management
  (48-Pin 7 mm × 7 mm × 0.9 mm VQFN)

2 Applications

- Power Supply for Active Matrix E Ink Vizplex Panels
- E-Book Readers
- EPSON® S1D13522 (ISIS) Timing Controller
- EPSON S1D13521 (Broadsheet) Timing Controller
- Application Processors With Integrated or Software Timing Controller (OMAP™)

3 Description

The TPS65182x device is a single-chip power supplies designed to for E Ink Vizplex displays used in portable e-reader applications and support panel sizes up to 9.7 inches. Two high efficiency DC/DC boost converters generate ±17-V rails which are boosted to 22 V and –20 V by two change pumps to provide the gate driver supply for the Vizplex panel.

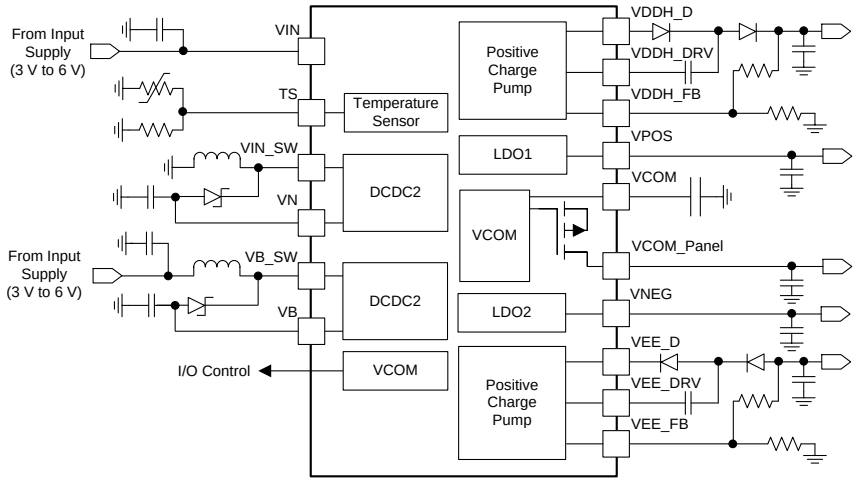
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65182(2)	VQFN (48)	7.00 mm × 7.00 mm
TPS65182B		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Not recommended for new design.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2010) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Description (continued)

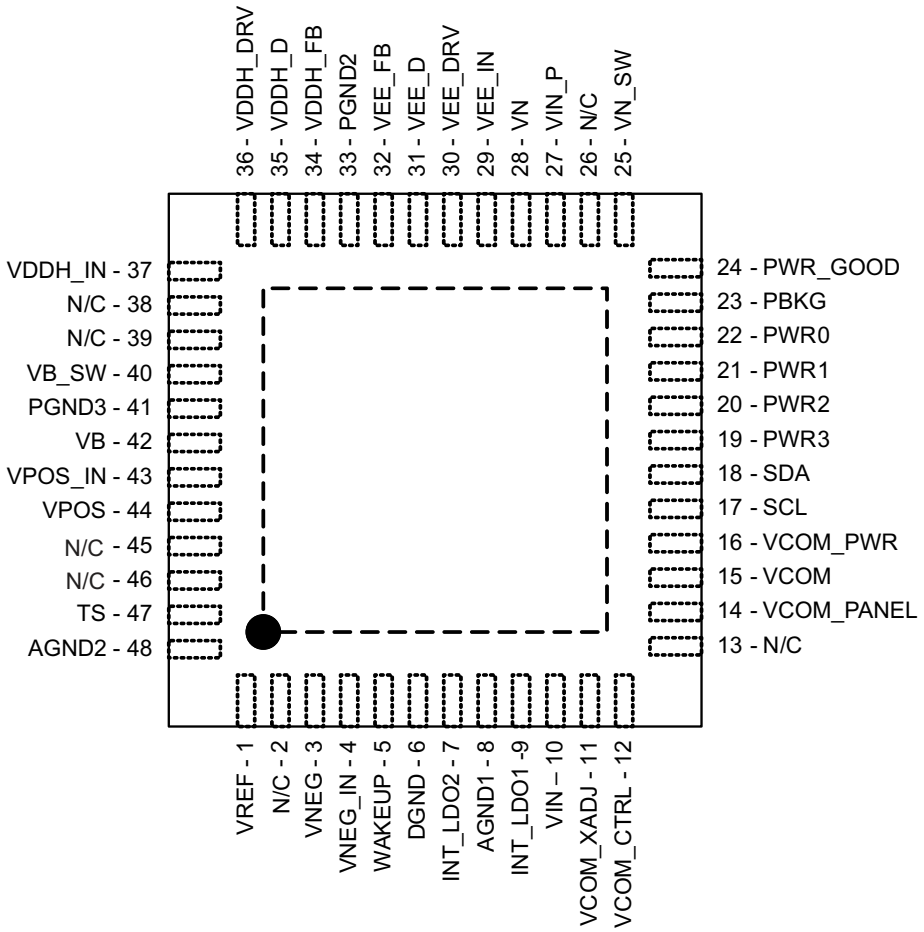
Two tracking LDOs create the ±15-V source driver supplies which support up to 120-mA of output current. All rails are adjustable through the I^2C interface to accommodate specific panel requirements.

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by an external resistor or the I^2C interface. The VCOM driver can source or sink current depending on panel condition.

The TPS65182x provides precise temperature measurement function to monitor the panel temperature during operation. The temperature reading is updated every 60 s and can be accessed through the I^2C interface.

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION(1)
NO.	NAME		
1	VREF	O	Filter pin for 2.25-V internal reference to ADC
2	N/C	—	Not connected
3	VNEG	O	Negative supply output pin for panel source drivers
4	VNEG_IN	I	Input pin for LDO2 (VNEG)
5	WAKEUP	I	Wake up pin (active high). Pull this pin high to wake up from sleep mode.
6	DGND	—	Digital ground
7	INT_LDO2	O	Internal supply (digital circuitry) filter pin
8	AGND1	—	Analog ground for general analog circuitry
9	INT_LDO1	O	Internal supply (analog circuitry) filter pin
10	VIN	I	Input power supply to general circuitry
11	VCOM_XADJ	I	Analog input for conventional VCOM setup method. Tie this pin to ground if VCOM is set through I^2C interface.

(1) There will be 0-ns, 93.75-µs, 62.52-µs of deglitch for PWRx, WAKEUP, and VCOM_CTRL, respectively.

Pin Functions (continued)

PIN		I/O	DESCRIPTION(1)
NO.	NAME		
12	VCOM_CTRL	I	VCOM_PANEL gate driver enable (active high)
13	N/C	—	Not connected
14	VCOM_PANEL	O	Panel common-voltage output pin
15	VCOM	O	Filter pin for panel common-voltage driver
16	VCOM_PWR	I	Internal supply input pin to VCOM buffer. Connect to the output of DCDC2.
17	SCL	I	Serial interface (I^2C) clock input
18	SDA	I/O	Serial interface (I^2C) data input/output
19	PWR3	I	Enable pin for CP1 (VDDH) (active high)
20	PWR2	I	Enable pin for LDO1 (VPOS) (active high)
21	PWR1	I	Enable pin for CP2 (VEE) (active high)
22	PWR0	I	Enable pin for LDO2 (VNEG) and VCOM (active high)
24	PWR_GOOD	O	Open drain power good output pin (active low)
25	VN_SW	O	Inverting buck-boost converter switch out (DCDC2)
26	N/C	—	Not connected
27	VIN_P	I	Input power supply to inverting buck-boost converter (DCDC2)
28	VN	I	Feedback pin for inverting buck-boost converter (DCDC2)
29	VEE_IN	I	Input supply pin for CP1 (VEE)
30	VEE_DRV	O	Driver output pin for negative charge pump (CP2)
31	VEE_D	O	Base voltage output pin for negative charge pump (CP2)
32	VEE_FB	I	Feedback pin for negative charge pump (CP2)
33	PGND2	—	Power ground for CP1 (VDDH) and CP2 (VEE) charge pumps
34	VDDH_FB	I	Feedback pin for positive charge pump (CP1)
35	VDDH_D	O	Base voltage output pin for positive charge pump (CP1)
36	VDDH_DRV	O	Driver output pin for positive charge pump (CP1)
37	VDDH_IN	I	Input supply pin for positive charge pump (CP1)
38	N/C	—	Not connected
39	N/C	—	Not connected
40	VB_SW	O	Boost converter switch out (DCDC1)
41	PGND3	—	Power ground for DCDC1
42	VB	I	Feedback pin for boost converter (DCDC1)
43	VPOS_IN	I	Input pin for LDO1 (VPOS)
44	VPOS	O	Positive supply output pin for panel source drivers
45	N/C	—	Not connected
46	N/C	—	Not connected
47	TS	I	Thermistor input pin. Connect a 10k NTC thermistor and a 43k linearization resistor between this pin and AGND2.
48	AGND2	—	Reference point to external thermistor and linearization resistor
23	PowerPad (PBKG)	—	Die substrate/thermal pad. Connect to VN with short, wide trace. Wide copper trace will improve heat dissipation. PowerPad must not be connected to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
	Input voltage range at VIN, VINP	–0.3	7	V
	Ground pins to system ground	–0.3	0.3	V
	Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD	–0.3	3.6	V
	VCOM_XADJ	–3.6	0.3	V
	Voltage on VB, VB_SW, VPOS_IN, VDDH_IN	–0.3	20	V
	Voltage on VN, VNEG_IN, VEE_IN, VCOM_PWR	–20	0.3	V
	Voltage from VINP to VN_SW	–0.3	30	V
	Peak output current		Internally limited	mA
	Continuous total power dissipation		2	W
T_J	Operating junction temperature	–10	125	°C
T_A	Operating ambient temperature (3)	–10	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) It is recommended that copper plane in proper size on board be in contact with die thermal pad to dissipate heat efficiently. Thermal pad is electrically connected to PBKG, which is supposed to be tied to the output of buck-boost converter. Thus wide copper trace in the buck-boost output will help heat dissipated efficiently.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input voltage range at VIN, VINP	3	3.7	6	V
	Voltage range at SDA, SCL, WAKEUP, PWR3, PWR2, PWR1, PWR0, VCOM_CTRL, VDDH_FB, VEE_FB, VCOM_XADJ, PWR_GOOD	0		3.6	V
T_A	Operating ambient temperature	–10		85	°C
T_J	Operating junction temperature	–10		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65182x RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Estimated when mounted on high K JEDEC board per JESD 51-7 with thickness of 1.6 mm, 4 layers, size of 76.2 mm X 114.3 mm, and 2 oz. copper for top and bottom plane. Actual thermal impedance will depend on PCB used in the application.

7.5 Electrical Characteristics

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{IN}	Input voltage range		3	3.7	6	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.9		V
V_{HYS}	Undervoltage lockout hysteresis	V_{IN} rising		400		mV
INPUT CURRENT						
I_Q	Operating quiescent current into VIN	Device switching, no load		5.5		mA
I_{STD}	Operating quiescent current into VIN	Device in standby mode		130		µA
I_{SLEEP}	Shutdown current	Device in sleep mode		2.8	10	µA
INTERNAL SUPPLIES						
VI_{NT_LDO1}	Internal supply			2.7		V
V_{INT_LDO2}	Internal supply			2.7		V
V_{REF}	Internal supply			2.25		V
DCDC1 (POSITIVE BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
V_{OUT}	Output voltage range			17		V
	DC set tolerance		–5%		5%	
I_{OUT}	Output current				160	mA
$R_{DS(ON)}$	MOSFET on resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5		A
	Switch current accuracy		–30%		30%	
f_{SW}	Switching frequency			1		MHz
L	Inductor			2.2		µH
C	Capacitor			2x4.7		µF
ESR	Capacitor ESR			20		mΩ
DCDC2 (INVERTING BUCK-BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
V_{OUT}	Output voltage range			–17		V
	DC set tolerance		–5%		5%	
I_{OUT}	Output current				160	mA
$R_{DS(ON)}$	MOSFET on resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5		A
	Switch current accuracy		–30%		30%	

Electrical Characteristics (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L	Inductor			4.7		µH
C	Capacitor			2x4.7		µF
ESR	Capacitor ESR			20		mΩ
LDO1 (VPOS)						
V_{POS_IN}	Input voltage range		16.15	17	17.85	V
V_{SET}	Output voltage set value	V_{IN} = 17 V	14.25	15	15.75	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = 17 V		250		mV
V_{POS_OUT}	Output voltage range	V_{SET} = 15 V, I_{LOAD} = 20 mA	14.85	15	15.15	V
V_{OUTTOL}	Output tolerance	V_{SET} = 15 V, I_{LOAD} = 20 mA	–1%		1%	
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90%			1%	
I_{LOAD}	Load current range			120		mA
I_{LIMIT}	Output current limit		200			mA
T_{SS}	Soft start time			1		ms
C	Recommended output capacitor			4.7		µF
LDO2 (VNEG)						
V_{NEG_IN}	Input voltage range		–17.85	–17	–16.15	V
V_{SET}	Output voltage set value	V_{IN} = –17 V	–15.75	–15	–14.25	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = –17 V		250		mV
V_{NEG_OUT}	Output voltage range	V_{SET} = –15 V, I_{LOAD} = –20 mA	–15.15	–15	–14.85	V
V_{OUTTOL}	Output tolerance	V_{SET} = –15 V, I_{LOAD} = –20 mA	–1%		1%	
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90%			1%	
I_{LOAD}	Load current range			120		mA
I_{LIMIT}	Output current limit		200			mA
T_{SS}	Soft start time			1		ms
C	Recommended output capacitor			4.7		µF
LD01 (POS) AND LDO2 (VNEG) TRACKING						
V_{DIFF}	Difference between VPOS and VNEG	V_{SET} = ±15 V, I_{LOAD} = ±20 mA, 0°C to 60°C	–50		50	mV
VCOM DRIVER						
V_{COM}	Output voltage range		–2.5		–0.3	V
G	V_{COM} gain (V_{COM_XADJ}/V_{COM})	V_{COM_ADJ} = 0 V		1		V/V
VCOM SWITCH						
T_{ON}	Switch ON time	V_{COM} = –1.25 V, V_{COM_PANEL} = 0 V C_{VCOM} = 4.7 µF, C_{VCOM_PANEL} = 4.7 µF			1	ms
$R_{DS(ON)}$	MOSFET ON resistance	V_{COM} = –1.25 V, I_{COM} = 30 mA		20	35	Ω
I_{LIMIT}	MOSFET current limit	Not tested in production		200		mA
I_{SWLEAK}	Switch leakage current	V_{COM} = 0 V, V_{COM_PANEL} = –2.5 V			8.3	nA
CP1 (VDDH) CHARGE PUMP						
V_{DDH_IN}	Input voltage range		16.15	17	17.85	V
V_{FB}	Feedback voltage			1		V
	Accuracy		–3%		3%	
V_{DDH_OUT}	Output voltage range	V_{SET} = 22 V, I_{LOAD} = 2 mA	21	22	23	V
I_{LOAD}	Load current range				10	mA
f_{SW}	Switching frequency			560		KHz

Electrical Characteristics (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_D	Recommended driver capacitor			10		nF
C_O	Recommended output capacitor			4.7		µF
CP2 (VEE) NEGATIVE CHARGE PUMP						
V_{EE_IN}	Input voltage range		–17.75	–17	–16.15	V
V_{FB}	Feedback voltage			–1		V
	Accuracy		–3%		3%	
V_{EE_OUT}	Output voltage range	V_{SET} = –20 V, I_{LOAD} = 3 mA	–21	–20	–19	V
I_{LOAD}	Load current range				12	mA
f_{SW}	Switching frequency			560		KHz
C_D	Recommended driver capacitor			10		nF
C_O	Recommended output capacitor			4.7		µF
THERMISTOR MONITOR(1)						
A_{TMS}	Temperature to voltage ratio	Not tested in production		–0.0158		V/°C
$Offset_{TMS}$	Offset	Temperature = 0°C		1.575		V
V_{TMS_HOT}	Temp hot trip voltage (T = 50°C)	TEMP_HOT_SET = 0x8C		0.768		V
V_{TMS_COOL}	Temp hot escape voltage (T = 45°C)	TEMP_COOL_SET = 0x82		0.845		V
V_{TMS_MAX}	Maximum input level			2.25		V
R_{NTC_PU}	Internal pull up resistor			7.307		KΩ
R_{LINEAR}	External linearization resistor			43		KΩ
ADC_{RES}	ADC resolution	Not tested in production, 1 bit		16.1		mV
ADC_{DEL}	ADC conversion time	Not tested in production		19		µs
$TMST_{TOL}$	Accuracy	Not tested in production	–1		1	LSB
LOGIC LEVELS AND TIMING CHARTERISTICS (SCL, SDA, PWR_GOOD, PWRx, WAKEUP)						
V_{OL}	Output low threshold level	I_O = 3 mA, sink current (SDA, PWR_GOOD)			0.4	V
V_{IL}	Input low threshold level				0.4	V
V_{IH}	Input high threshold level		1.2			V
$I_{(bias)}$	Input bias current	V_{IO} = 1.8 V			1	µA
$t_{low,WAKEUP}$	WAKEUP low time	minimum low time for WAKEUP pin	150			ms
f_{SCL}	SCL clock frequency				400	KHz
OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A = –40°C to 85°C	–10%		10%	
THERMAL SHUTDOWN						
T_{SHTDWN}	Thermal trip point			150		°C
	Thermal hysteresis			20		°C

(1) 10-KΩ Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43 KΩ, 1%) are used at TS pin for panel temperature measurement.

7.6 Data Transmission Timing

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency		100		400	KHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{BUF}	Bus Free Time Between Stop and Start Condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Pulse width of spikes which mst be suppressed by the input filter	SCL = 100 KHz	n/a		n/a	ns
		SCL = 400 KHz	0		50	
C_b	Capacitive load for each bus line	SCL = 100 KHz			400	pF
		SCL = 400 KHz			400	

7.7 Typical Characteristics

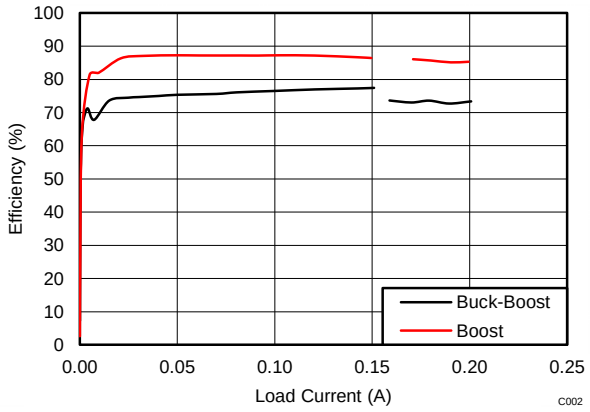


Figure 1. Efficiency vs Load Current

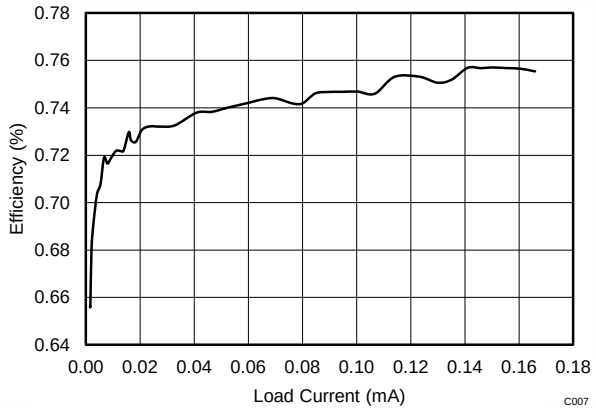


Figure 2. Load Current vs Efficiency

8 Detailed Description

8.1 Overview

The TPS65182x family of devices provides two adjustable LDOs, inverting buck-boost converter, boost converter, thermistor monitoring, and flexible power-up and power-down sequencing. The system can be supplied by a regulated input voltage ranging from 3 V to 6 V. The device is characterized across a –10°C to 85°C temperature range, best suited for personal electronic applications.

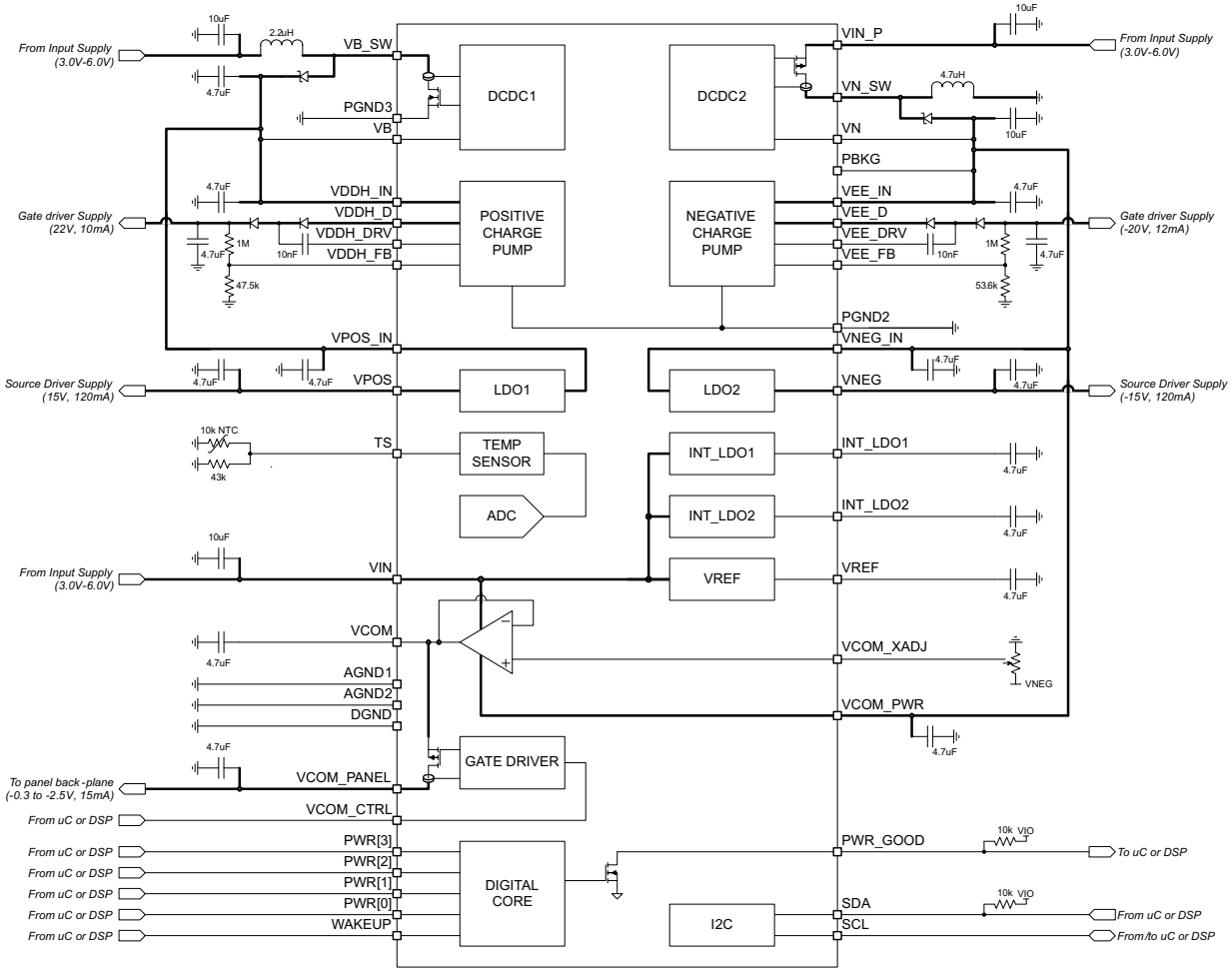
The I_2C interface provides comprehensive features for using the TPS65182x family of devices. All rails can be enabled or disabled. Power-up and power-down sequences can also be programmed through the I_2C interface, as well as thermistor and interrupt configurations. Voltage adjustment can also be controlled through the I_2C interface.

The adjustable LDOs can supply up to 120 mA of current. The default output voltages for each LDO can be adjusted through the I_2C interface. LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign, but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be less than 50 mv.

There are two charge pumps: VDDH and VEE 10 mA and 12 mA respectively. These charge pumps boost the DC-DC boost converters ±16-V rails to provide a gate channel supply. The power good functionality is open-drain output, if any of the four power rails (CP1, CP2, LDO1, LDO2) are not in regulation, encounters a fault, or is disabled, the pin is pulled low. PWR_GOOD remains low if one of the rails is not enabled by the host, and only after all rails are in regulation, PWR_GOOD is released to HiZ state (pulled up by external resistor).

The TPS65182x family of devices provides circuitry to bias and measure an external NTC to monitor the display panel temperature in a range from –10°C to 85°C with an accuracy of ±1°C from 0°C to 50°C. Temperature measurements are triggered by the controlling host and the last temperature reading is always stored in the TMST_VALUE register. Interrupts are issued when the temperature exceeds the programmable HOT, or drops below the programmable COLD threshold, or when the temperature has changed by more than a user-defined threshold from the baseline value.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Modes of Operation

The TPS65182x has three modes of operation, SLEEP, STANDBY, and ACTIVE. SLEEP mode is the lowest-power mode in which all internal circuitry is turned off. In STANDBY, all power rails are shut down but the device is ready to accept commands through PWR[3:0] pins and/or I^2C interface. In ACTIVE mode one or more power rails are enabled.

SLEEP This is the lowest power mode of operation. All internal circuitry is turned off and the device does not respond to I^2C communications. TPS65182x enters SLEEP mode whenever WAKEUP pin is pulled low.

STANDBY In STANDBY all internal support circuitry is powered up and the device is ready to accept commands either through GPIO or I^2C control but none of the power rails are enabled. To enter STANDBY mode the WAKEUP pin must be pulled high and all PWRx pins must be pulled low. The device also enters STANDBY mode if input under voltage lock out (UVLO), positive boost under voltage (VB_UV), or inverting buck-boost under voltage (VN_UV) is detected, or thermal shutdown occurs.

ACTIVE The device is in ACTIVE mode when any of the output rails are enabled and no fault condition is present. This is the normal mode of operation while the device is powered up. In ACTIVE mode, a falling edge on any PWRx pin shuts down and a rising edge powers up the corresponding rail.

Feature Description (continued)

8.3.2 Mode Transistions

SLEEP → ACTIVE WAKEUP pin is pulled high (rising edge) with any PWRx pin high. Rails come up in a pre-defined power-up sequence.

SLEEP → STANDBY WAKEUP pin is pulled high (rising edge) with all PWRx pins low. Rails will remain down until one or more PWRx pin is pulled high.

ACTIVE → SLEEP WAKEUP pin is pulled low (falling edge). Rails are shut down following the pre-defined power-down sequence.

ACTIVE → STANDBY WAKEUP pin is high. All PWRx pins are pulled low (falling edge). Rails shut down in the order in which PWRx pins are pulled low. In the event of thermal shut down (TSD), under voltage lock out (UVLO), positive boost or inverting buck-boost under voltage (UV), the device shuts down all rails in a pre-defined power-down sequence.

STANDBY → ACTIVE WAKEUP pin is high and any PWRx pin is pulled high (rising edge). Rails come up in the same order as PWRx pins are pulled high.

STANDBY → SLEEP WAKEUP pin is pulled low (falling edge) while none of the output rails are enabled.

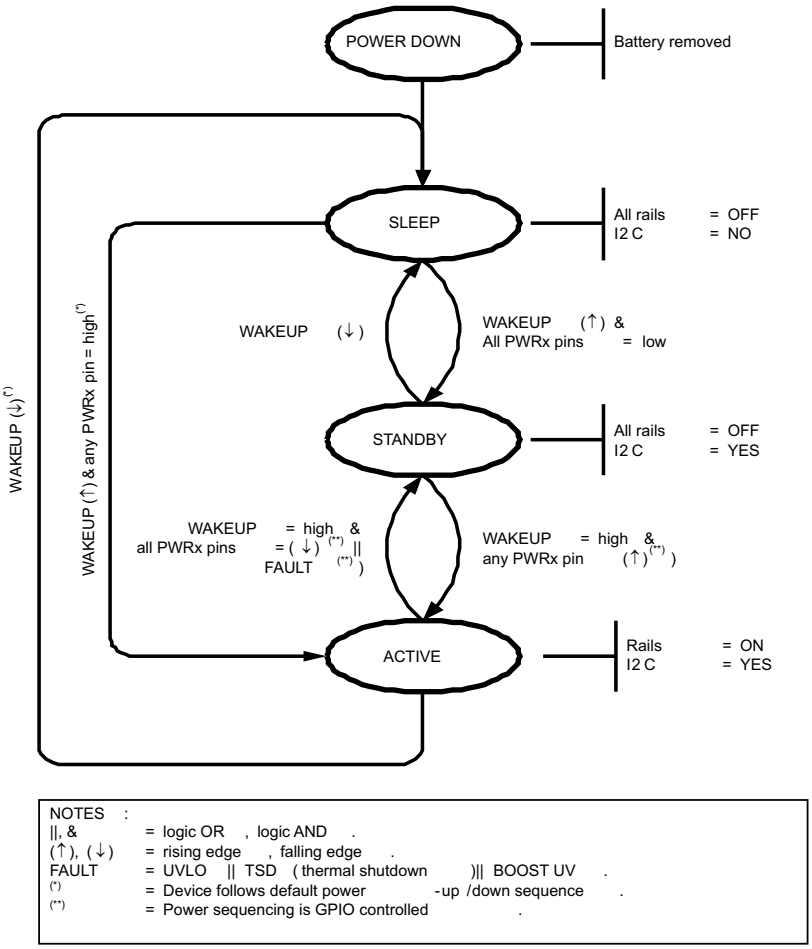


Figure 3. Global State Diagram

Feature Description (continued)

8.3.3 Wake-Up and Power Up Sequencing

The TPS65182x supports a default power-up sequence supporting E Ink Vizplex displays. It also offers full user control of the power-up sequence through GPIO control using the PWR3, 2, 1, 0 pins. Using GPIO control, the output rails are enabled/disabled in the order in which the PWRx pins are asserted/de-asserted, respectively, and the power-up timing is controlled by the host only. Rails are in regulation 2 ms after their respective PWRx pin has been asserted with the exception of the first rail, which takes 6 ms to power up. The additional time is needed to power up the positive and inverting buck-boost regulator which need to be turned on before any other rail can be enabled. Once all rails are enabled and in regulation the PWR_GOOD pin is released (pin status = HiZ and power good line is pulled high by external pull-up resistor). The PWRx pins are assigned to the rails as follows:

- PWR0: LDO2 (VNEG) and VCOM
- PWR1: CP2 (VEE)
- PWR3: LDO2 (VPOS)
- PWR4: CP1 (VDDH)

Rails are powered down whenever the host de-asserts the respective PWRx pin, and once all rails are disabled the device enters STANDBY mode. The next step is then to de-assert the WAKEUP pin to enter SLEEP mode which is the lowest-power mode of operation.

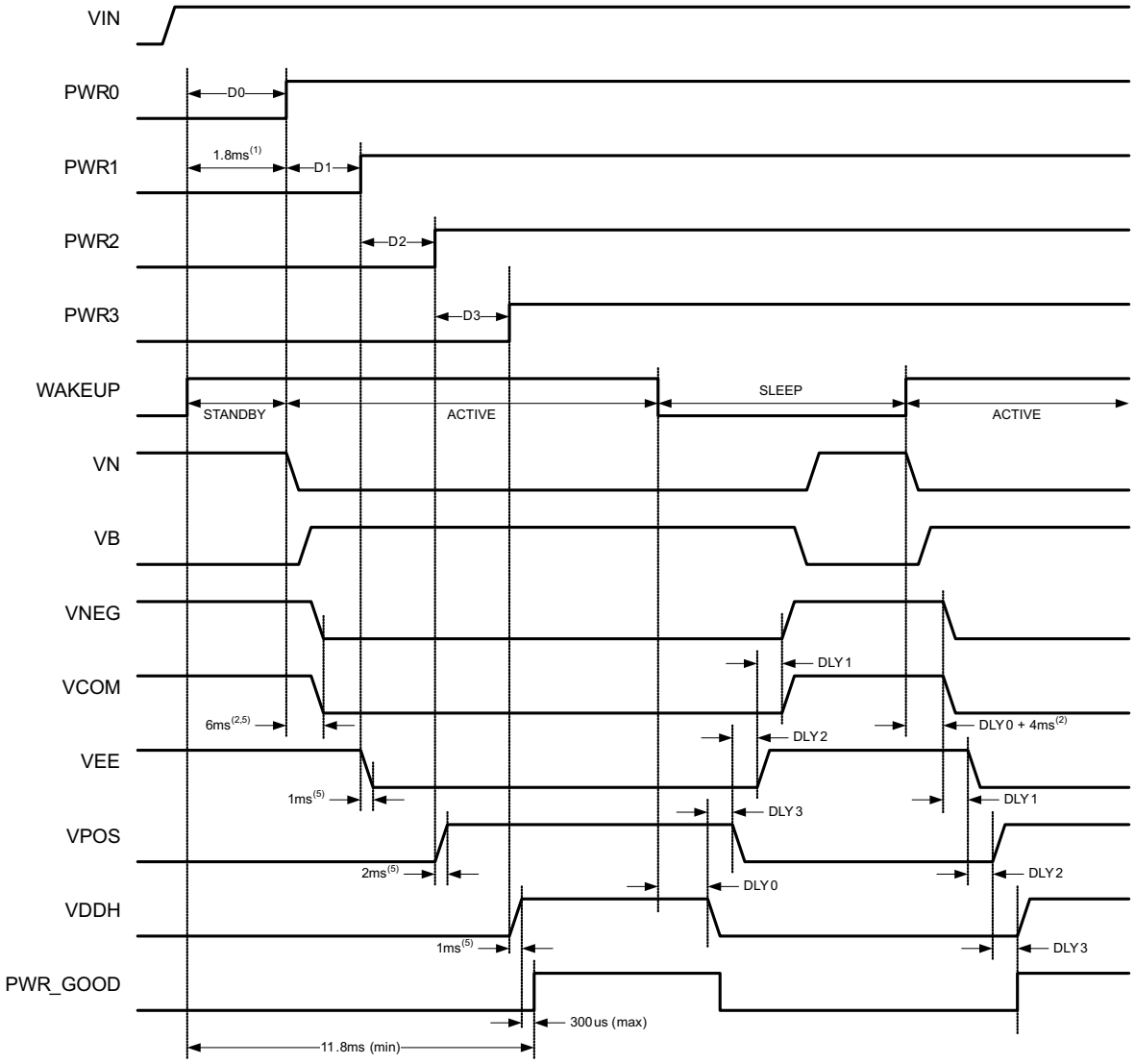
It is possible for the host to force the TPS65182x directly into SLEEP mode from ACTIVE mode by de-asserting the WAKEUP pin in which case the device follows the pre-defined power-down sequence before entering SLEEP mode.

8.3.4 Dependencies Between Rails

Charge pumps, LDOs, and VCOM driver are dependent on the positive and inverting buck-boost converters and several dependencies exist that affect the power-up sequencing. These dependencies are listed below.

1. Inverting buck-boost (DCDC2) must be in regulation before positive boost (DCDC1) can be enabled. Internally, DCDC1 enable is gated by DCDC2 power good.
2. Positive boost (DCDC1) must be in regulation before LDO2 (VNEG) can be enabled. Internally LDO2 enable is gated DCDC1 power-good.
3. Positive boost (DCDC1) must be in regulation before VCOM can be enabled; Internally VCOM enable is gated by DCDC1 power good.
4. Positive boost (DCDC1) must be in regulation before negative charge pump (CP2) can be enabled. Internally CP2 enable is gated by DCDC1 power good.
5. Positive boost (DCDC1) must be in regulation before positive charge pump (CP1) can be enabled. Internally CP1 enable is gated by DCDC1 power good.
6. LDO2 must be in regulation before LDO1 can be enabled. Internally LDO1 enable is gated by LDO2 power good.
7. The minimum delay time between any two PWRx pins must be > 62.5 µs in order to follow the power up sequence defined by GPIO control. If any two PWRx pins are pulled up together (< 62.5 µs apart) rails will be staggered in a manner that a subsequent rail's enable is gated by PG of a preceding rail. In this case, the default order of power-up is LDO2 (VNEG), CP2 (VEE), LDO1 (VPOS), and CP1(VDDH). If any two PWRx pins are pulled low then all rails will go down at the same time.

Feature Description (continued)



(1) Minimum delay time between WAKEUP rising edge and IC rady to accept I 2C transaction.
(2) It takes 2ms minimum for each internal boost regulator to start up before VNEG can be enabled .
(5) It takes up to 2ms for LDOs (VPOS,VNEG) and 1ms for charge pumps (VDDH,VEE), to reach their steady state after being enabled.
DLY0-DLY3 are power up/down delays are factory-set to 2ms.

Figure 4. Power-Up and Power-Down Timing Diagram

8.3.5 Soft-Start

Softstart for DCDC1, DCDC2, LDO1, and LDO2 is accomplished by lowering the current limits during start-up. If DCDC1 or DCDC2 are unable to reach power-good status within 10 ms, the device enters STANDBY mode.

8.3.6 VCOM Adjustment

VCOM can be adjusted by an external potentiometer by connecting a potentiometer to the VCOM_XADJ pin. The potentiometer must be connected between ground and a negative supply. The gain from VCOM_XADJ to VCOM is 1 and therefore the voltage applied to VCOM_XADJ pin should range from -0.3 to -2.5V.

8.3.7 VPOS and VNEG Supply Tracking

LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be < 50 mV.

Feature Description (continued)

8.3.8 Fault Handling and Recovery

The TPS65182x monitors input and output voltages and die temperature and will take action if operating conditions are outside normal limits. Whenever the TPS65182x encounters:

- Thermal Shutdown (TSD)
- Positive Boost Under Voltage (VB_UV)
- Inverting Buck-Boost Under Voltage (VN_UV)
- Input Under Voltage Lock Out (UVLO)

it will shut down all power rails and enter STANDBY mode. Shut down follows the pre-defined power-down sequence and once a fault is detected, the PWR_GOOD pin is pulled low.

Whenver the TPS65182x encounters under voltage on VNEG (VNEG_UV), VPOS (VPOS_UV), VEE (VEE_UV) or VDDH (VDDH_UV) it will shut down the corresponding rail (plus any dependent rail) only and remain in ACTIVE mode, allowing the DCDC converters to remain up. Again, the PWR_GOOD pin will be pulled low.

As the PWRx inputs are edge sensitive, the host must toggle the PWRx pins to re-enable the rails through GPIO control, i.e. it must bring the PWRx pins low before asserting them again.

8.3.9 Power Good Pin

The power good pin (PWR_GOOD) is an open drain output that is pulled high when all four power rails (CP1, CP2, LDO1, LDO2) are in regulation and is pulled low if any of the rails encounters a fault. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to HiZ state (pulled up by external resistor).

8.3.10 Panel Temperature Monitoring

The TPS65182x provides circuitry to bias and measure an external negative temperature coefficient resistor (NTC) to monitor device temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. Temperature reading is automatically updated every 60 s.

8.3.11 NTC Bias Circuit

Figure 5 below shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25-V reference voltage through an integrated 7.307-KΩ bias resistor. A 43-KΩ resistor is connected parallel to the NTC to linearize the temperature response curve. The circuit is designed to work with a nominal 10-KΩ NTC and achieves accuracy of ±1°C from 0°C to 50°C. The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 1.

Feature Description (continued)

Table 1. ADC Output Value vs Termperature

TEMPERATURE	TMST_VALUE[7:0]
< -10°C	1111 0110
-10°C	1111 0110
-9°C	1111 0111
...	...
-2°C	1111 1110
-1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
2°C	0000 0010
...	...
25°C	0001 1001
...	
85°C	0101 0101
> 85°C	0101 0101

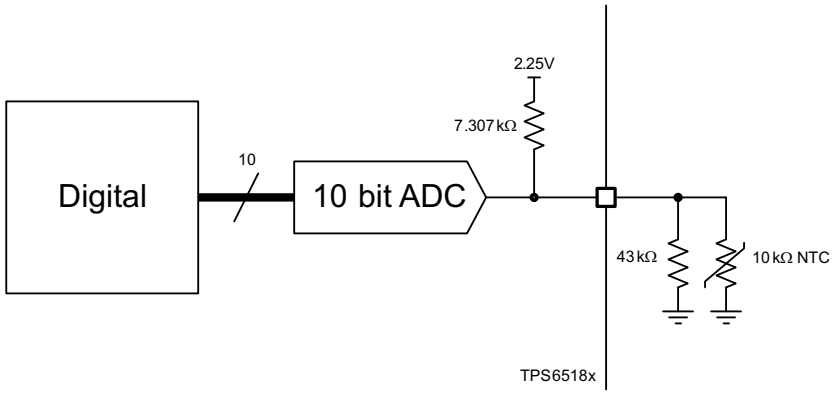


Figure 5. NTC Bias and Measurement Circuit

8.4 Device Functional Modes

8.4.1 I²C Bus Operation

The TPS65182x supports a special I²C mode making it compatible with the EPSON® Broadsheet S1D13521 timing controller. Standard I²C protocol requires the following steps to read data from a register:

1. Send device slave address, R/nW bit set low (write command)
2. Send register address
3. Send device slave address, R/nW set high (read command)
4. The slave will respond with data from the specified register address.end device slave address, R/nW set high (read command).

The EPSON® Broadsheet S1D13521 controller does not support I²C writes nor I²C reads from addressed registers, therefore the TPS65182x I²C interface has been modified and the reading the temperature data is reduced to two steps:

1. Send device address, R/nW set high (read command)
2. Read the data from the slave. The slave will respond with data from TMST_VALUE register address.

Device Functional Modes (continued)

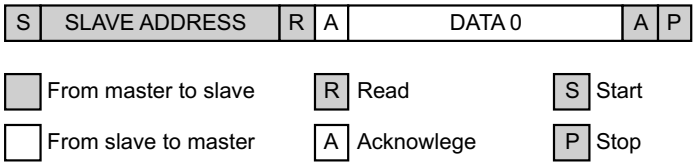


Figure 6. Subaddress in I²C Transmission

The I²C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open Drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 7. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. Reference Figure 7.

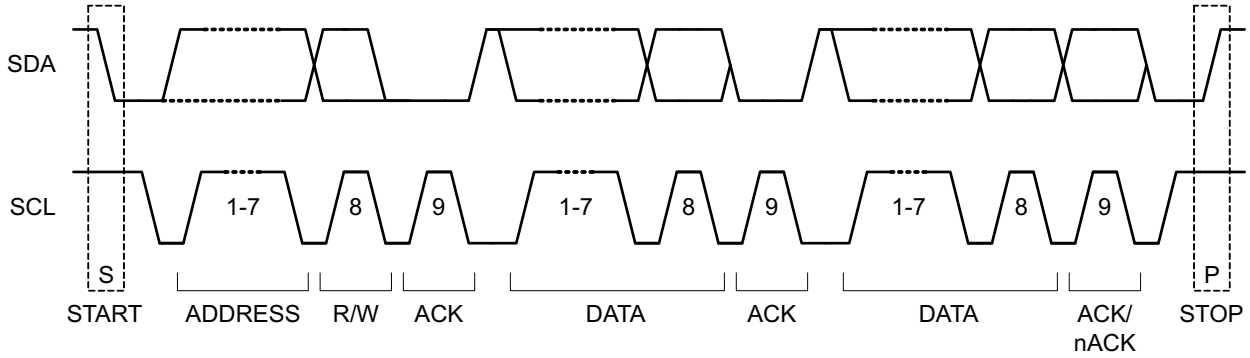


Figure 7. I²C Start/Stop/Acknowledge Protocol

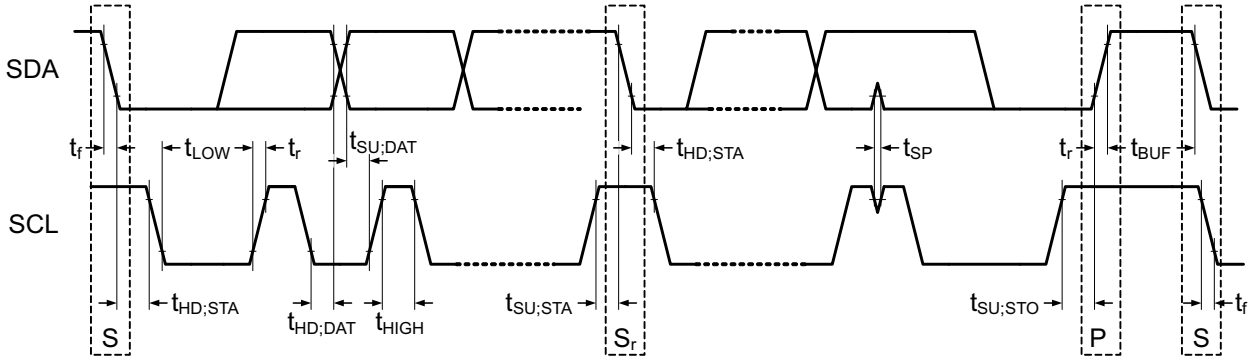


Figure 8. I²C Data Transmission Timing

8.5 Register Maps

Table 2. Register Address Map

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	TMST_VALUE	N/A	Thermistor value read by ADC

8.5.1 Thermistor Readout (TMST_VALUE) Register (offset = 0x00h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TMST_VALUE[7:0]							
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

FIELD NAME	BIT DEFINITION
TMST_VALUE[7:0]	Temperature read-out 1111 0110 – < -10°C 1111 0110 – -10°C 1111 0111 – -9°C ... 1111 1110 – -2°C 1111 1111 – -1 °C 0000 0000 – 0 °C 0000 0001 – 1°C 0000 0010 – 2°C ... 0001 1001 – 25°C ... 0101 0101 – 85°C 0101 0101 – > 85°C

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65185 device is used to power display screens in E-book applications, specifically E-Ink Vizplex display, by connecting the screen to the positive and negative charge pump, LDOs 1 and 2, and VCOM rails. The display screens size that can be supported up to 9.7 inches.

9.2 Typical Application

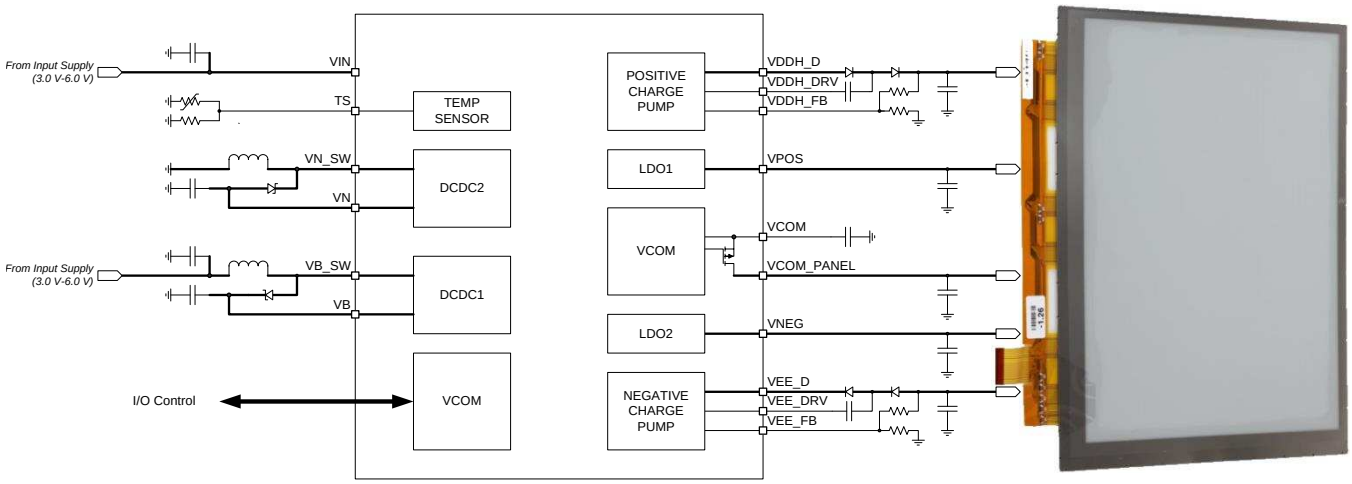


Figure 9. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

	VOLTAGE	SEQUENCE (STROBE)
VNEG (LDO2)	–15 V	1
VEE (Charge pump 2)	–20 V	2
VPOS (LDO1)	15 V	3
VDDH (Charge pump 1)	22 V	4

9.2.2 Detailed Design Procedure

For the positive boost regulator (DCDC1) a 10-µF capacitor can be used as the input capacitor value; two 4.7-µF capacitor are used as output capacitors to reduce ESR along with a 2.2-µH inductor. For the inverting buck-boost regulator (DCDC2), an 10-µF capacitor can be used at the input capacitor value; A 10-µF and 4.7-µF capacitor are used as output capacitors to reduce ESR, with a 4.7-µH inductor. Capacitor ESR for all capacitors should be around 20 mΩ, and ceramic X5R material. These are the typical the values used, additional inductor and capacitor values can be used for improved functionality, but the parts should be rated the same as the recommended external components listed in Table 4.

Table 4. Recommended External Components

PART NUMBER	VALUE	SIZE	MANUFACTURER
INDUCTORS			
LQH44PN4R7MP0	4.7 µH	4 mm × 4 mm × 1.65 mm	Murata
NR4018T4R7M	4.7 µH	4 mm × 4 mm × 1.8 mm	Taiyo Yuden
VLS252015ET-2R2M	2.2 µH	2 mm × 2.5 mm × 1.5 mm	TDK
NR4012T2R2M	2.2 µH	4 mm × 4 mm × 1.2 mm	Taiyo Yuden
CAPACITORS			
GRM21BC81E475KA12L	4.7 µF, 25 V, X6S	805	Murata
GRM32ER71H475KA88L	4.7 µF, 50 V, X7R	1210	Murata
All other capacitors	X5R or better	—	—
DIODES			
BAS3010	—	SOD-323	Infineon
MBR130T1	—	SOD-123	ON-Semi
BAV99	—	SOT-23	Fairchild
THERMISTOR			
NCP18XH103F03RB	10 kΩ	603	Murata

9.2.3 Application Curves

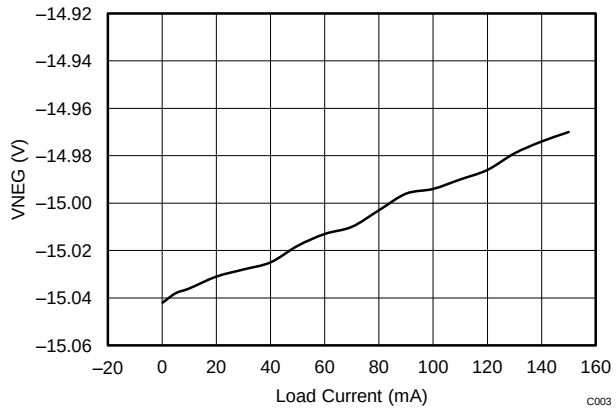


Figure 10. Load Current vs VNEG

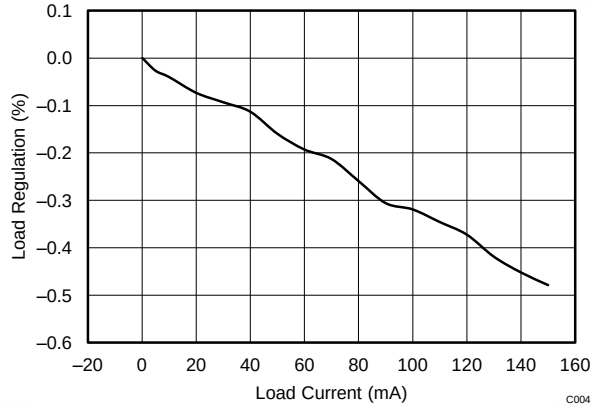


Figure 11. Load Current vs Load Regulation

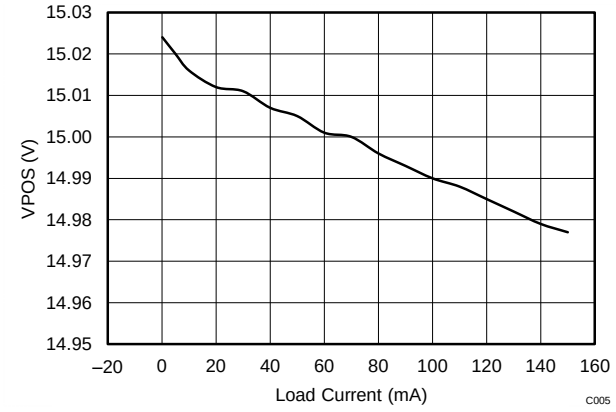


Figure 12. Load Current vs VPOS

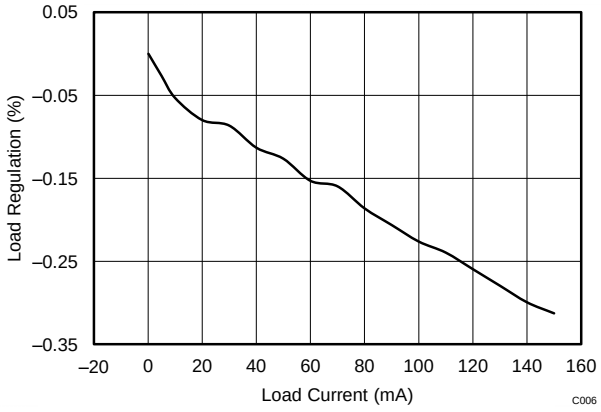


Figure 13. Load Current vs Load Regulation

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 3 V to 6 V. This input supply can be from a externally regulated supply. If the input supply is located more than a few inches from the TPS65185, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The layout guidelines for TPS65182x are as follows:

- PBKG (Die substrate must connect to VN (–16 V) with short, wide trace. Wide copper trace will improve heat dissipation.
- Power pad is internally connected to PBKG and must be connected to ground, but connected to VN with a short wide copper trace.
- Inductor traces must be kept on the PCB top layer free of any vias.
- Feedback traces must be routed away from any potential noise source to avoid coupling.
- Output caps must be placed immediately at output pin.
- VIN pins must be bypassed to ground with low ESR ceramic bypass capacitors.

11.2 Layout Example

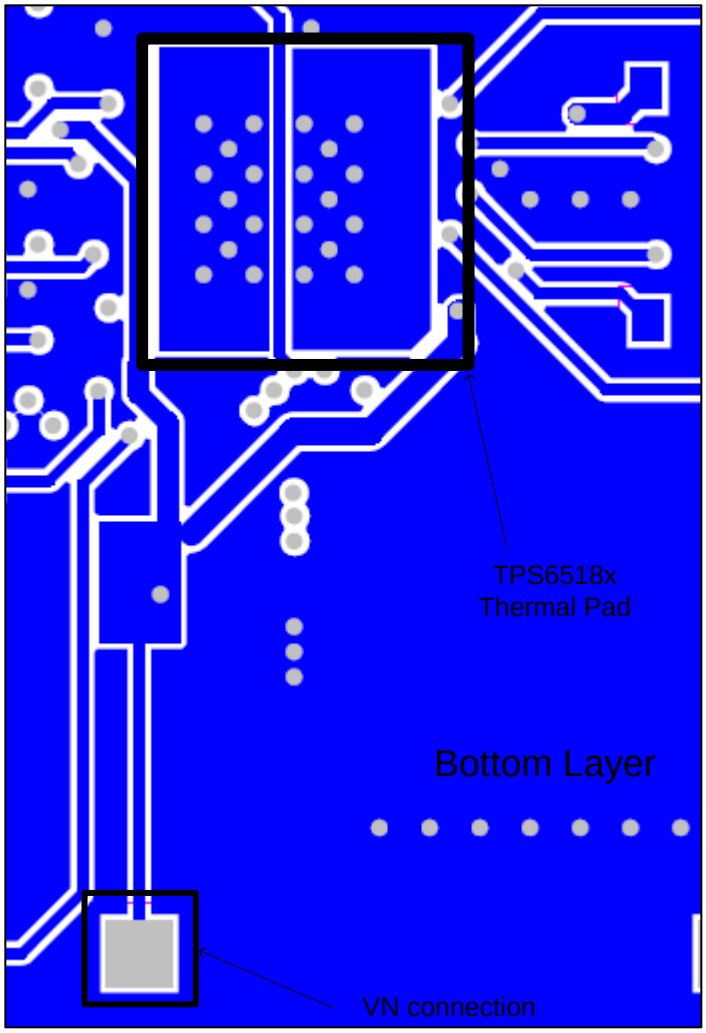


Figure 14. Typical Layout of TPS6518x

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65182	Click here	Click here	Click here	Click here	Click here
TPS65182B	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

OMAP, E2E are trademarks of Texas Instruments.
Vizplex is a trademark of E Ink Corporation.
E Ink is a registered trademark of E Ink Corporation.
EPSON is a registered trademark of Seiko Epson Corporation.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65182BRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	E INK TPS65182B	Samples
TPS65182BRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	E INK TPS65182B	Samples
TPS65182RGZR	NRND	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	E INK TPS65182	
TPS65182RGZT	NRND	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	E INK TPS65182	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

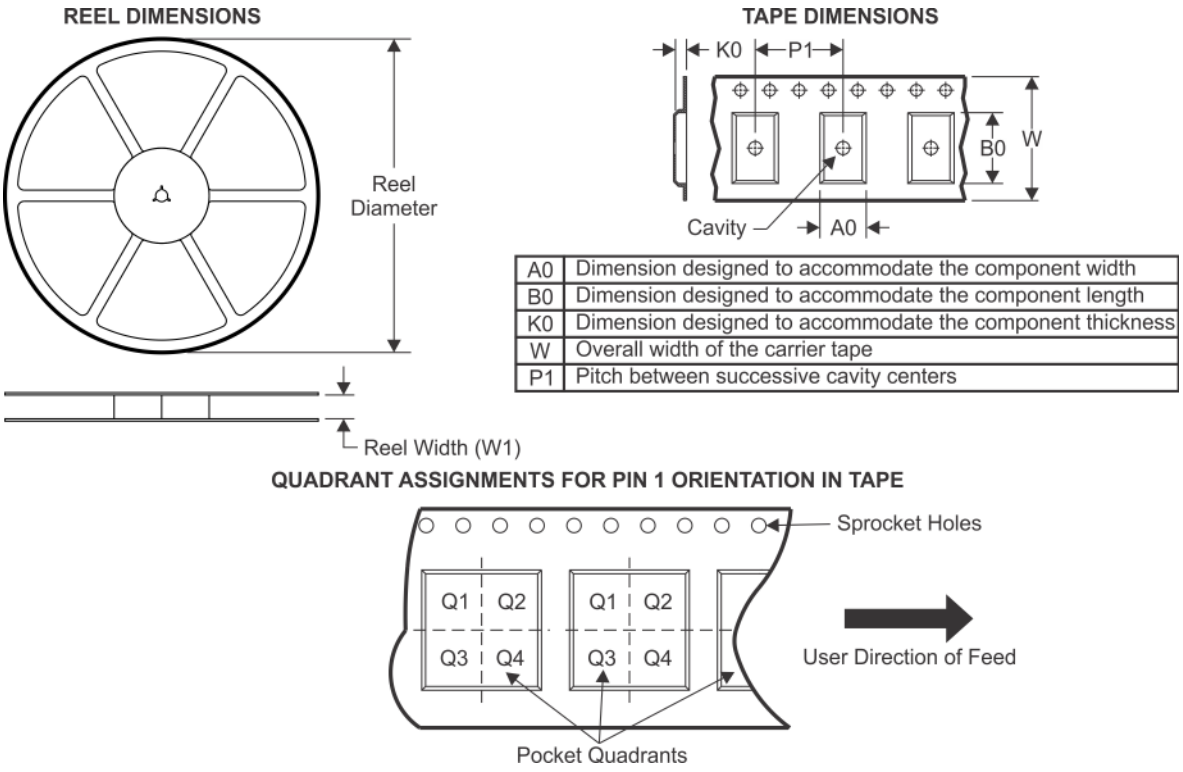
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

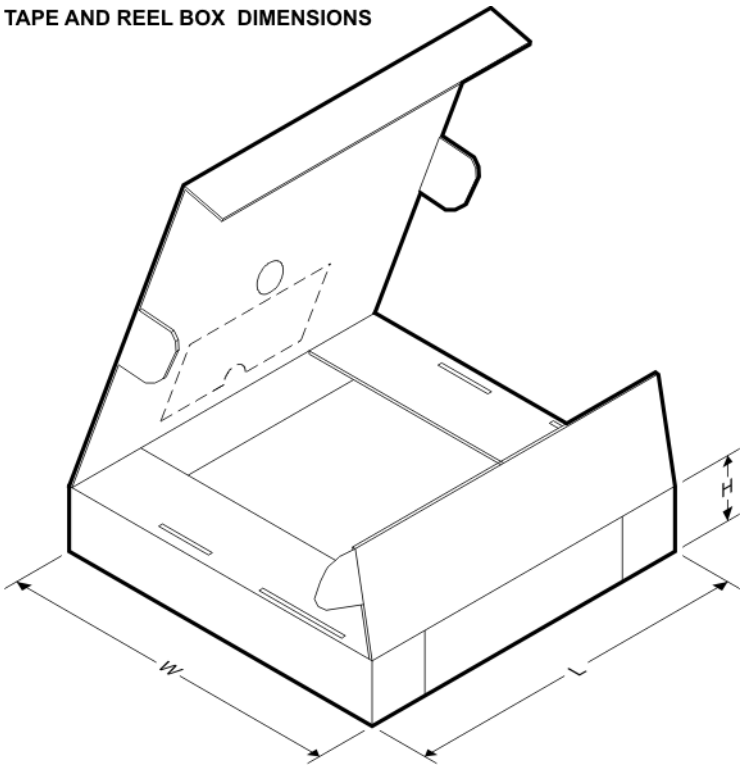


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65182BRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TPS65182BRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TPS65182RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TPS65182RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65182BRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65182BRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
TPS65182RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65182RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

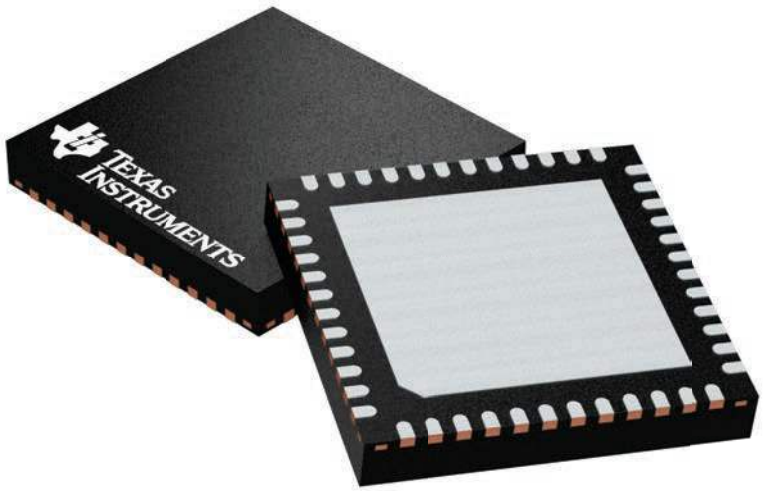
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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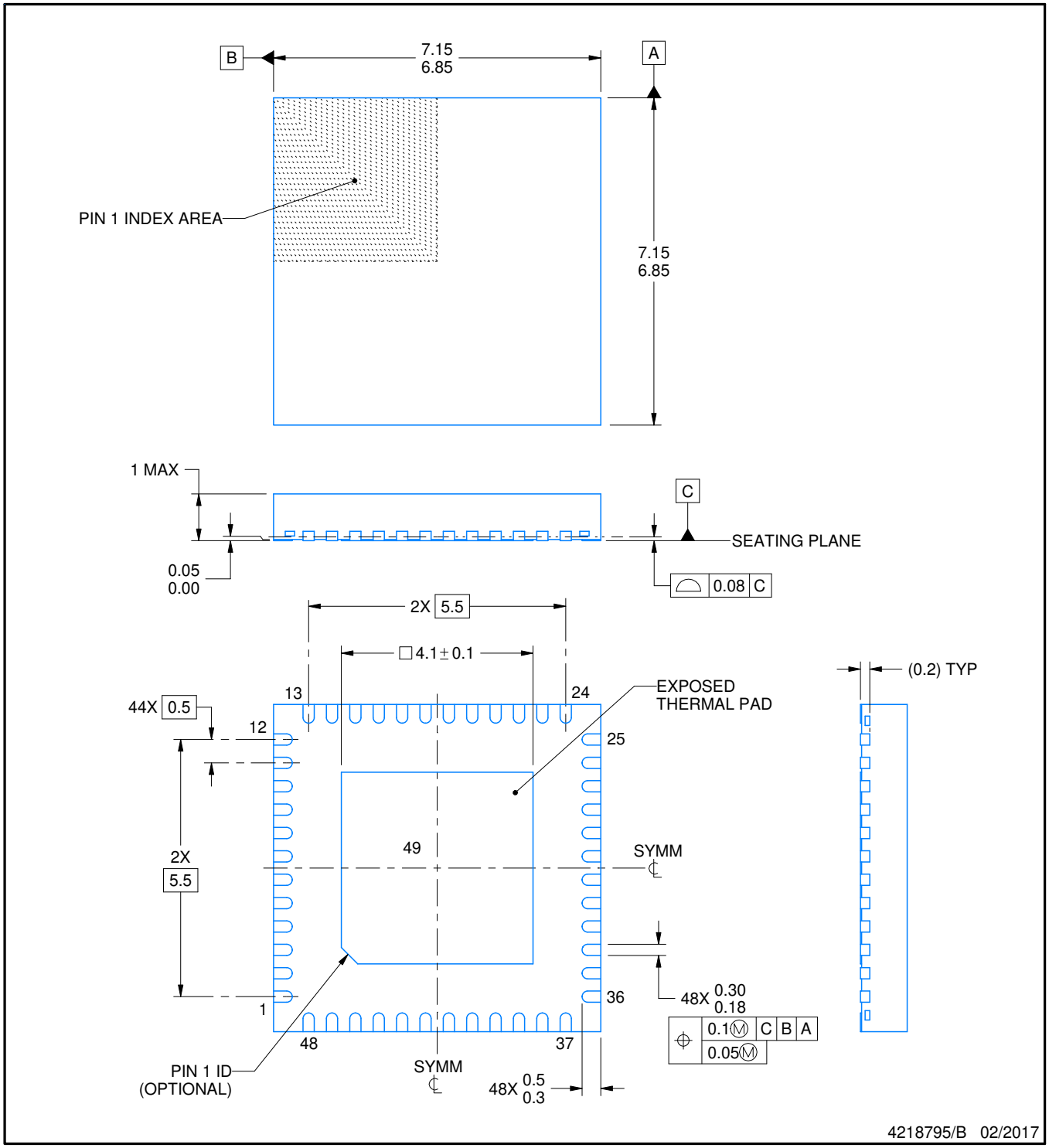
RGZ0048B

PACKAGE OUTLINE

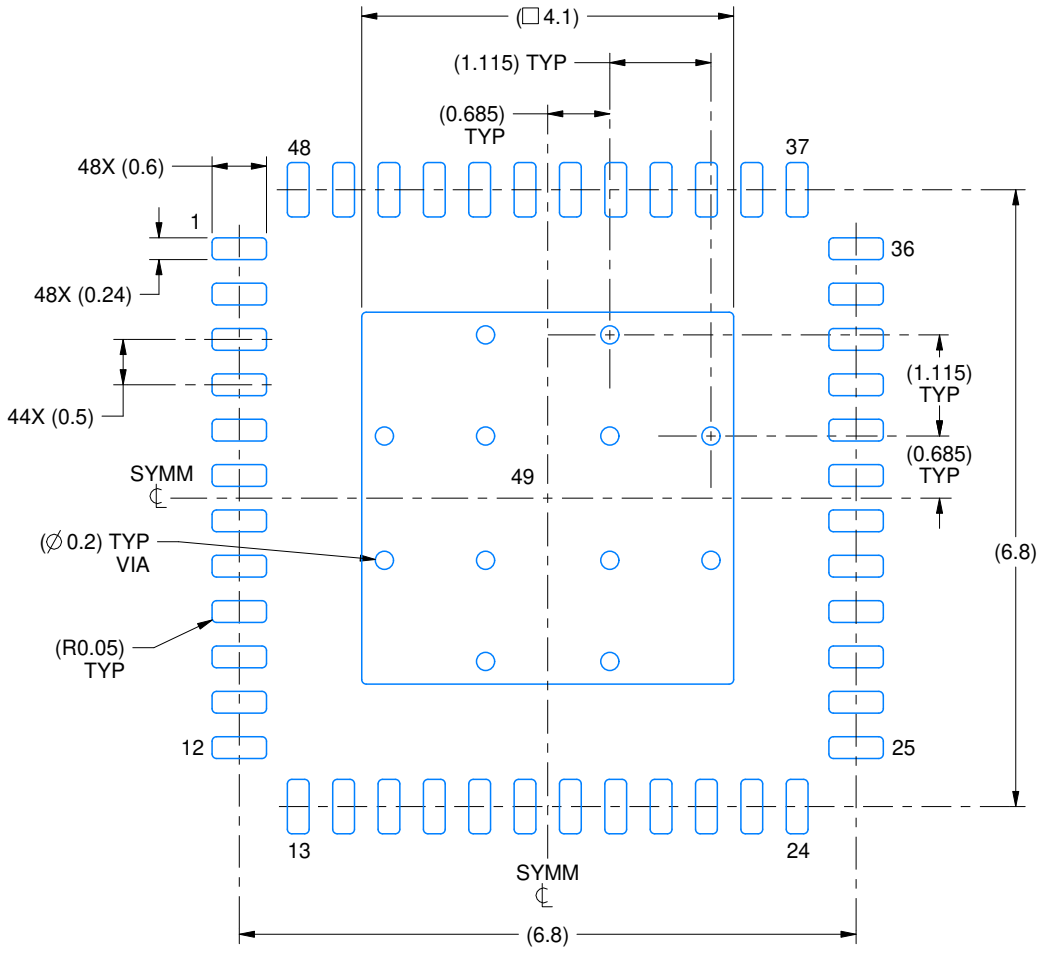
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

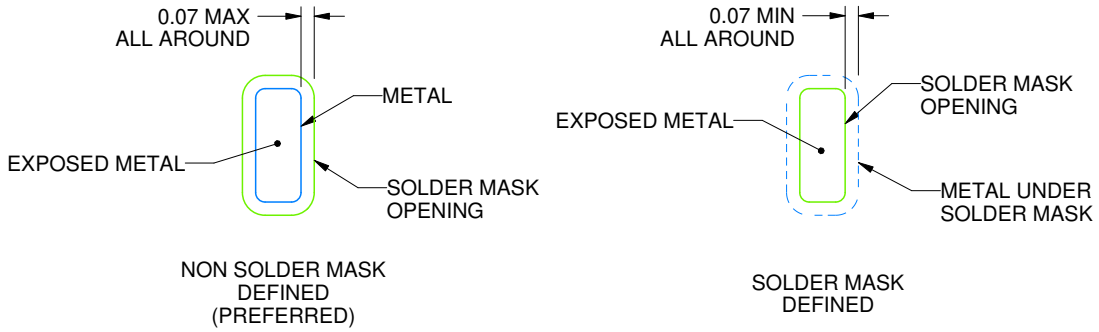


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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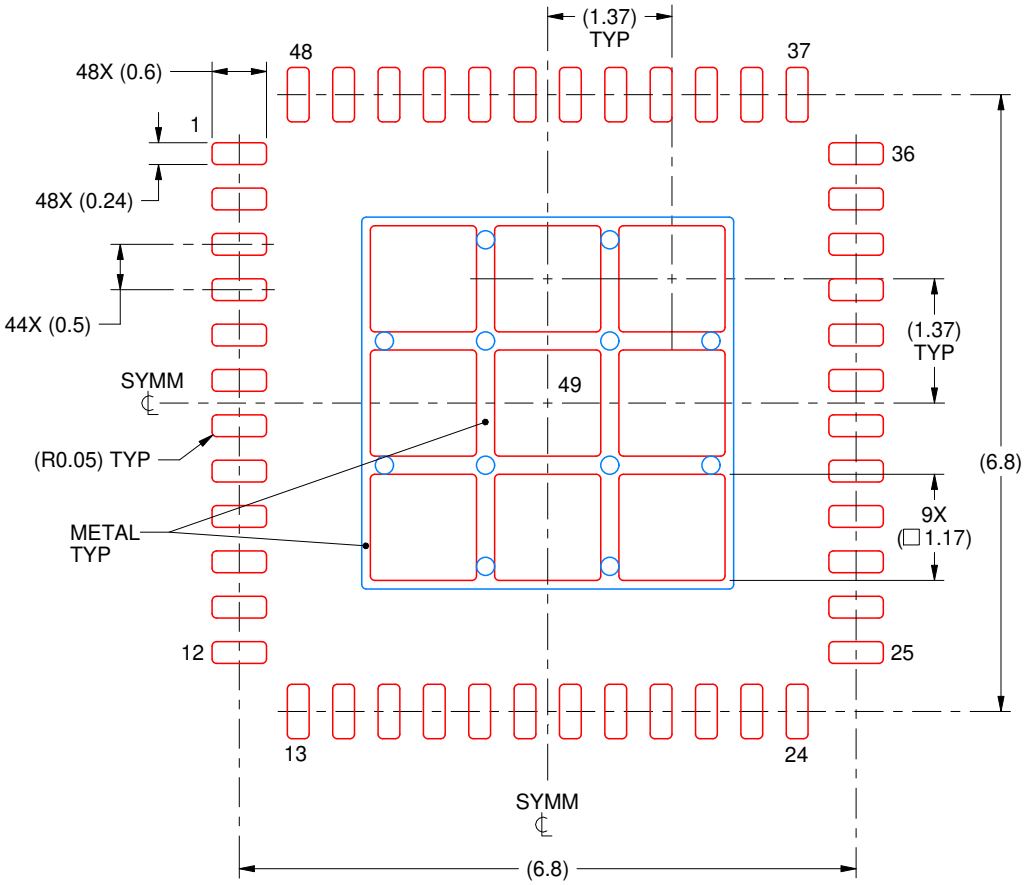
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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