NVLJD4007NZ

MOSFET – Dual, N-Channel, Small Signal, Gate ESD Protection, 2x2 WDFN

30 V, 245 mA

ON Semiconductor®

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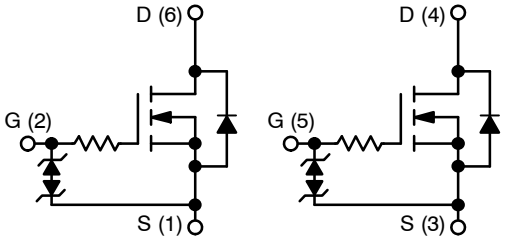
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ @ V_{GS}	I_D MAX (Note 1)
30 V	1.4 Ω @ 4.5 V	245 mA
	2.3 Ω @ 2.5 V	

Features

- Optimized Layout for Excellent High Speed Signal Integrity
- Low Gate Charge for Fast Switching
- Small 2 x 2 mm Footprint
- ESD Protected Gate
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

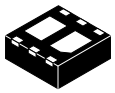
Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	30	V
Gate−to−Source Voltage		V_{GS}	±10	V
Continuous Drain Current (Note 1)	Steady State = 25°C	I_D	245	mA
Power Dissipation (Note 1)	Steady State = 25°C	P_D	755	mW
Pulsed Drain Current	$t_P \leq 10$ μs	I_{DM}	1.2	A
Operating Junction and Storage Temperature		T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)		I_{SD}	245	mA
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	166	°C/W

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



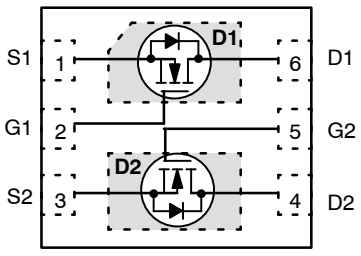
WDFN6
CASE 506AN

MARKING DIAGRAM

JG = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NVLJD4007NZTAG	WDFN6 (Pb−Free)	3000/Tape & Reel
NVLJD4007NZTBG	WDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 μA	30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to 25°C, I_D = 100 μA		27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V			1.0	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V, T = 85 °C			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V			±25	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V			±1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V T = 85 °C			±1.0	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 100 μA	0.5	1.0	1.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C, I_D = 100 μA		−2.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 125 mA		1.4	7.0	Ω
		V_{GS} = 2.5 V, I_D = 125 mA		2.3	7.5	
Forward Transconductance	g_{FS}	V_{DS} = 3 V, I_D = 125 mA		80		mS
CAPACITANCES & GATE CHARGE						
Input Capacitance	C_{ISS}	V_{DS} = 5.0 V, f = 1 MHz, V_{GS} = 0 V		12.2	20	pF
Output Capacitance	C_{OSS}			10	15	
Reverse Transfer Capacitance	C_{RSS}			3.3	6.0	
Total Gate Charge	Q_g	V_{DS} = 24 V, I_D = 100 mA, V_{GS} = 4.5 V		0.75		nC
Gate−to−Source Charge	Q_{gs}			0.20		
Gate−to−Drain Charge	Q_{gd}			0.20		
Plateau Voltage	V_{GP}			1.57		V
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 125 mA, R_G = 10 Ω		9		ns
Rise Time	t_r			41		ns
Turn−Off Delay Time	$t_{d(OFF)}$			96		
Fall Time	t_f			72		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 125 mA		0.79	0.9	V

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

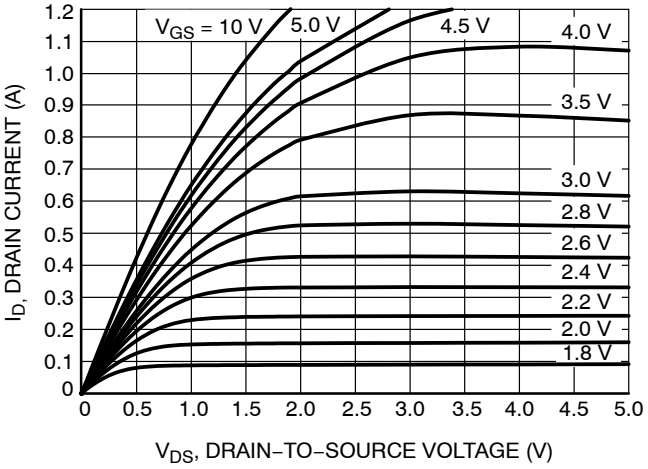


Figure 1. On−Region Characteristics

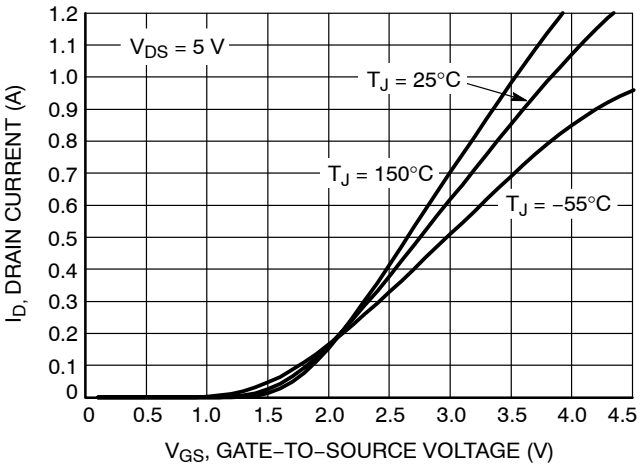


Figure 2. Transfer Characteristics

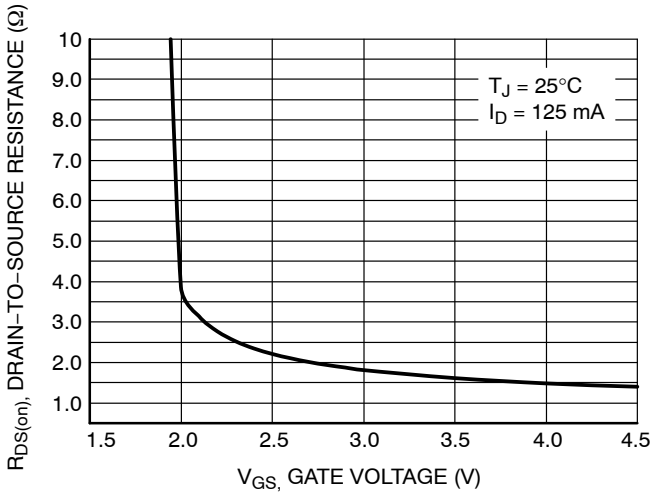


Figure 3. On−Resistance vs. Gate−to−Source Voltage

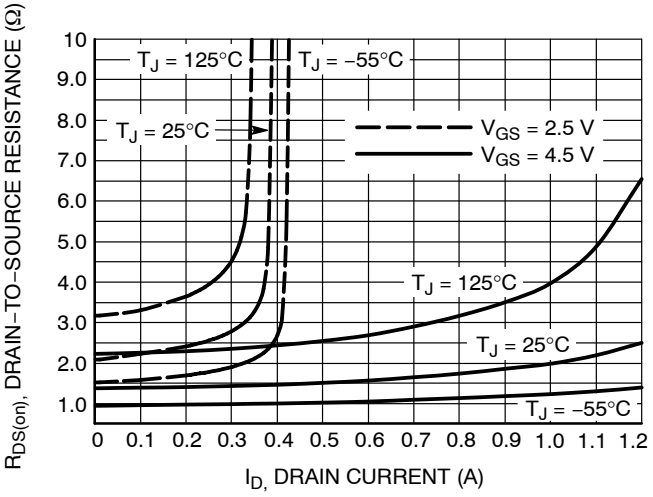


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

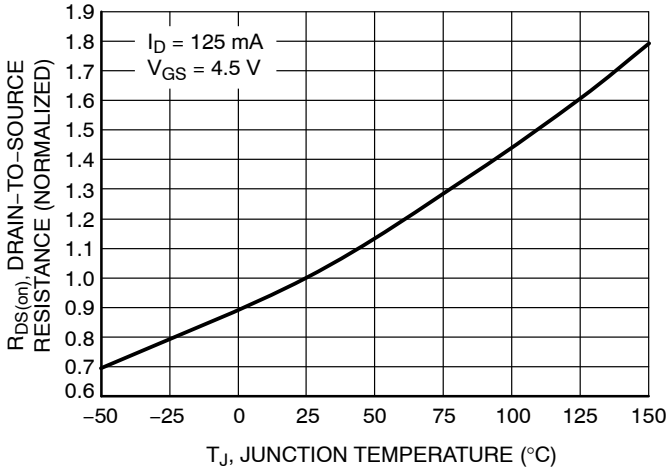


Figure 5. On−Resistance Variation with Temperature

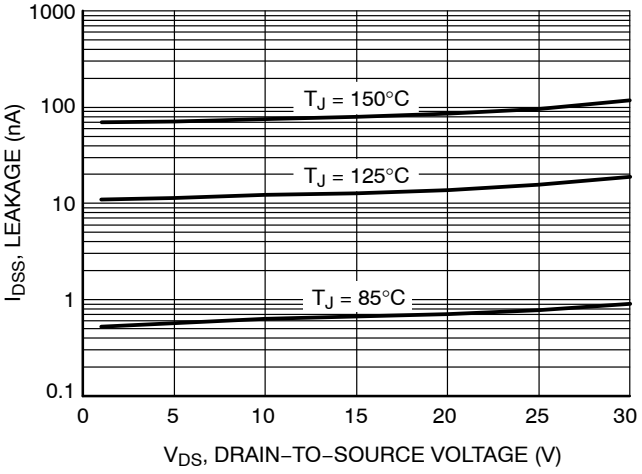


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

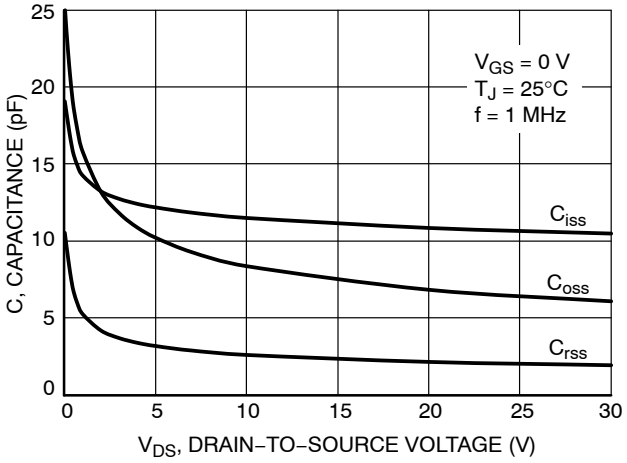


Figure 7. Capacitance Variation

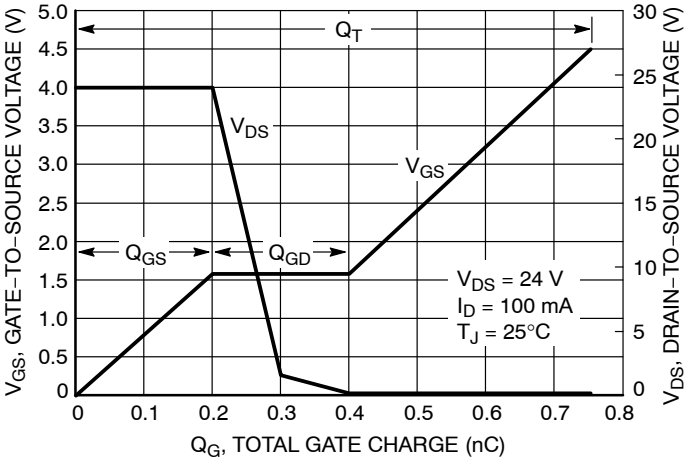


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

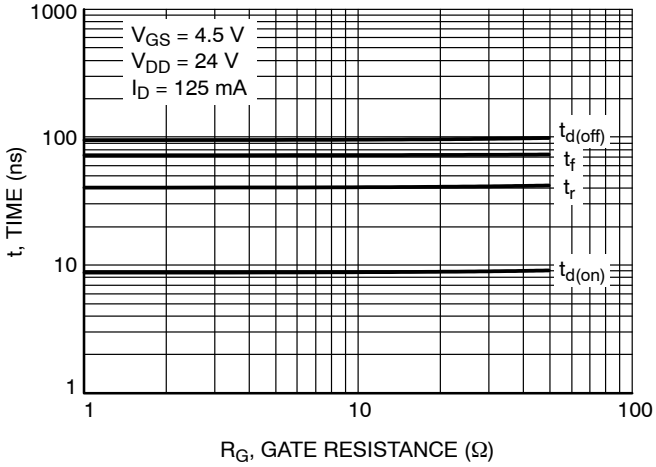


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

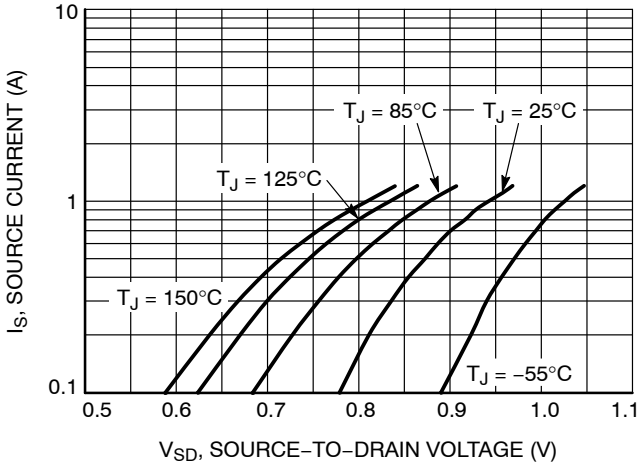


Figure 10. Diode Forward Voltage vs. Current

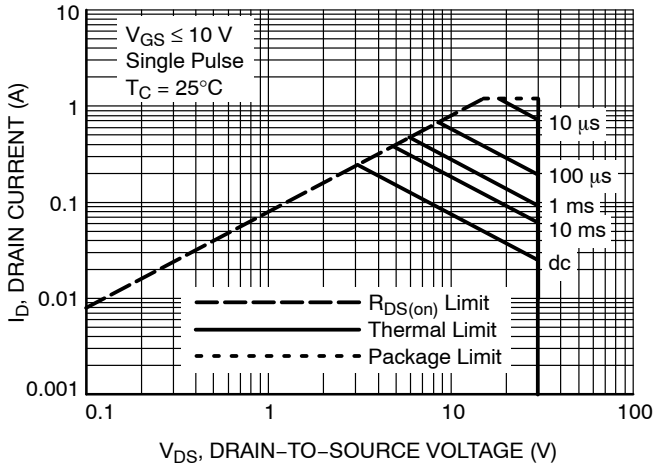


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

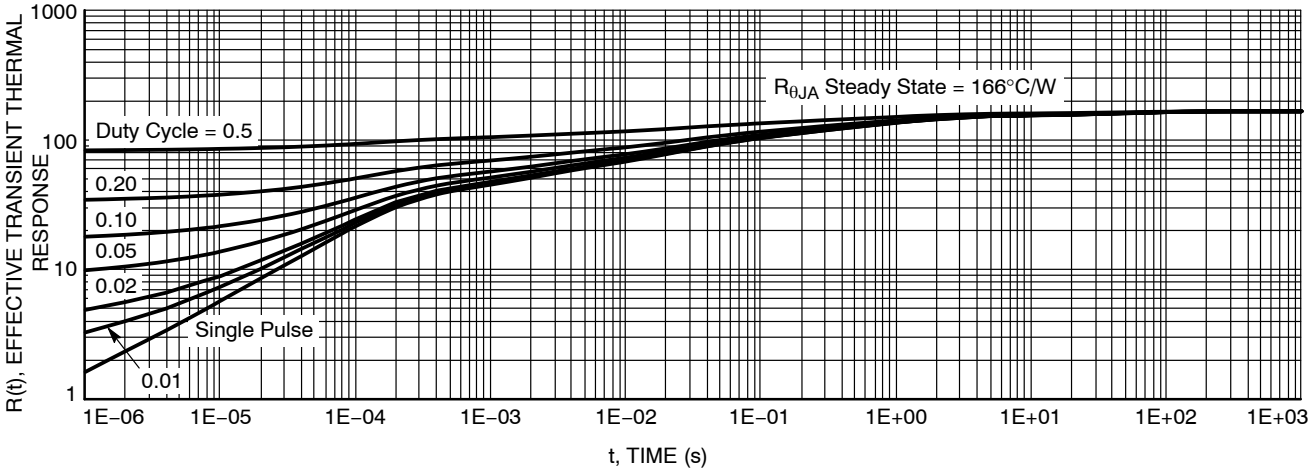
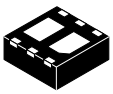


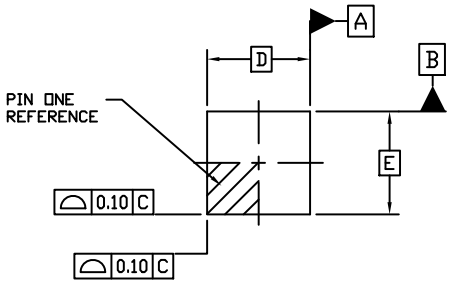
Figure 12. Thermal Impedance (Junction−to−Ambient)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022

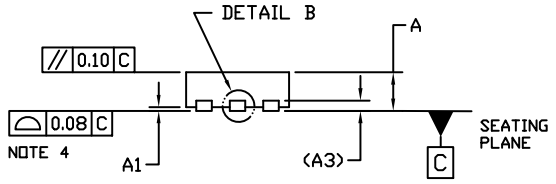


TOP VIEW

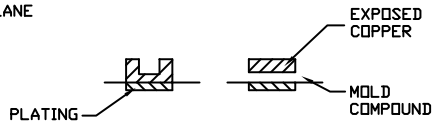
DETAIL A
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

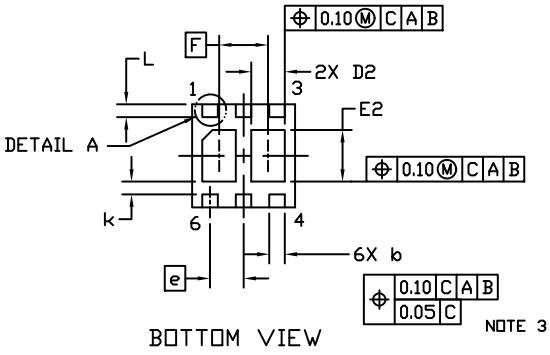


SIDE VIEW

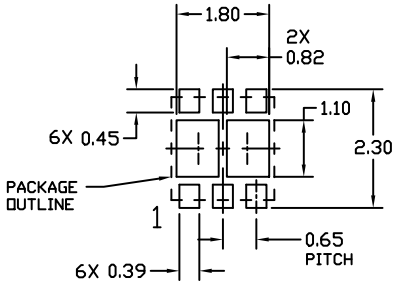


DETAIL B
OPTIONAL CONSTRUCTIONS

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT
SOLDERMASK DEFINED

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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