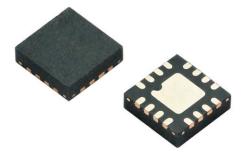
SiP12109



4 A, 4.5 V to 15 V Input Synchronous Buck Regulator



DESCRIPTION

The SiP12109 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 4 A continuous current at 1.5 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 4.5 V to 15 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiP12109's CM-COT architecture delivers ultra-fast transient response with minimum output capacitance and tight ripple regulation at very light load. The part is stable with any capacitor type and no ESR network is required for loop stability. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output overvoltage protection (OVP), output under voltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and internal soft-start ramp.

The SiP12109 is available in lead (Pb)-free power enhanced 3 mm x 3 mm QFN16-33G package.

FEATURES

- 4.5 V to 15 V input voltage
- Adjustable output voltage down to 0.6 V
- 4 A continuous output current
- Selectable switching frequency from 400 kHz to 1.5 MHz with an external resistor
- 95 % peak efficiency
- · Stable with any capacitor. No external ESR network required
- Ultrafast transient response
- Power saving scheme for increased light load efficiency
- ± 1 % accuracy of V_{OUT} setting
- Cycle-by-cycle current limit
- Fully protected with OTP, SCP, UVP, OVP
- P_{GOOD} indicator
- -40 °C to +125 °C operating junction temperature
- Output voltage tracking
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Low voltage, distributed power architectures with 5 V or 12 V rails
- · Computing, broadband, networking, LAN/WAN, optical, test and measurement
- A/V, high density cards, storage, DSL, STB, DVR, DTV, Industrial PC

TYPICAL APPLICATION CIRCUIT

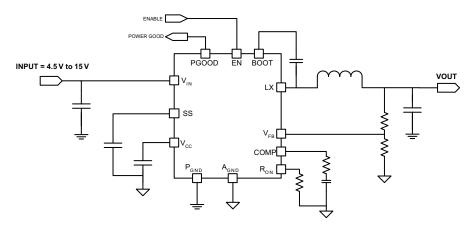


Fig. 1 - Typical Application Circuit for SiP12109

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1 For technical questions, contact: powerictechsupport@vishay.com Document Number: 62694



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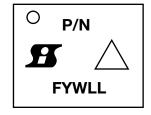
ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING (LINE 2: P/N)
SiP12109DMP-T1-GE4	QFN16 3 x 3	2109
SiP12109DB	N/A	-

Note

• "DB" means demo board

MARKING



Format: Line 1: dot Line 2: P/N Line 3: Siliconix logo and ESD symbol Line 4: factory code and year code and work week code and LOT code

ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT	
V _{IN}	Reference to P _{GND}	-0.3 to 16		
V _{CC}	Reference to A _{GND}	-0.3 to 6		
LX	Reference to P _{GND}	-0.3 to 16		
LX (AC)	100 ns	17	V	
Boot		-0.3 to $V_{IN} + V_{CC}$		
A _{GND} to P _{GND}		-0.3 to 0.3		
All logic inputs	Reference to A _{GND}	-0.3 to V _{CC} + 0.3		
TEMPERATURE			-	
Max. operating junction temperature		-40 to +150	°C	
Storage temperature		-65 to +150	U	
POWER DISSIPATION				
Junction to ambient thermal impedance (R_{thJA})		36.3	°C/W	
Meximum neuror discinction	Ambient temperature = 25 °C	3.4		
Maximum power dissipation	Ambient temperature = 100 °C	1.3	— W	
ESD PROTECTION	· · ·		·	
Electrostatic discharge protection	HBM	2	kV	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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RECOMMENDED OPERATING RA	ANGE (all voltages ref	erenced to GND	= 0 V)	
ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
V _{IN}	4.5	-	15	
Vcc	4.5	-	5.5	V
LX	-1	-	15	v
V _{OUT}	0.6	-	5.5	
TEMPERATURE				
Recommended ambient temperature		-40 to +85		°C
Operating junction temperature		-40 to +125		C

ELECTRICAL SPECIFICATIONS (test condition unless otherwise specified)							
	0/4/201	TEST CONDITION LIMITS					
PARAMETER	SYMBOL	V_{IN} = 12 V, T_A = -40 °C to +85 °C	MIN.	TYP.	MAX.	UNIT	
POWER SUPPLY							
Power input voltage range	V _{IN}	Note 1	4.5	-	15	v	
V _{CC} regulator voltage	V _{CC}		4.5	5	5.5	v	
Input current	IV _{IN_NOLOAD}	$T_A = 25 \text{ °C}, R_{on} = 75 \text{ k}\Omega,$ Non-switching, $I_O = 0 \text{ A}$	-	1.2	-	mA	
Shutdown current	IV _{IN_SHDN}	EN = 0 V	-	5	8	μA	
V _{CC} UVLO threshold	V _{CC_UVLO}	V _{CC} rising	2.3	2.55	2.8	V	
V _{CC} UVLO hysteresis	V _{CC_UVLO_HYS}		-	300	-	mV	
CONTROLLER AND TIMING							
Feedback reference	V	T _A = 25 °C	0.596	0.600	0.604	v	
Feedback reference	V _{FB}	$T_A = -40 \ ^\circ C \ to \ +85 \ ^\circ C$	0.594	0.600	0.606	v	
V _{FB} input bias current	I _{FB}		-	2	200	nA	
Transconductance	9 _m		-	1	-	mS	
COMP source current	ICOMP_SOURCE		-	50	-		
COMP sink current	I _{COMP_SINK}		-	50	-	μA	
On-time	t _{ON}	R _{on} = 75 kΩ	100	135	170	ns	
Minimum off-time	t _{OFF_MIN} .		145	200	255	ns	
Soft start current	I _{SS}		3	5	7	μA	
POWER MOSFETS							
High-side on resistance	R _{ON_HS}		-	45	67		
Low-side on resistance	R _{ON_LS}	$V_{GS} = 5 V$	-	27	41	mΩ	
FAULT PROTECTIONS							
Over current limit	I _{OCP}	Inductor valley current	4	5	6	Α	
Output OVP threshold	V _{FB_OVP}	W with respect to 0.6 W reference	-	21	-	%	
Output UVP threshold	V _{FB_UVP}	V_{FB} with respect to 0.6 V reference	-	-65	-	70	
Over temperature protection		Rising temperature	-	160	-	°C	
Over temperature protection		Hysteresis	-	35	-	C	
POWER GOOD							
Power good output threshold	V _{FB_RISING_VTH_OV}	V _{FB} rising above 0.6 V reference	-	21	-	%	
Fower good output threshold	V _{FB_FALLING_VTH_UV}	V _{FB} falling below 0.6 V reference	-	-12.5	-	70	
Power good on resistance	R _{ON_PGOOD}		-	30	60	Ω	
Power good delay time	t _{DLY_PGOOD}		-	5	-	μs	
ENABLE THRESHOLD							
Logic high level	V _{EN_H}		1.5	-	-	v	
Logic low level	V _{EN_L}		-	-	0.4	v	

Note

 $^{(1)}~$ Tie V_{CC} to V_{IN} when V_{IN} is <5.5~V



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FUNCTIONAL BLOCK DIAGRAM

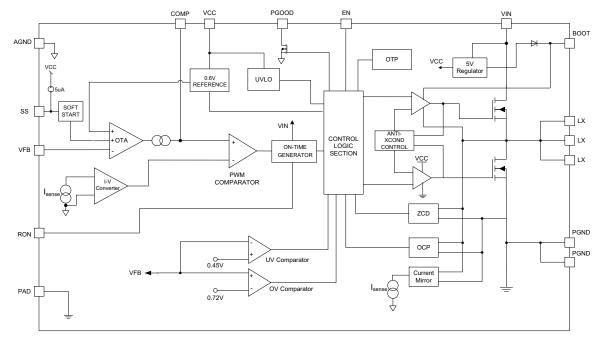
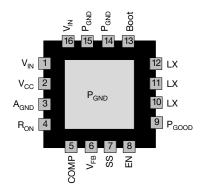


Fig. 2 - SiP12109 Functional Block Diagram

PIN CONFIGURATION





PIN CONFIG	URATION	
PIN NUMBER	NAME	FUNCTION
1, 16	V _{IN}	Input supply voltage for power MOS. $V_{IN} = 4.5$ V to 15 V
2	V _{CC}	Internal regulator output, tie V_{CC} to V_{IN} when V_{IN} is < 5.5 V
3	A _{GND}	Analog ground
4	R _{ON}	An external resistor between R _{ON} and A _{GND} sets the switching on time
5	COMP	Connect to an external RC network for loop compensation and droop function
6	V _{FB}	Feedback voltage. 0.6 V (typ.). Use a resistor divider between V _{OUT} and A _{GND} to set the output voltage
7	SS	An external capacitor between SS and A _{GND} sets the soft start time
8	EN	Enable pin. Pull enable above 1.5 V to enable and below 0.4 V to disable the part. Do not float this pin
9	P _{GOOD}	Power good output. Open drain
10, 11, 12	LX	Switching node, inductor connection point
13	BOOT	Bootstrap pin - connect a capacitor of at least 100 nF from BOOT to LX to develop the floating supply for the high-side gate drive

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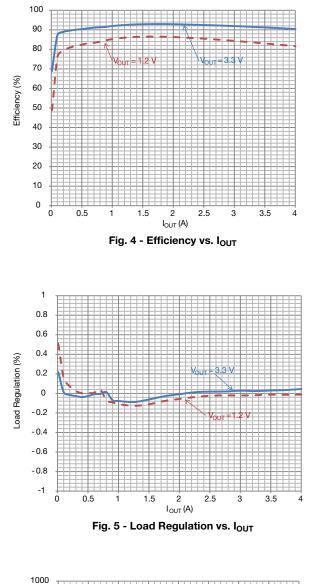
PIN CONFIGURATION PIN NUMBER NAME 14, 15, PAD P_{GND}

	FUNCTION	
Power ground		



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ELECTRICAL CHARACTERISTICS (VIN = 12 V, VOUT = 1.2 V, Fsw = 1 MHz, L0 = 1 µH, C0 = 3 x 22 µF, unless noted otherwise)



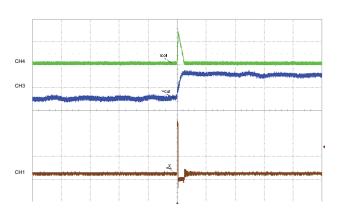


Fig. 7 - Steady-State, $I_{OUT} = 0 A$, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (20 mV/div), CH4 (GRN) = I_{COIL} (1 A/div), Time = 5 µs/div

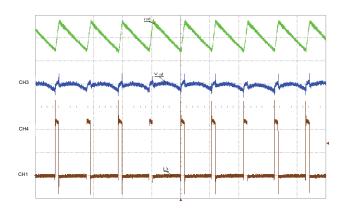


Fig. 8 - Steady-State, I_{OUT} = 4 A, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (20 mV/div), CH4 (GRN) = I_{COIL} (1 A/div), Time = 1 µs/div

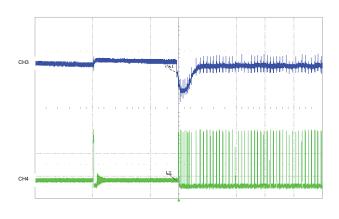


Fig. 9 - Load Step Undershoot Response, I_{OUT} = 0 A to 4 A, CH3 (BLU) = V_{OUT} (100 mV/div), CH4 (GRN) = LX (5 V/div), Time = 10 µs/div

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0.5

1.5

2 I_{OUT} (A) Fig. 6 - Frequency Variation vs. IOUT

2.5

3

3.5

900 800

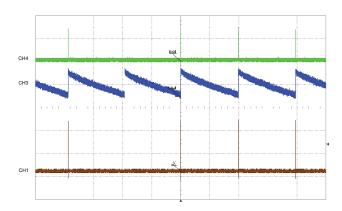
700

Switching Frequecy (kHz)

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Fig. 10 - Steady-State, $I_{OUT} = 0 A$, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (20 mV/div), CH4 (GRN) = I_{COIL} (1 A/div), Time = 5 ms/div

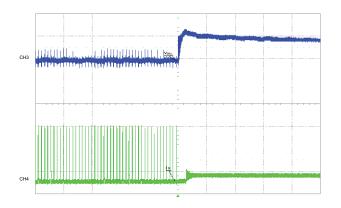


Fig. 11 - Load Step Overshoot Response, I_{OUT} = 4 A to 0 A , CH3 (BLU) = V_{OUT} (100 mV/div), CH4 (GRN) = LX (5 V/div), Time = 10 µs/div

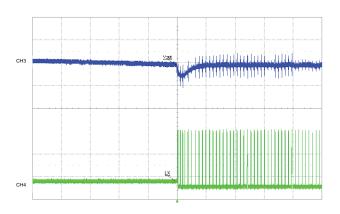


Fig. 12 - Load Step Undershoot Response, $I_{OUT} = 0$ A to 2 A, CH3 (BLU) = V_{OUT} (100 mV/div), CH4 (GRN) = LX (5 V/div), Time = 10 µs/div

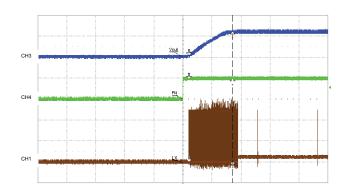


Fig. 13 - Start-Up, I_{OUT} = 0 A, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (1 V/div), CH4 (GRN) = EN (5 V/div), Time = 1 ms/div

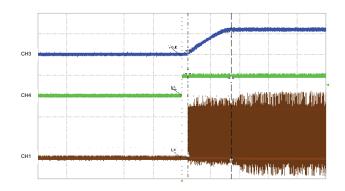


Fig. 14 - Start-Up, I_{OUT} = 4 A, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (1 V/div), CH4 (GRN) = EN (5 V/div), Time = 1 ms/div

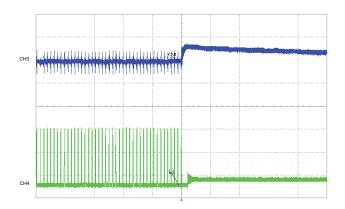
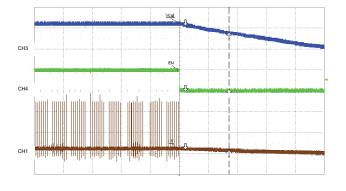


Fig. 15 - Load Step Overshoot Response, $I_{OUT} = 2 \text{ A to 0 A}$, CH3 (BLU) = V_{OUT} (100 mV/div), CH4 (GRN) = LX (5 V/div), Time = 10 µs/div

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Fig. 16 - Shut-Down, I_{OUT} = 0 A, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (1 V/div), CH4 (GRN) = EN (5 V/div), Time = 1 ms/div

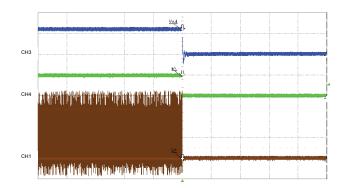


Fig. 17 - Shut-Down, I_{OUT} = 4 A, CH1 (BRN) = LX (5 V/div), CH3 (BLU) = V_{OUT} (1 V/div), CH4 (GRN) = EN (5 V/div), Time = 1 ms/div

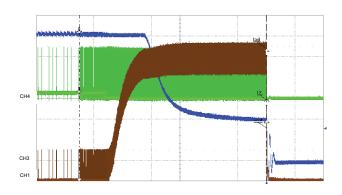
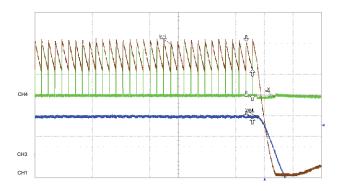
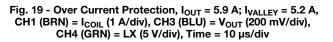
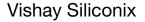


Fig. 18 - Over Current Protection, $I_{OUT} = 5.9 \text{ A}$; $I_{VALLEY} = 5.2 \text{ A}$, CH1 (BRN) = I_{COIL} (1 A/div), CH3 (BLU) = V_{OUT} (200 mV/div), CH4 (GRN) = LX (5 V/div), Time = 500 µs/div





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OPERATIONAL DESCRIPTION

Device Overview

SiP12109 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 4 A continuous current. The device has programmable switching frequency up to 1.5 MHz. The control scheme is based on current-mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency foldback as load decreases.

SiP12109 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output

This device is available in QFN16 3 x 3 package to deliver high power density and minimize PCB area.

Power Stage

SiP12109 integrates a high-performance power stage with a ~ 45 m Ω high side n-channel MOSFET and a ~ 27 m Ω low side n-channel MOSFET. The MOSFETs are optimized to achieve 95 % efficiency at up to 1.5 MHz switching frequency.

The power input voltage (V_{IN}) can go up to 15 V and down as low as 4.5 V for the power conversion. The logic bias voltage (V_{CC}) ranges from 4.5 V to 5.5 V.

PWM Control Mechanism

SiP12109 employs a state-of-the-art current-mode COT control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated on the COMP pin. In the meantime, inductor valley current is sensed, and its slope (I_{sense}) is converted into a voltage signal ($V_{current}$) to be compared with V_{COMP} . Once $V_{current}$ is lower than V_{COMP} , a single shot on-time is generated for a fixed time programmed by the external R_{ON} . Fig. 20 illustrates the basic block diagram for CM-COT architecture and Fig. 21 demonstrates the basic operational principle:

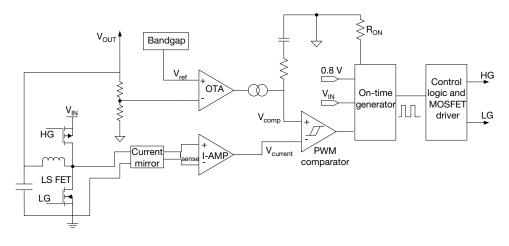


Fig. 20 - CM-COT Block Diagram



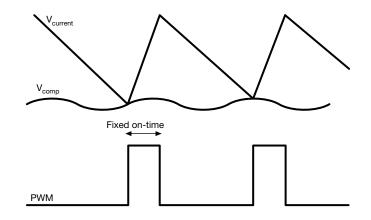


Fig. 21 - CM-COT Operational Principle

The following equation illustrates the relationship between on-time, $V_{\text{IN}},\,V_{\text{OUT}}$ and R_{ON} value:

$$T_{ON} = R_{ON} \times K \times \frac{1}{V_{IN}}$$
, where $K = 17.5 \times 10^{-12}$ is a constant set internally

$$f \operatorname{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{1}{V_{IN}} \times R_{ON} \times K} = \frac{V_{OUT}}{R_{ON} \times K}$$

Loop Stability and Compensator Design

Due to the nature of current mode control, a simple RC network (type II compensator) is required between COMP and A_{GND} for loop stability and transient response purpose. The general concept of this loop design is to introduce a single zero through the compensator to determine the crossover frequency of overall close loop system.

The overall loop can be broken down into following segments.

Output feedback divider transfer function H_{fb}Z:

$$H_{fb} = \frac{R_{fb2}}{R_{fb1} \ x \ R_{fb2}}$$

Voltage compensator transfer function G_{COMP} (s):

$$G_{COMP} (s) = \frac{R_{O} x (1 + sC_{COMP}R_{COMP})}{(1 + sR_{O}C_{COMP})} gm$$

Modulator transfer function H_{mod} (s):

$$H_{mod} (s) = \frac{1}{AV_1 x R_{DS(on)}} x \frac{R_{load} x (1 + sC_0 R_{ESR})}{(1 + sC_0 R_{load})}$$

The complete loop transfer function is given by:

$$H_{mod}(s) = \frac{R_{fb2}}{R_{fb1} x R_{fb2}} x \frac{R_{O} x (1 + sC_{COMP}R_{COMP})}{(1 + sR_{O}C_{COMP})} gm x \frac{1}{AV_{1} x R_{DS(on)}} x \frac{R_{load} x (1 + sC_{O}R_{ESR})}{(1 + sC_{O}R_{load})}$$

When:

C _{COMP} = compensation capacitor	R _{fb1}	= feedback resistor connect to LX
R _{COMP} = compensation resistor	R_{fb2}	= feedback resistor connect to ground
gm = error amplifier transconductance	R _O	= output impedance of error amplifier = 20 $M\Omega$
R _{load} = load resistance	AV_1	= voltage to current gain = 3
C _O = output capacitor		
R _{DS(on)} = LS switch resistance		

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Light Load Operation

To further improve efficiency at light-load condition, SiP12109 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal zero crossing detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In light load operation as soon as inductor valley current crosses zero, the device first deploys diode

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiP12109 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined time, the valley current is compared with internal threshold (5 A typ.) to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses while keeping output ripple within tolerance. The switching frequency is set by the controller to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output under-voltage protection (UVP), which latches the device off to prevent catastrophic thermal-related failure. UVP is described in the next section. OCP is enabled immediately after V_{CC} passes UVLO level.

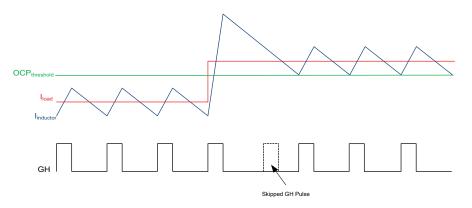


Fig. 22 - Over-Current Protection Illustration

Output Under-Voltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. Once the voltage level at V_{FB} is below 0.2 V for more than 20 µs, then UVP event is recognized and both HS and LS MOSFETs are turned off. UVP latches the device off until either V_{CC} or EN is recycled.

UVP is only active after the completion of soft-start sequence.

Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through V_{FB} pin. After soft-start, if the voltage level at V_{FB} is above 21 % (typ.), OVP is triggered with HS FET turning off and LS FET turning on immediately to discharge the output. Normal operation is resumed once V_{FB} drops back to 0.675 V.

OVP is active immediately after V_{CC} passes UVLO level.

Over-Temperature Protection (OTP)

SS

SiP12109 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 160 °C (typ.). A hysteresis of 30 °C is implemented, so when junction temperature drops below 130 °C, the device restarts by initiating the soft-start sequence again.

Soft Start up

SiP12109 soft-start time is adjustable by selecting a capacitor value from the following equation. Once V_{CC} is above UVLO level (2.55 V typ.), V_{OUT} will ramp up slowly, rising monotonically to the programmed output voltage. There is an internal 5 μ A current source tied to the soft start pin which charges the external soft start cap

time =
$$\frac{\text{Cext x 0.8 V}}{5 \, \mu \text{A}}$$

During soft-start period, OCP is activated. OVP and

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short-circuit protection are not active until soft-start is complete.

Pre-bias Startup

In case of pre-bias startup, output is monitored through V_{FB} pin. If the sensed voltage on V_{FB} is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage

spike and excessive current sinking through LS FET.

Power Good (P_{GOOD})

SiP12109's power good is an open-drain output. Pull PGOOD pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the below diagram. If voltage level on V_{FB} pin is out of this window, P_{GOOD} signal is de-asserted by pulling down to GND.

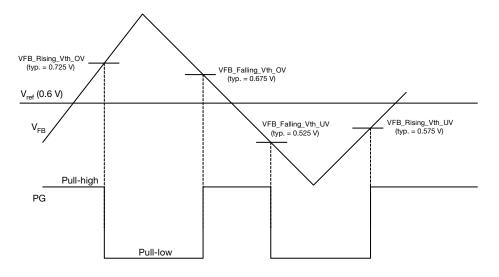
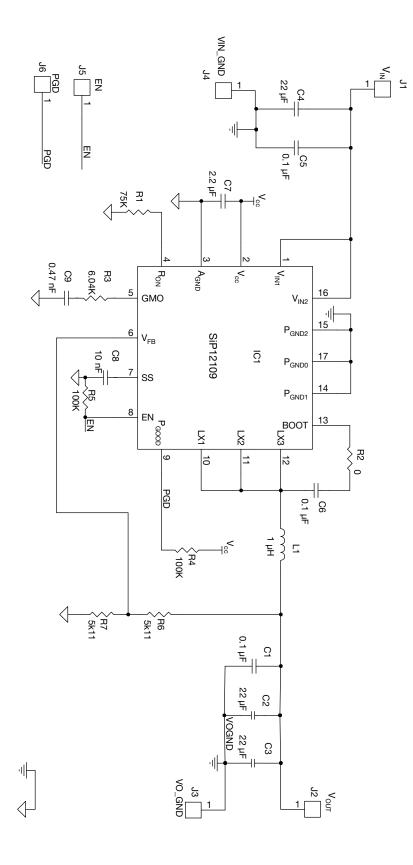


Fig. 23 - PGOOD Window and Timing Diagram





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SiP12109



BILI	L OF	MATERIAL					
ITEM	QTY	REFERENCE	VALUE	VOLTAGE	FOOTPRINT	PART NUMBER	MANUFACTURER
1	3	C1, C5, C6	0.1 µF	35 V	C0402-TDK	GMK105BJ104KV-F	Taiyo Yuden
2	2	C2, C3	22 µF	10 V	C0805-TDK	LMK212BJ226MG-T	Taiyo Yuden
3	1	C4	22 µF	35 V	C0805-TDK	C2012X5R1V226M125AC	TDK
4	1	C7	2.2 µF	16 V	C0603-TDK	C0603C225K4PACTU	Kemet
5	1	C8	10 nF	16 V	C0402-TDK	CC0402KRX7R7BB103	Yageo
6	1	C9	0.47 nF	50 V	C0402-TDK	C1005C0G1H471J050BA	TDK
7	1	IC1	SiP12109	-	QFN16 3 x 3	SiP12109DMP-T1-GE4	Vishay
8	6	J1, J2, J3, J4, J5, J6	V _{IN} , V _{OUT} , V _{O_GND} , V _{IN_GND} , EN, PGD	-	TP30	2108-2-00-44-00-00-07	Mill-Max
9	1	L1	1 µH	-	IHLP1616	IHLP1616BZER1R0M11	Vishay
10	1	R1	75K	-	R0402-Vishay	CRCW040275K0FKEDHP	Vishay
11	1	R2	0	-	R0402-Vishay	RCG04020000Z0ED	Vishay
12	1	R3	6.04K	-	R0402-Vishay	CRCW04026K04FKED	Vishay
13	2	R4, R5	100K	-	R0402-Vishay	CRCW0402100KFKED	Vishay
14	2	R6, R7	5k11	-	R0402-Vishay	CRCW04025K11FKED	Vishay

Fig. 24 - Reference Board Schematic

PCB LAYOUT OF REFERENCE BOARD

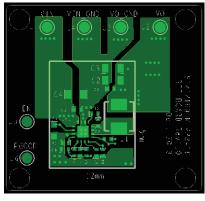


Fig. 25 - Top Layer

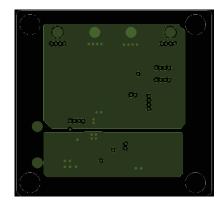


Fig. 26 - Inner Layer1

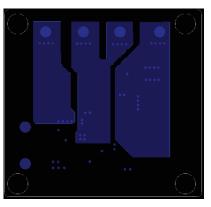


Fig. 27 - Bottom Layer

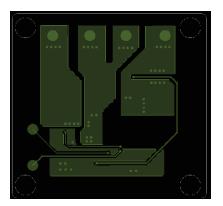


Fig. 28 - Inner Layer2



Vishay Siliconix

	0.040400
Part number	SiP12109
Description	4 A, 4.5 V to 15 V input, 1.5 MHz synchronous buck regulator
Input voltage min. (V)	4.5
Input voltage max. (V)	15
Output voltage min. (V)	0.6
Output voltage max. (V)	5.5
Continuous current (A)	4
Switch frequency min. (kHz)	200
Switch frequency max. (kHz)	1500
Pre-bias operation (yes / no)	Yes
Internal bias reg. (yes / no)	Yes
Compensation	External
Enable (yes / no)	Yes
P _{GOOD} (yes / no)	Yes
Overcurrent protection	Fixed
Protection	OVP, OCP, OTP, SCP, UVLO
Light load mode	Powersave
Peak efficiency (%)	95
Package type	QFN16-33G
Package size (W, L, H) (mm)	3.0 x 3.0 x 0.8
Status code	2
Product type	microBUCK (step down regulator)
Applications	Computing, consumer, networking, industrial, healthcare

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62694.



Vishay

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